NEC

# Data Sheet Addendum

# V850ES/Fx3-L

## 32-bit Single-Chip Microcontroller

## Injected Current

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| V850ES/FE3-L: | V850ES/FF3-L: | V850ES/FG3-L: |
|---|---|---|
| µPD70F3610 | µPD70F3615 | µPD70F3620 |
| µPD70F3611 | µPD70F3616 | µPD70F3621 |
| µPD70F3612 | µPD70F3617 | µPD70F3622 |
| µPD70F3613 | µPD70F3618 | |
| µPD70F3614 | µPD70F3619 | |

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# Notes for CMOS Devices

1. **Precaution against ESD for semiconductors**
   Strong electric field, when exposed to a MOS device, can cause destruction of the gate oxide and ultimately degrade the device operation. Steps must be taken to stop generation of static electricity as much as possible, and quickly dissipate it once, when it has occurred. Environmental control must be adequate. When it is dry, humidifier should be used. It is recommended to avoid using insulators that easily build static electricity. Semiconductor devices must be stored and transported in an anti-static container, static shielding bag or conductive material. All test and measurement tools including work bench and floor should be grounded. The operator should be grounded using wrist strap. Semiconductor devices must not be touched with bare hands. Similar precautions need to be taken for PW boards with semiconductor devices on it.

2. **Handling of unused input pins for CMOS**
   No connection for CMOS device inputs can be cause of malfunction. If no connection is provided to the input pins, it is possible that an internal input level may be generated due to noise, etc., hence causing malfunction. CMOS devices behave differently than Bipolar or NMOS devices. Input levels of CMOS devices must be fixed high or low by using a pull-up or pull-down circuitry. Each unused pin should be connected to VDD or GND with a resistor, if it is considered to have a possibility of being an output pin. All handling related to the unused pins must be judged device by device and related specifications governing the devices.

3. **Status before initialization of MOS devices**
   Power-on does not necessarily define initial status of MOS device. Production process of MOS does not define the initial operation status of the device. Immediately after the power source is turned ON, the devices with reset function have not yet been initialized. Hence, power-on does not guarantee out-pin levels, I/O settings or contents of registers. Device is not initialized until the reset signal is received. Reset operation must be executed immediately after power-on for devices having reset function.

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For further information please contact:

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1753, Shimonumabe, Nakahara-ku,
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Tel: 044 4355111
http://www.necel.com/

**[America]**

**NEC Electronics America, Inc.**
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U.S.A.
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**NEC Electronics (Europe) GmbH**
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Linford Wood
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18322 Täby, Sweden
Tel: 08 6387200

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20124 Milano, Italy
Tel: 02 667541

**Branch The Netherlands**
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The Netherlands
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ZhiChunLu Haidian District,
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Tel: 010 82351155
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200 Yincheng Road Central,
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Tel: 021 5888 5400
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# Table of Contents

# 1. Pin Group Information

## 1.1 Device package information

The V850ES/Fx3-L device series comprises several members. An overview with the pin and package information is given in the following table:

| Series Member | # Pins | Device package information |
|---|---|---|
| µPD70F3610<br>µPD70F3611<br>µPD70F3612<br>µPD70F3613<br>µPD70F3614 | 64 | FE3-L |
| µPD70F3615<br>µPD70F3616<br>µPD70F3617<br>µPD70F3618<br>µPD70F3619 | 80 | FG3-L |
| µPD70F3620<br>µPD70F3621<br>µPD70F3622 | 100 | FG3-L |

## 1.2 Pin Groups 1x: Pins supplied by EVDD

1B: (SHMT1)
- P04, P30-31, P34; P40, P91, P913-915 (FE3-L)
- P04, P30-31, P34; P38-39, P40, P91, P913-915 (FF3-L)
- P04, P30-31, P34; P36-39, P40, P91, P911, P913-915 (FG3-L)

1D: (SHMT3)
- P00-03, P05-P06, P32-33, P35, P41-42, P50-55, P90, P96-99 (FE3-L)
- P00-03, P05-P06, P32-33, P35, P41-42, P50-55, P90, P96-99 (FF3-L)
- P00-03, P05-P06, P10-11, P32-33, P35, P41-42, P50-55, P90, P92-910, P912 (FG3-L)

## 1.3 Pin Groups 2x: Pins supplied by EVDD

2A: (CMOS)
- PCM0-1 (FE3-L)
- PCM0-3, PCS0-1, PCT0-1, PCT4, PCT6 (FF3-L)

2D: (SHMT3)
- PDL0-7 (FE3-L)
- PDL0-11 (FF3-L)

## 1.4 Pin Groups 3x: Pins supplied by BVDD

3A: (CMOS)
- PCM0-3, PCS0-1, PCT0-1, PCT4, PCT6 (FG3-L)

3D: (SHMT3)
- PDL0-13 (FG3-L)

## 1.5 Pin Groups 4: Pins supplied by AVREF0

4: (CMOS)
- P70-79 (FE3-L)
- P70-711 (FF3-L)
- P70-715 (FG3-L)

### 1.6 Pin Groups 6: Pins supplied by EVDD

- RESET (SHMT2)
- IC, FLMD0

### 1.7 Pin Groups 7: Pins supplied by VRO

- X1, X2, XT1, XT2

## 2. Electrical Specifications of (A)-Grade

This product has to be used only under the conditions of VDD=EVDD=BVDD. Operation is not ensured at the time of using this product except this condition.

### 2.1 Absolute Maximum Ratings

**Absolute Maximum Ratings (Ta=25°C)**

| Parameter | Symbol | Conditions | | Rating | Unit |
|---|---|---|---|---|---|
| Supply voltage | VDD | VDD=EVDD=BVDD | | -0.5 to +6.5 | V |
| | EVDD | VDD=EVDD=BVDD | | -0.5 to +6.5 | V |
| | BVDD | VDD=EVDD=BVDD | | -0.5 to +6.5 | V |
| | AVREF0 | | | -0.5 to +6.5 | V |
| | VSS | VSS=EVSS=BVSS=AVSS | | -0.5 to +0.5 | V |
| | EVSS | VSS=EVSS=BVSS=AVSS | | -0.5 to +0.5 | V |
| | BVSS | VSS=EVSS=BVSS=AVSS | | -0.5 to +0.5 | V |
| | AVSS | VSS=EVSS=BVSS=AVSS | | -0.5 to +0.5 | V |
| Pos. Overload Current $V_{IN} > V_{DD}$ | $I_{INJPM}$ Note1 | Pin Group 1x, 2x | 1 pin | 4 | mA |
| | | | Total | 50 | mA |
| | | Pin Group 3x | 1 pin | 4 | mA |
| | | | Total | 50 | mA |
| | | Pin Group 4 | 1 pin | 4 | mA |
| | | | Total | 20 | mA |
| Neg. Overload Current $V_{IN} < V_{SS}$ | $I_{INJNM}$ Note1 | Pin Group 1x, 2x | 1 pin | -4 | mA |
| | | | Total | -50 | mA |
| | | Pin Group 3x | 1 pin | -4 | mA |
| | | | Total | -50 | mA |
| | | Pin Group 4 | 1 pin | -4 | mA |
| | | | Total | -20 | mA |

**Notes: 1.** Be sure not to exceed the absolute maximum ratings (Max. value) of each supply voltage.

**Remark:** BVDD and BVSS are not available for V850ES/FE3-L and V850ES/FF3-L.

## 2.2 DC Characteristics

### 2.2.1 Overload Current

**(Ta = -40 to +85°C, VDD = EVDD = BVDD = 3.3V to 5.5V, 4.0 ≤ AVREF0 ≤ 5.5V, VSS = EVSS = BVSS = AVSS = 0V)**

| Parameter | Symbol | Conditions | | MIN | TYP | MAX | Unit |
|---|---|---|---|---|---|---|---|
| Pos. Overload Current $V_{IN} > V_{DD}$ | $I_{INJP}$ | Pin Group 1x, 2x | 1 pin | | | 2 | mA |
| | | | Total | | | 20 | mA |
| | | Pin Group 3x | 1 pin | | | 2 | mA |
| | | | Total | | | 20 | mA |
| | | Pin Group 4 | 1 pin | | | 2 | mA |
| | | | Total | | | 12 | mA |
| Neg. Overload Current $V_{IN} < V_{SS}$ Note1 | $I_{INJN}$ | Pin Group 1x, 2x | 1 pin | | | -0.5 | mA |
| | | | Total | | | -5 | mA |
| | | Pin Group 3x | 1 pin | | | -0.5 | mA |
| | | | Total | | | -5 | mA |
| | | Pin Group 4 | 1 pin | | | -0.5 | mA |
| | | | Total | | | -3 | mA |

**Remarks: 1.** Not tested in production.

**2.** Refer to the next paragraphs for Input leakage current and A/D characteristics.

**Notes: 1.** In case of using Sub clock, an adjacent pin of XT2 pin is the following specification.

| Parameter | Symbol | Conditions | MIN | TYP | MAX | Unit |
|---|---|---|---|---|---|---|
| Neg. Overload Current $V_{IN} < V_{SS}$ | $I_{INJN}$ | an adjacent pin of XT2 pin Note2 | | | -0.1 | mA |

**2.** The adjacent pin of XT2 pin is as follows:
V850ES/FE3-L: P00 pin, V850ES/FF3-L: P05 pin, V850ES/FG3-L: P02 pin

#### 2.2.1.1 DC Characteristics for input pins influenced by injected current on adjacent pins

**(Ta = -40 to +85°C, VDD = EVDD = BVDD = 3.3V to 5.5V, 4.0 ≤ AVREF0 ≤ 5.5V, VSS = EVSS = BVSS = AVSS = 0V)**

| Parameter | Symbol | Conditions | | MIN | TYP | MAX | Unit |
|---|---|---|---|---|---|---|---|
| Leakage current coupling factor for pos. Overload Current | $K_{INJP}$ | Pin Group 1x, 2x, 3x | | | | $2.5 \times 10^{-4}$ | |
| | | Pin Group 4 | | | | $2.5 \times 10^{-4}$ | |
| Leakage current coupling factor for neg. Overload Current | $K_{INJN}$ | Pin Group 1x, 2x, 3x | | | | $2.5 \times 10^{-3}$ | |
| | | Pin Group 4 | | | | $1.5 \times 10^{-3}$ | |

**Remarks: 1.** These specifications are not tested in outgoing inspection, but specified based on the device characterization.

**2.** An overload current through a input pin will cause a certain error current in the adjacent input pins. This error current must be added to the respective leakage current (ILIH / ILIL) of the adjacent pins.

**3.** The amount of error leakage current depends on the overload current and is defined by the overload coupling factor KINJ. The total leakage current through a input pin is:
| IPINtotal | =| ILIx | + (| IINJy | * KINJy) + (| IINJz | * KINJz)

- x=H or L
- y=P or N and IINJy is the overload current of the pin that is adjacent directly to the right side
- z=P or N and IINJz is the overload current of the pin that is adjacent directly to the left side

#### 2.2.1.2 A/D converter influenced by injected current on adjacent pins

**(Ta = -40 to +85°C, VDD = EVDD = BVDD = 3.3V to 5.5V, 4.0 ≤ AVREF0 ≤ 5.5V, VSS = EVSS = BVSS = AVSS = 0V)**

| Parameter | Symbol | Conditions | MIN | TYP | MAX | Unit |
|---|---|---|---|---|---|---|
| Degradation of Overall error[Note1] | | $I_{INJP}$ = 1 mA | | | +/- 0.10 | %FSR |
| | | $I_{INJN}$ = -0.5 mA | | | +/- 0.25 | %FSR |

**Remark:** These specifications are not tested in outgoing inspection, but specified based on the device characterization.

**Notes: 1.** This value is the degradation by injected current on an adjacent pin. Therefore, this value is added to the specification of A/D converter's overall error defined separately as the electrical specifications.

**2.** When there is an increased leakage current on the analog input pins, based on currents injected into the pins adjacent to the converted channel, the effect on the ADC accuracy depends on the external analog source impedance.
Example:

- Conditions: AVREF0 = 5.0V, external analog source impedance = 10K ohm.
  If there is a leakage current of 1uA by injected current, the effect on the ADC accuracy is 1(uA) * 10K(ohm) / 5(V) = 0.2%FSR

# 3. Electrical Specifications of (A1)-Grade

This product has to be used only under the conditions of VDD=EVDD=BVDD. Operation is not ensured at the time of using this product except this condition.

## 3.1 Absolute Maximum Ratings

**Absolute Maximum Ratings (Ta=25°C)**

| Parameter | Symbol | Conditions | | Rating | Unit |
|---|---|---|---|---|---|
| Supply voltage | VDD | VDD=EVDD=BVDD | | -0.5 to +6.5 | V |
| | EVDD | VDD=EVDD=BVDD | | -0.5 to +6.5 | V |
| | BVDD | VDD=EVDD=BVDD | | -0.5 to +6.5 | V |
| | AVREF0 | | | -0.5 to +6.5 | V |
| | VSS | VSS=EVSS=BVSS=AVSS | | -0.5 to +0.5 | V |
| | EVSS | VSS=EVSS=BVSS=AVSS | | -0.5 to +0.5 | V |
| | BVSS | VSS=EVSS=BVSS=AVSS | | -0.5 to +0.5 | V |
| | AVSS | VSS=EVSS=BVSS=AVSS | | -0.5 to +0.5 | V |
| Pos. Overload Current $V_{IN} > V_{DD}$ | $I_{INJPM}$ Note1 | Pin Group 1x, 2x | 1 pin | 4 | mA |
| | | | Total | 20 | mA |
| | | Pin Group 3x | 1 pin | 4 | mA |
| | | | Total | 20 | mA |
| | | Pin Group 4 | 1 pin | 4 | mA |
| | | | Total | 10 | mA |
| Neg. Overload Current $V_{IN} < V_{SS}$ | $I_{INJNM}$ Note1 | Pin Group 1x, 2x | 1 pin | -4 | mA |
| | | | Total | -20 | mA |
| | | Pin Group 3x | 1 pin | -4 | mA |
| | | | Total | -20 | mA |
| | | Pin Group 4 | 1 pin | -4 | mA |
| | | | Total | -10 | mA |

**Notes: 1.** Be sure not to exceed the absolute maximum ratings (Max. value) of each supply voltage.

**Remark:** BVDD and BVSS are not available for V850ES/FE3-L and V850ES/FF3-L.

## 3.2 DC Characteristics

### 3.2.1 Overload Current

**(Ta = -40 to +110°C, VDD = EVDD = BVDD = 3.3V to 5.5V, 4.0 ≤ AVREF0 ≤ 5.5V, VSS = EVSS = BVSS = AVSS = 0V)**

| Parameter | Symbol | Conditions | | MIN | TYP | MAX | Unit |
|---|---|---|---|---|---|---|---|
| Pos. Overload Current $V_{IN} > V_{DD}$ | $I_{INJP}$ | Pin Group 1x, 2x | 1 pin | | | 2 | mA |
| | | | Total | | | 20 | mA |
| | | Pin Group 3x | 1 pin | | | 2 | mA |
| | | | Total | | | 20 | mA |
| | | Pin Group 4 | 1 pin | | | 2 | mA |
| | | | Total | | | 10 | mA |
| Neg. Overload Current $V_{IN} < V_{SS}$ Note1 | $I_{INJN}$ | Pin Group 1x, 2x | 1 pin | | | -0.5 | mA |
| | | | Total | | | -5 | mA |
| | | Pin Group 3x | 1 pin | | | -0.5 | mA |
| | | | Total | | | -5 | mA |
| | | Pin Group 4 | 1 pin | | | -0.5 | mA |
| | | | Total | | | -3 | mA |

**Remarks: 1.** Not tested in production.
**2.** Refer to the next paragraphs for Input leakage current and A/D characteristics.

**Notes: 1.** In case of using Sub clock, an adjacent pin of XT2 pin is the following specification.

| Parameter | Symbol | Conditions | MIN | TYP | MAX | Unit |
|---|---|---|---|---|---|---|
| Neg. Overload Current $V_{IN} < V_{SS}$ | $I_{INJN}$ | an adjacent pin of XT2 pin Note2 | | | -0.1 | mA |

**2.** The adjacent pin of XT2 pin is as follows:
V850ES/FE3-L: P00 pin, V850ES/FF3-L: P05 pin, V850ES/FG3-L: P02 pin

#### 3.2.1.1 DC Characteristics for input pins influenced by injected current on adjacent pins

Specification is identical to that from (A)-Grade except Ta=-40 to +110°C.

#### 3.2.1.2 A/D converter influenced by injected current on adjacent pins

Specification is identical to that from (A)-Grade except Ta=-40 to +110°C.

# 4. Electrical Specifications of (A2)-Grade

This product has to be used only under the conditions of VDD=EVDD=BVDD. Operation is not ensured at the time of using this product except this condition.

## 4.1 Absolute Maximum Ratings

Specification is identical to that from (A1)-Grade except Ta=-40 to +125°C.

## 4.2 DC Characteristics

### 4.2.1 Overload Current

Specification is identical to that from (A1)-Grade except Ta=-40 to +125°C.

#### 4.2.1.1 DC Characteristics for input pins influenced by injected current on adjacent pins

Specification is identical to that from (A)-Grade except Ta=-40 to +125°C.

#### 4.2.1.2 A/D converter influenced by injected current on adjacent pins

Specification is identical to that from (A)-Grade except Ta=-40 to +125°C.

## 5. Change History

| Version | Chapter | Comment |
|---|---|---|
| V1.0 | | Initial release |

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