NEC

Customer Notification

V850E/IA3, V850E/IA4™

32-Bit Single-Chip Microcontrollers

Operating Precautions

μPD703183
μPD70F3184
μPD703185
μPD703186
μPD70F3186

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(A) Table of Operating Precautions

No.	Outline		μPD70F3184 μPD70F3186			
		Rev.	1.0	1.1	2.0	
		Rank[Note]	K	E	P	X
1	Port: Software pull-up resistor function missing (Technical limitation)		✗	✗	✓	✓
2	CG: Clock monitor function fails (Technical limitation)		✗	✗	✓	✓
3	TMQ/TMQOP: Dead-time fails on a timing conflict between capture/compare register match and dead-time counter termination (Technical limitation)		✗	✗	✓	✓
4	Standby Function: Entering IDLE or STOP may fail for higher system clock rates (Specification change notice)		✗	✗	✗	✗
5	TMM: Unexpected compare match interrupt after start (Technical limitation)		✗	✗	✓	✓
6	CPU: After reset the system status register (SYS) holds incorrect value (Technical limitation)		✗	✗	✓	✓
7	ADC0, ADC1, ADC2: Low accurracy of conversion results (Technical limitation)		✗	✓	✓	✓
8	INTP6 Pin: Unexpected behavior of edge detection (Technical limitation)		✗	✗	✗	✓
9	ADC0, ADC1: Missing conversion result in one-shot select mode or one-shot scan mode when software trigger mode is selected (Specification change notice)		✗	✗	✗	✗
10	ADC2: Conflict between conversion end and conversion stop (Specification change notice)		✗	✗	✗	✗

✓ : Not applicable

✗ : Applicable

Note: The rank is indicated by the letter appearing at the 5th position from the left in the lot number, marked on each product.

No.	Outline	μPD703183 μPD703185 μPD703186	
	Rev.		
	Rank[Note]	K	E
1	Port: Software pull-up resistor function missing (Technical limitation)	✓	✓
2	CG: Clock monitor function fails (Technical limitation)	✓	✓
3	TMQ/TMQOP: Dead-time fails on a timing conflict between capture/compare register match and dead-time counter termination (Technical limitation)	✓	✓
4	Standby Function: Entering IDLE or STOP may fail for higher system clock rates (Specification change notice)	✗	✗
5	TMM: Unexpected compare match interrupt after start (Technical limitation)	✓	✓
6	CPU: After reset the system status register (SYS) holds incorrect value (Technical limitation)	✓	✓
7	ADC: Low accurracy of conversion results (Technical limitation)	✓	✓
8	INTP6 Pin: Unexpected behavior of edge detection (Technical limitation)	✗	✓
9	ADC0, ADC1: Missing conversion result in one-shot select mode or one-shot scan mode when software trigger mode is selected (Specification change notice)	✗	✗
10	ADC2: Conflict between conversion end and conversion stop (Specification change notice)	✗	✗

✓ : Not applicable

✗ : Applicable

Note: The rank is indicated by the letter appearing at the 5th position from the left in the lot number, marked on each product.

(B) Description of Operating Precautions

No. 1	Port: Software pull-up resistor function missing (Technical limitation)

Details

If the PUDLn bit in the PUDL regsiter is set (1) and the corresponding PMDLn bit specifies the input mode (1), a pull-up resistor is connected to the port pin PDLn (n = 0 to 15).
However, in case of port pins PDL4 or PDL5 the pull-up resistor is not connected even if the PUDL4 or PUDL5 bits set to (1) in input mode.

Workaround

If necessary, use external pull-up resistors for port pins PDL4 and PDL5.

No. 2	CG: Clock monitor function fails (Technical limitation)

Details

Normally the clock monitor function samples the main oscillator clock using the on-chip ring oscillator. If a standstill of the main oscillator is detected, the timer outputs for the motor control go into high -impedance state.
However, even if the monitor function detects a standstill of the main oscillator, there is the possibility that the timer outputs will not enter high-impedance state.

Workaround

None.

No. 3	TMQ/TMQOP: Dead-time fails on a timing conflict between capture/compare register match and dead-time counter termination (Technical limitation)

Details

Due to a timing conflict there are two cases where the TMQ/TMQOP timer outputs change the output state although the dead time has not completely elapsed.

Case 1: When the TMQm capture/compare register n (TQmCCRn) matches with TMQm value, and the TMQn dead-time compare register (TQmDTC) matches with the dead-time counter value simultaneously, the timer output (TOQmTnm, TOQmBn) may change unintentionally.

Case 2: When the TMQm capture/compare register n (TQmCCRn) is rewritten by a reload, and the TMQn dead-time compare register (TQmDTC) matches with the dead-time counter value simultaneously, the timer output (TOQmTnm, TOQmBn) may change unintentionally.

Remark: m = 0, 1
n = 1 to 3

Workaround

Set the TMQm dead-time compare register with an odd value, and set the TMQm capture/compare register with an even value.

No. 4	Standby Function: Entering IDLE or STOP may fail for higher system clock rates (Specification change notice)

Details

When IDLE or STOP modes are entered while the internal system clock is set to higher clock rates, entering the standby mode may fail.

Workaround

Before entering the IDLE or STOP mode set the lowest clock rate for internal system clock using the PCC register .

Example

```
mov     0x03, r10          ; set internal system clock to fXX/8
st.b    r10, PRCMD[r0]
st.b    r10, PCC[r0]
mov     0x01, r10          ; STOP mode = 0x01, IDLE mode = 0x00
st.b    r10, PSMR[r0]
mov     0x02, r10          ; enter standby mode
st.b    r10, PRCMD[r0]
st.b.   r10, PSC[r0]
nop
nop
nop
nop
nop
(next instruction)
```

No. 5	TMM: Unexpected compare match interrupt after start (Technical limitation)

Details

If the TMM compare register 0 (TMM0CM0) is set to FFFFH, and when counting is admitted (TM0CE bit = 1), an interrupt occurs simultaneously when the counter starts.

Workaround

Don not set TMM compare register 0 (TMM0CM0) to FFFFH. Use a value in the range from 0000H to FFFEH.

No. 6	CPU: After reset the system status register (SYS) holds incorrect value (Technical limitation)

Details

After releasing reset, the PRERR flag in the system status register (SYS) is incorrectly set to 1.

Workaround

Clear the PRERR flag to 0 by software after reset.

No. 7	ADC: Low accurracy of conversion results (Technical limitation)

Details

Due to the analog power supply, where AVDD0 and AVDD1 pins are connected inside, and connected to AVDD and AVREF of A/D converters 0 to 2, as well as to operational amplifiers, comparators, and analog input buffers, the accurracy is restricted.

For acccurracy improvement of the A/D converters, the inside connection of AVDD0 and AVDD1 pins has been changed for future versions.
AVDD0 and AVDD1 pins split the analog power supplies as follows:
AVDD0 pin is connected to AVREF and analog input buffers of A/D converters 0 to 2.
AVDD1 pin is connected to AVDD of A/D converters 0 to 2, operational amplifiers, and comparators.

Workaround

None.

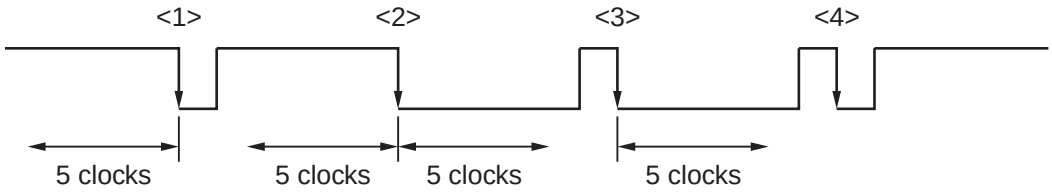
No. 8	INTP6 Pin: Unexpected behavior of edge detection (Technical limitation)

Details

(1) Judgement of inactive/active level duration

The INTP6 pin features a digital noise elimination function that eliminates a pulse of 5 clocks or shorter as noise. When an inactive level continues 5 clocks or longer, an interrupt edge is input, and then an active level is input for 5 clocks or longer, this function acknowledges the input as an interrupt. Against the expected behavior the device judge the occurrence of interrupts only by the active level period, so when the specified edge is input by the noise, etc., during an active level and the active level is input for 5 clocks or longer, this function acknowledges the input as an interrupt (see <3> below).

<Operation when falling edge is specified>



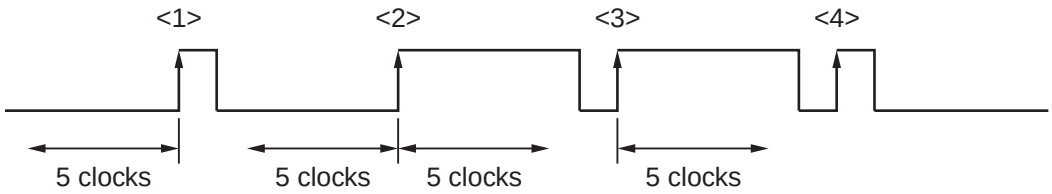
<1>: The low-level period after the falling edge is shorter than 5 clocks, so the input signal is eliminated as noise (normal operation).

<2>: The high-/low-level period before/after the falling edge is longer than 5 clocks, so the input signal is acknowledged as an interrupt (normal operation).

<3>: The low-level period after the falling edge is longer than 5 clocks, so the input signal is acknowledged as an interrupt **(operation affected by this limitation)**.
In accordance with the specifications, a high-level period of 5 clocks or longer is required before the falling edge of <3>, but a low-level period after the falling edge continues for longer than 5 clocks, so the input signal is acknowledged as an interrupt.

<4>: The low-level period after the falling edge is shorter than 5 clocks, so the input signal is eliminated as noise (normal operation).

<Operation when rising edge is specified>



<1>: The high-level period after the rising edge is shorter than 5 clocks, so the input signal is eliminated as noise (normal operation).

<2>: The high-/low-level period before/after the rising edge is longer than 5 clocks, so the input signal is acknowledged as an interrupt (normal operation).

No. 8	INTP6 Pin: Unexpected behavior of edge detection (Technical limitation)

(cont.)

<3>: The high-level period after the rising edge is longer than 5 clocks, so the input signal is acknowledged as an interrupt **(operation affected by this limitation)**.
In accordance with the specifications, a low-level period of 5 clocks or longer is required before the rising edge of <3>, but a high-level period after the rising edge continues for longer than 5 clocks, so the input signal is acknowledged as an interrupt.

<4>: The high-level period after the rising edge is shorter than 5 clocks, so the input signal is eliminated as noise (normal operation).

(2) Occurrenc of illegal interrupt in accordance with pin level when edge is specified

INTP6 is an interrupt pin for which an input edge can be specified. If the pin level is high when the rising edge has been specified, or if the pin level is low when the falling edge has been specified, an interrupt occurs even if no edge is input. An interrupt does not occur when setting is other than above (see tabel below).

	Pin Level = H	Pin Level = L
Rising edge specified	Illegal interrupt occurs	Behavior as expected
Falling edge specified	Behavior as expected	Illegal interrupt occurs

Workaround

(1) Judgement of inactive/active level duration

None.

(2) Occurrenc of illegal interrupt in accordance with pin level when edge is specified

Clear bit 7 (interrupt request flag) of the interrupt control register (PIC6) via software after writing to INTR06 and INTF06, and before releasing the interrupt masking.

No. 9	ADC0, ADC1: Missing conversion result in one-shot select mode or one-shot scan mode when software trigger mode is selected (Specification change notice)

Details

While A/D converters 0 and 1 are set as described in <1> or <2> below, if a write is performed on any of the A/D conversion registers described in <3> at the same time as completion of an A/D conversion, then normally the re-conversion operation is executed with a new condition.
However, the re-conversion operation is not performed and the A/D converter enters the state described in <4>, due to this restriction. In addition, no conversion end interrupts occur, and the last A/D conversion result is not stored.
Writing to the A/D conversion register (described in <3>) itself is performed normally.
When this situation occurs, the A/D converter can return to normal operation by setting ADAnM0.ADAnCE to 1.

<1>: One-shot select mode and software trigger mode are set (ADAnM0 = 1010xx0xb)

<2>: One-shot scan mode and software trigger mode are set (ADAnM0 = 1011xx0xb)

<3>: ADAnM0, ADAnM2, or ADAnS

<4>: A/D conversion operation is enabled (ADAnM0.ADAnCE = 1) and A/D conversion is being stopped (ADAnM0.ADAnEF = 0)

Remark: n = 0 or 1

Example

For example, 2-channels (ANIn0 and ANIn1) scanning (ADAnS = 00000001b) and modes as described in <2> are set. When a write is performed on a target register (<3>) during a conversion, at the same time as completion of the conversion, conversion for ANIn0 and storing the conversion result in the ADAnCR0 register are performed normally, but the result of conversion for ANIn1, which is executed immediately before completion of the conversion, is not stored in the ADAnCR1 register, and no conversion end interrupts occur.

Remark: Other modes and A/D converter 2 are not affected by this specification change.

No. 9	ADC0, ADC1: Missing conversion result in one-shot select mode or one-shot scan mode when software trigger mode is selected (Specification change notice)

(cont.)

Workaround

When performing a write to registers in <3> while <1> or <2> is set, avoid this restriction by implementing any of the following workarounds with software.

Workaround 1:

(1) Confirm that ADAnM0.ADAnEF is 0 (A/D conversion has been stopped).
(2) Perform writing to the target register in <3>.

Workaround 2:

(1) Disable acknowledgment of interrupts and DMA transfers.
(2) Successively execute an instruction to write to the target register in <3> and an instruction to set ADAnM0.ADAnCE to 1.
(3) Enable interrupts and DMA transfers.

This step is required for preventing a match between a conversion end timing and a write to a target register. For example, even if the timing at which the first write instruction is executed and the conversion end timing match and then the conversion is stopped, conversion can be started again by the subsequent step of setting ADAnM0.ADAnCE to 1.
If the write instruction is the one that sets ADAnM0.ADAnCE to 1, execute the instruction to set ADAnM0.ADAnCE to 1 twice in succession.

Workaround 3:

(1) Disable A/D conversion operations by clearing ADAnM0.ADAnCE to 0.
(2) Perform writing to the target register in <3>
(3) Enable A/D conversion operations by setting ADAnM0.ADAnCE to 1, and then start A/D conversion.

No. 10	ADC2: Conflict between conversion end and conversion stop (Specification change notice)

Details

When using A/D converter 2 the following critical situtations may occur between conversion end and conversion stop timing.

(1) If a conflict occurs between the timing at which a conversion result in conversion register SAR is stored in conversion result register ADA2CRn (storage timing) and the timing at which A/D conversion is stopped by the program operation (ADA2CTL0.ADA2CE = 0), an undefined value is written to the conversion result register.

(2) If a conflict occurs between the storage timing and the timing at which status register ADA2STR is read by program processing, an undefined value is read. The status register value itself is updated correctly.

(3) If a conflict occurs between the storage timing and the timing at which an analog input pin is switched by program processing (write to ADA2CTL2), an undefined value is written to the conversion result register. The analog input pin itself is switched correctly (value written to ADA2CTL2 is correctly set).

Remark: A/D converters 0 and 1 are not affected by this specification change.

Workaround

Workaround for situation (1)

(a) Method to stop A/D conversion without causing conflict (implement one of the following.)

1. Immediately set ADA2CTL0 to 0x80 or 0x00 in the servicing of the conversion end interrupt (INTAD2) of A/D converter 2.
   If setting cannot be performed immediately due to the interrupt priority or occurrence of multiple interrupts, stop the conversion before the next storage timing.
2. Start DMA by using conversion end interrupt INTAD2 of A/D converter 2 to set ADA2CTL0 to 0x80 or 0x00.

(b) Method to prevent conversion result value from being used illegally, without stopping A/D conversion (implement one of the following.)

1. Immediately read the conversion result register in the servicing of the conversion end interrupt (INTAD2) of A/D converter 2.
   If reading cannot be performed immediately due to the interrupt priority or occurrence of multiple interrupts, read the conversion result register before the next storage timing.
2. Start DMA by using conversion end interrupt INTAD2 of A/D converter 2 to read the conversion result register.
3. Read the conversion result register twice in succession and compare the read values. If the values match, the read value is correct. If the values do not match, read the value again and consider that the value read last is correct. Continue the judgment by reading the value twice until both last read values match, but perform this series of processes before the next conversion ends.

No. 10	ADC2: Conflict between conversion end and conversion stop (Specification change notice)
	(cont.) *Workaround* Workaround for situation (2) Read the status register twice in succession and compare the read values. If the values match, the value is correct. If the values do not match, read the value again and consider that the value read last is correct. Continue the judgment by reading the value twice until both last read values match, but perform this series of processes before the next conversion ends. Workaround for situation (3) Switch the analog input pin before reading the conversion result register.

(C) Valid Specification

Item	Date published	Document No.	Document Title
1	September 2005	U16543EJ3V0UD00	V850E/IA3, V850E/IA4 32-Bit Single-Chip Microcontroller Hardware (User's Manual)
2	February 2004	U14559EJ3V1UM00	V850E1 32-Bit Microprocessor Core Architecture (User's Manual)

(D) Revision History

Item	Date published	Document No.	Comment
1	July 2004	TPS-HE-B-4250	First release
2	March 2005	TPS-HE-B-4251	Operatings precautions no. 7 and 8 were added. Table of operating precautions for mask ROM versions μPD703183, μPD703185, and μPD703186 was added
3	July 2005	TPS-HE-B-4252	Operating precaution no. 9 was added.
4	May 2006	TPS-HE-B-4253	Operating precaution no. 10 was added.