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RENESAS TECHNICAL UPDATE

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Renesas Electronics Corporation

Product Category	MPU/MCU		Document No.	TN-RZ*-A0157A/E	Rev.	1.00
Title	User's manual update		Information Category	Technical Notification		
Applicable Product	RZ/G3S	Lot No. All	Reference Document	RZ/G3S Group User's Manual: Hardware Rev.1.20		

This Technical Update is intended to inform customers of partial revisions to the technical information (User's Manual) for the applicable products.
Further details, including the background of this update, its impact on customers, and detailed explanations with before-and-after comparisons, are provided in the attached document.

■Supplementary Explanation and Before/After Comparison
RZ/G3S User's Manual Update
Supplementary Explanation and Before/After Comparison
Rev 1.00

■Updated Contents
Modification of Register Descriptions (Default values & information)
- Chapter 28. xSPI - Command Map Configuration
- Chapter 28. xSPI - Common Status Register
- Chapter 32B. USB2.0 Function - PHY Function Control Register
- Chapter 39. ADC - A/D Converter Mode Register 1(ADM1)
- Chapter 22. Realtime Clock(RTC) - RTC Time Capture
- Chapter 42. VBATT – RTC Time Capture

Modification of Calculation Equations
- Chapter 18. GPT - Automatic Dead Time Setting correction
- Chapter 39. ADC - ADCR calculation formula

Added Supplemental Information
- Chapter 30. CAN-FD - DMA
- Chapter 33. SD/MMC - SD card clock supply

Update of Pin List
- Chapter 1.4. Pin Function List - Condition at Reset (PRST_N = "L")
- Chapter 1.4. Pin Function List - Handling for Unused Pins (xSPI, I3C)
- Chapter 1.4. Pin Function List - Handling for Unused Pins (xSPI, I3C) Software workaround

Update of I3C
- Chapter 26. * (An overall revision and update)

RZ/G3S User's Manual Update
Supplementary Explanation and Before/After Comparison

Renesas Electronics Corporation
Rev 1.00

RENESAS TECHNICAL UPDATE TN-RZ*-A0157A/E

Overview for Update

■ Updated Contents

✓ **Modification for Register Descriptions (Default values & information)**
- Chapter 28. xSPI - Command Map Configuration
- Chapter 28. xSPI - Common Status Register
- Chapter 32B. USB2.0 Function - PHY Function Control Register
- Chapter 39. ADC - A/D Converter Mode Register 1(ADM1)
- Chapter 22. Realtime Clock(RTC) - RTC Time Capture
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✓ **Modification for Calculation Equations**
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- Chapter 30. CAN-FD - DMA
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✓ **Update for Pin List**
- Chapter 1.4. Pin Function List - Condition at Reset (PRST_N = “L”)
- Chapter 1.4. Pin Function List - Handling for Unused Pins (xSPI, I3C)
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✓ **Update for I3C**
- Chapter 26. *(An overall revision and update)

MODIFICATION FOR REGISTER DESCRIPTIONS

Chapter 28. xSPI - Command Map Configuration

■ Update Background

- ✓ Correction of an error in the xSPI Command Map Configuration Register specification.

■ Impact on Customers(Details of the Issues or Issues Addressed)

- ✓ If the current UM is referenced, the initial value of the xSPI Command Map Configuration Register 0 CS0 (CMCFG0CS0) (Offset Address: H'010) may be configured based on an incorrect initial value description.
- ✓ This change corrects a documentation error in the register initial values after HW reset release.
- ✓ The actual device behavior complies with the specification, and please configure the settings to match the address size of the xSPI in use.

■ Details of the Fixes

- ✓ Table 28.4 Register Configuration (1/2) in 28.3 Register Descriptions
  Correction of the initial value of xSPI Command Map Configuration Register 0 CS0 (CMCFG0CS0) (Offset Address: H'010).
  Before change : H'0000_0000
  After change : H'0000_0008

- ✓ 28.3.1.4 xSPI Command Map Configuration Register 0 CSn
  Correction of initial values for bits 3 and 2 of xSPI Command Map Configuration Register 0 CS0 (CMCFG0CS0) (Offset Address: H'010).
  Before change : ADDSIZE[1:0] = 00b (n=0,1)
  After change : ADDSIZE[1:0] = 10b (n=0), 00b (n=1)

■ Affected Scope due to this Update

- ✓ This correction applies only to the UM description and has no impact on device functionality or silicon behavior.

Before

28.3 Register Descriptions

Table 28.4 Register Configuration (1/2)

Register Name	Abbreviation	R/W	Initial Value	Offset Address	Access Size
xSPI Wrapper Configuration Register	WRAPCFG	R/W	H'0000_0000	H'000	32
xSPI Common Configuration Register	COMCFG	R/W	H'0000_0000	H'004	32
xSPI Bridge Map Configuration Register	BMCFG	R/W	H'0000_0000	H'008	32
xSPI Command Map Configuration Register 0 CS0	CMCFG0CS0	R/W	H'0000_0000	H'010	32
xSPI Command Map Configuration Register 0 CS1	CMCFG0CS1	R/W	H'0000_0000	H'020	32
xSPI Command Map Configuration Register 1 CS0	CMCFG1CS0	R/W	H'0008_0000	H'014	32
xSPI Command Map Configuration Register 1 CS1	CMCFG1CS1	R/W	H'0008_0000	H'024	32
xSPI Command Map Configuration Register 2 CS0	CMCFG2CS0	R/W	H'0008_0000	H'018	32
xSPI Command Map Configuration Register 2 CS1	CMCFG2CS1	R/W	H'0008_0000	H'028	32
xSPI Link I/O Configuration Register CS0	LIOCFGCS0	R/W	H'0007_0000	H'050	32
xSPI Link I/O Configuration Register CS1	LIOCFGCS1	R/W	H'0007_0000	H'054	32
xSPI Bridge Map Control Register 0	BMCTL0	R/W	H'0000_00FF	H'060	32
xSPI Bridge Map Control Register 1	BMCTL1	R/W	H'0000_0000	H'064	32
xSPI Command Map Control Register	CMCTL	R/W	H'0000_0000	H'068	32
xSPI Command Manual Control Register 0	CDCTL0	R/W	H'0000_0000	H'070	32
xSPI Command Manual Control Register 1	CDCTL1	R/W	H'0000_0000	H'074	32
xSPI Command Manual Control Register 2	CDCTL2	R/W	H'0000_0000	H'078	32
xSPI Command Manual Type Buf 0	CDTBUF0	R/W	H'0000_0000	H'080	32
xSPI Command Manual Type Buf 1	CDTBUF1	R/W	H'0000_0000	H'090	32
xSPI Command Manual Type Buf 2	CDTBUF2	R/W	H'0000_0000	H'0A0	32
xSPI Command Manual Type Buf 3	CDTBUF3	R/W	H'0000_0000	H'0B0	32
xSPI Command Manual Address Buf 0	CDABUF0	R/W	H'0000_0000	H'084	32
xSPI Command Manual Address Buf 1	CDABUF1	R/W	H'0000_0000	H'094	32
xSPI Command Manual Address Buf 2	CDABUF2	R/W	H'0000_0000	H'0A4	32
xSPI Command Manual Address Buf 3	CDABUF3	R/W	H'0000_0000	H'0B4	32
xSPI Command Manual Data 0 Buf 0	CDD0BUF0	R/W	H'0000_0000	H'088	32
xSPI Command Manual Data 0 Buf 1	CDD0BUF1	R/W	H'0000_0000	H'098	32
xSPI Command Manual Data 0 Buf 2	CDD0BUF2	R/W	H'0000_0000	H'0A8	32
xSPI Command Manual Data 0 Buf 3	CDD0BUF3	R/W	H'0000_0000	H'0B8	32
xSPI Command Manual Data 1 Buf 0	CDD1BUF0	R/W	H'0000_0000	H'08C	32
xSPI Command Manual Data 1 Buf 1	CDD1BUF1	R/W	H'0000_0000	H'09C	32

After

28.3 Register Descriptions

Table 28.4 Register Configuration (1/2)

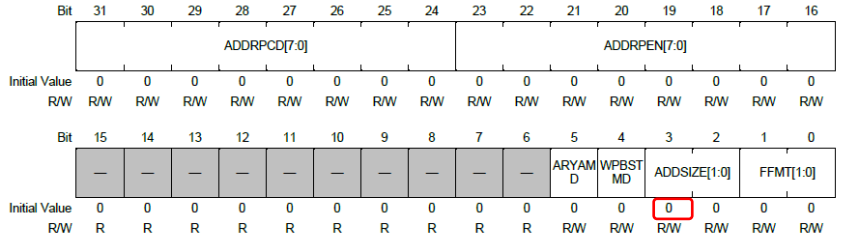
Register Name	Abbreviation	R/W	Initial Value	Offset Address	Access Size
xSPI Wrapper Configuration Register	WRAPCFG	R/W	H'0000_0000	H'000	32
xSPI Common Configuration Register	COMCFG	R/W	H'0000_0000	H'004	32
xSPI Bridge Map Configuration Register	BMCFG	R/W	H'0000_0000	H'008	32
xSPI Command Map Configuration Register 0 CS0	CMCFG0CS0	R/W	H'0000_0008	H'010	32
xSPI Command Map Configuration Register 0 CS1	CMCFG0CS1	R/W	H'0000_0000	H'020	32
xSPI Command Map Configuration Register 1 CS0	CMCFG1CS0	R/W	H'0008_0000	H'014	32
xSPI Command Map Configuration Register 1 CS1	CMCFG1CS1	R/W	H'0008_0000	H'024	32
xSPI Command Map Configuration Register 2 CS0	CMCFG2CS0	R/W	H'0008_0000	H'018	32
xSPI Command Map Configuration Register 2 CS1	CMCFG2CS1	R/W	H'0008_0000	H'028	32
xSPI Link I/O Configuration Register CS0	LIOCFGCS0	R/W	H'0007_0000	H'050	32
xSPI Link I/O Configuration Register CS1	LIOCFGCS1	R/W	H'0007_0000	H'054	32
xSPI Bridge Map Control Register 0	BMCTL0	R/W	H'0000_00FF	H'060	32
xSPI Bridge Map Control Register 1	BMCTL1	R/W	H'0000_0000	H'064	32
xSPI Command Map Control Register	CMCTL	R/W	H'0000_0000	H'068	32
xSPI Command Manual Control Register 0	CDCTL0	R/W	H'0000_0000	H'070	32
xSPI Command Manual Control Register 1	CDCTL1	R/W	H'0000_0000	H'074	32
xSPI Command Manual Control Register 2	CDCTL2	R/W	H'0000_0000	H'078	32
xSPI Command Manual Type Buf 0	CDTBUF0	R/W	H'0000_0000	H'080	32
xSPI Command Manual Type Buf 1	CDTBUF1	R/W	H'0000_0000	H'090	32
xSPI Command Manual Type Buf 2	CDTBUF2	R/W	H'0000_0000	H'0A0	32
xSPI Command Manual Type Buf 3	CDTBUF3	R/W	H'0000_0000	H'0B0	32
xSPI Command Manual Address Buf 0	CDABUF0	R/W	H'0000_0000	H'084	32
xSPI Command Manual Address Buf 1	CDABUF1	R/W	H'0000_0000	H'094	32
xSPI Command Manual Address Buf 2	CDABUF2	R/W	H'0000_0000	H'0A4	32
xSPI Command Manual Address Buf 3	CDABUF3	R/W	H'0000_0000	H'0B4	32
xSPI Command Manual Data 0 Buf 0	CDD0BUF0	R/W	H'0000_0000	H'088	32
xSPI Command Manual Data 0 Buf 1	CDD0BUF1	R/W	H'0000_0000	H'098	32
xSPI Command Manual Data 0 Buf 2	CDD0BUF2	R/W	H'0000_0000	H'0A8	32
xSPI Command Manual Data 0 Buf 3	CDD0BUF3	R/W	H'0000_0000	H'0B8	32
xSPI Command Manual Data 1 Buf 0	CDD1BUF0	R/W	H'0000_0000	H'08C	32
xSPI Command Manual Data 1 Buf 1	CDD1BUF1	R/W	H'0000_0000	H'09C	32

Modified

Before

28.3.1.4 xSPI Command Map Configuration Register 0 CSn (CMCFG0CSn) (n = 0, 1)

This register has functions to configure xSPI Master function.

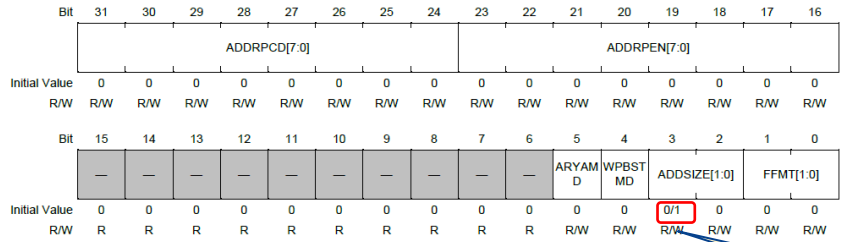


Bit	Bit Name	Initial Value	R/W	Description
31 to 24	ADDRPCD [7:0]	All 0	R/W	Address Replace Code These bits configure the code to replace the MSByte of system bus address in memory-mapping mode. It replaces the corresponding bits when Address Replace Enable bit is set to 1.
23 to 16	ADDRPEN [7:0]	All 0	R/W	Address Replace Enable These bits select the bits to replace for MSByte of system bus address in memory-mapping mode. 0: No replacement (xSPI frame address field is same as system bus address) 1: Replacement
15 to 6	—	All 0	R	Reserved These bits are read as 0. The write value should be 0.
5	ARYAMD	0b	R/W	Array address mode 0: Normal address mode 1: Array address mode When this field is set to 1, address for memory is mapped as {A [25:10], A [9:4], 6{RSV}, A [3:0]} where A [25:0] is normal address, and RSV is reserved value(0b). This field is effective only when FFMT [1:0] = 01b.
4	WPBSTMD	0b	R/W	Wrapping burst mode 0: Separate xSPI transfer at the wrapping address boundary 1: Not separate xSPI transfer at the wrapping address boundary
3, 2	ADDSIZE[1:0]	00b	R/W	Address size These bits configure the number of address byte in memory-mapping mode. In case of 8D-8D-8D profile 2.0, it should be configured to 4 bytes. 0 0: 1 byte (256 bytes address space) 0 1: 2 bytes (64 Kbytes address space) 1 0: 3 bytes (16 Mbytes address space) 1 1: 4 bytes (4 Gbytes address space)
1, 0	FFMT[1:0]	00b	R/W	Frame format These bits configure xSPI frame format in memory-mapping mode. Please see **Table 28.10** for detail. 0 0: Normal format: Command 1 byte, Address ADDSIZE, Data to AHB transaction. 0 1: 8D-8D-8D profile 1.0 format: Command 2 bytes, Address ADDSIZE, Data to AHB transaction 1 0: 8D-8D-8D profile 2.0 Command Modifier format: Command & Modifier 6 bytes, Data to AHB transaction 1 1: 8D-8D-8D profile 2.0 Commands with Extended Command Modifier format: Command & Modifier 6 bytes, Data to AHB transaction

After

28.3.1.4 xSPI Command Map Configuration Register 0 CSn (CMCFG0CSn) (n = 0, 1)

This register has functions to configure xSPI Master function.



Bit	Bit Name	Initial Value	R/W	Description
31 to 24	ADDRPCD [7:0]	All 0	R/W	Address Replace Code These bits configure the code to replace the MSByte of system bus address in memory-mapping mode. It replaces the corresponding bits when Address Replace Enable bit is set to 1.
23 to 16	ADDRPEN [7:0]	All 0	R/W	Address Replace Enable These bits select the bits to replace for MSByte of system bus address in memory-mapping mode. 0: No replacement (xSPI frame address field is same as system bus address) 1: Replacement
15 to 6	—	All 0	R	Reserved These bits are read as 0. The write value should be 0.
5	ARYAMD	0b	R/W	Array address mode 0: Normal address mode 1: Array address mode When this field is set to 1, address for memory is mapped as {A [25:10], A [9:4], 6{RSV}, A [3:0]} where A [25:0] is normal address, and RSV is reserved value(0b). This field is effective only when FFMT [1:0] = 01b.
4	WPBSTMD	0b	R/W	Wrapping burst mode 0: Separate xSPI transfer at the wrapping address boundary 1: Not separate xSPI transfer at the wrapping address boundary
3, 2	ADDSIZE[1:0]	10b (n = 0) 00b (n = 1)	R/W	Address size These bits configure the number of address byte in memory-mapping mode. In case of 8D-8D-8D profile 2.0, it should be configured to 4 bytes. 0 0: 1 byte (256 bytes address space) 0 1: 2 bytes (64 Kbytes address space) 1 0: 3 bytes (16 Mbytes address space) 1 1: 4 bytes (4 Gbytes address space)
1, 0	FFMT[1:0]	00b	R/W	Frame format These bits configure xSPI frame format in memory-mapping mode. Please see **Table 28.10** for detail. 0 0: Normal format: Command 1 byte, Address ADDSIZE, Data to AHB transaction. 0 1: 8D-8D-8D profile 1.0 format: Command 2 bytes, Address ADDSIZE, Data to AHB transaction 1 0: 8D-8D-8D profile 2.0 Command Modifier format: Command & Modifier 6 bytes, Data to AHB transaction 1 1: 8D-8D-8D profile 2.0 Commands with Extended Command Modifier format: Command & Modifier 6 bytes, Data to AHB transaction

Modified

Chapter 28. xSPI - Common Status Register

■ Update Background

- ✓ Correction of an error in the xSPI Common Status Register specification.

■ Impact on Customers(Details of the Issues or Issues Addressed)

- ✓ This update corrects a documentation error in the reserved bits of registers, which are not intended for customer use.

■ Details of the Fixes

- ✓ In 28.3 Register Descriptions, Table 28.4 Register Configuration (2/2):Correction of the initial value of the xSPI Common Status Register (COMSTT) (Offset Address: H'184).
  Before change: H'0000_0000
  After change: H'0033_0000

- ✓ In 28.3.3.2 xSPI Common Status Register (COMSTT):Correction of the initial values of the reserved bits of the xSPI Common Status Register (COMSTT)(Offset Address: H'184, bits 21, 20, 17, and 16).
  Before change: H'0000_0000
  After change: H'0033_0000

■ Affected Scope due to this Update

- ✓ This correction applies only to the UM description and has no impact.

Before

28.3 Register Descriptions

Table 28.4 Register Configuration (2/2)

Register Name	Abbreviation	R/W	Initial Value	Offset Address	Access Size
xSPI Command Manual Data 1 Buf 2	CDD1BUF2	R/W	H'0000_0000	H'0AC	32
xSPI Command Manual Data 1 Buf 3	CDD1BUF3	R/W	H'0000_0000	H'0BC	32
xSPI Link Pattern Control 0 register	LPCTL0	R/W	H'0000_0000	H'100	32
xSPI Link Pattern Control 1 register	LPCTL1	R/W	H'0000_0000	H'104	32
xSPI Link I/O Control register	LIOCTL	R/W	H'0003_0003	H'108	32
xSPI Command Calibration Control Register 0 CS0	CCCTL0CS0	R/W	H'1F00_0000	H'130	32
xSPI Command Calibration Control Register 0 CS1	CCCTL0CS1	R/W	H'1F00_0000	H'150	32
xSPI Command Calibration Control Register 1 CS0	CCCTL1CS0	R/W	H'0000_0000	H'134	32
xSPI Command Calibration Control Register 1 CS1	CCCTL1CS1	R/W	H'0000_0000	H'154	32
xSPI Command Calibration Control Register 2 CS0	CCCTL2CS0	R/W	H'0000_0000	H'138	32
xSPI Command Calibration Control Register 2 CS1	CCCTL2CS1	R/W	H'0000_0000	H'158	32
xSPI Command Calibration Control Register 3 CS0	CCCTL3CS0	R/W	H'0000_0000	H'13C	32
xSPI Command Calibration Control Register 3 CS1	CCCTL3CS1	R/W	H'0000_0000	H'15C	32
xSPI Command Calibration Control Register 4 CS0	CCCTL4CS0	R/W	H'0000_0000	H'140	32
xSPI Command Calibration Control Register 4 CS1	CCCTL4CS1	R/W	H'0000_0000	H'160	32
xSPI Command Calibration Control Register 5 CS0	CCCTL5CS0	R/W	H'0000_0000	H'144	32
xSPI Command Calibration Control Register 5 CS1	CCCTL5CS1	R/W	H'0000_0000	H'164	32
xSPI Command Calibration Control Register 6 CS0	CCCTL6CS0	R/W	H'0000_0000	H'148	32
xSPI Command Calibration Control Register 6 CS1	CCCTL6CS1	R/W	H'0000_0000	H'168	32
xSPI Command Calibration Control Register 7 CS0	CCCTL7CS0	R/W	H'0000_0000	H'14C	32
xSPI Command Calibration Control Register 7 CS1	CCCTL7CS1	R/W	H'0000_0000	H'16C	32
xSPI Version Register	VERSTT	R	H'0000_0000	H'180	32
xSPI Common Status Register	COMSTT	R	H'0000_0000	H'184	32
xSPI Calibration Status Register CS0	CASTTCS0	R	H'0000_0000	H'188	32
xSPI Calibration Status Register CS1	CASTTCS1	R	H'0000_0000	H'18C	32
xSPI Interrupt Status Register	INTS	R	H'0000_0000	H'190	32
xSPI Interrupt Clear Register	INTC	W	H'0000_0000	H'194	32
xSPI Interrupt Enable Register	INTE	R/W	H'0000_0000	H'198	32

After

28.3 Register Descriptions

Table 28.4 Register Configuration (2/2)

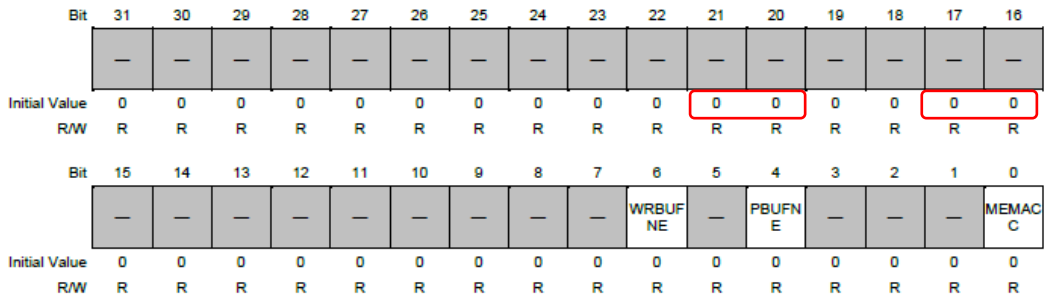
Register Name	Abbreviation	R/W	Initial Value	Offset Address	Access Size
xSPI Command Manual Data 1 Buf 2	CDD1BUF2	R/W	H'0000_0000	H'0AC	32
xSPI Command Manual Data 1 Buf 3	CDD1BUF3	R/W	H'0000_0000	H'0BC	32
xSPI Link Pattern Control 0 register	LPCTL0	R/W	H'0000_0000	H'100	32
xSPI Link Pattern Control 1 register	LPCTL1	R/W	H'0000_0000	H'104	32
xSPI Link I/O Control register	LIOCTL	R/W	H'0003_0003	H'108	32
xSPI Command Calibration Control Register 0 CS0	CCCTL0CS0	R/W	H'1F00_0000	H'130	32
xSPI Command Calibration Control Register 0 CS1	CCCTL0CS1	R/W	H'1F00_0000	H'150	32
xSPI Command Calibration Control Register 1 CS0	CCCTL1CS0	R/W	H'0000_0000	H'134	32
xSPI Command Calibration Control Register 1 CS1	CCCTL1CS1	R/W	H'0000_0000	H'154	32
xSPI Command Calibration Control Register 2 CS0	CCCTL2CS0	R/W	H'0000_0000	H'138	32
xSPI Command Calibration Control Register 2 CS1	CCCTL2CS1	R/W	H'0000_0000	H'158	32
xSPI Command Calibration Control Register 3 CS0	CCCTL3CS0	R/W	H'0000_0000	H'13C	32
xSPI Command Calibration Control Register 3 CS1	CCCTL3CS1	R/W	H'0000_0000	H'15C	32
xSPI Command Calibration Control Register 4 CS0	CCCTL4CS0	R/W	H'0000_0000	H'140	32
xSPI Command Calibration Control Register 4 CS1	CCCTL4CS1	R/W	H'0000_0000	H'160	32
xSPI Command Calibration Control Register 5 CS0	CCCTL5CS0	R/W	H'0000_0000	H'144	32
xSPI Command Calibration Control Register 5 CS1	CCCTL5CS1	R/W	H'0000_0000	H'164	32
xSPI Command Calibration Control Register 6 CS0	CCCTL6CS0	R/W	H'0000_0000	H'148	32
xSPI Command Calibration Control Register 6 CS1	CCCTL6CS1	R/W	H'0000_0000	H'168	32
xSPI Command Calibration Control Register 7 CS0	CCCTL7CS0	R/W	H'0000_0000	H'14C	32
xSPI Command Calibration Control Register 7 CS1	CCCTL7CS1	R/W	H'0000_0000	H'16C	32
xSPI Version Register	VERSTT	R	H'0000_0000	H'180	32
xSPI Common Status Register	COMSTT	R	H'0033_0000	H'184	32
xSPI Calibration Status Register CS0	CASTTCS0	R	H'0000_0000	H'188	32
xSPI Calibration Status Register CS1	CASTTCS1	R	H'0000_0000	H'18C	32
xSPI Interrupt Status Register	INTS	R	H'0000_0000	H'190	32
xSPI Interrupt Clear Register	INTC	W	H'0000_0000	H'194	32
xSPI Interrupt Enable Register	INTE	R/W	H'0000_0000	H'198	32

Modified

Before

28.3.3.2 xSPI Common Status Register (COMSTT)

This register indicates the status of xSPI Master.

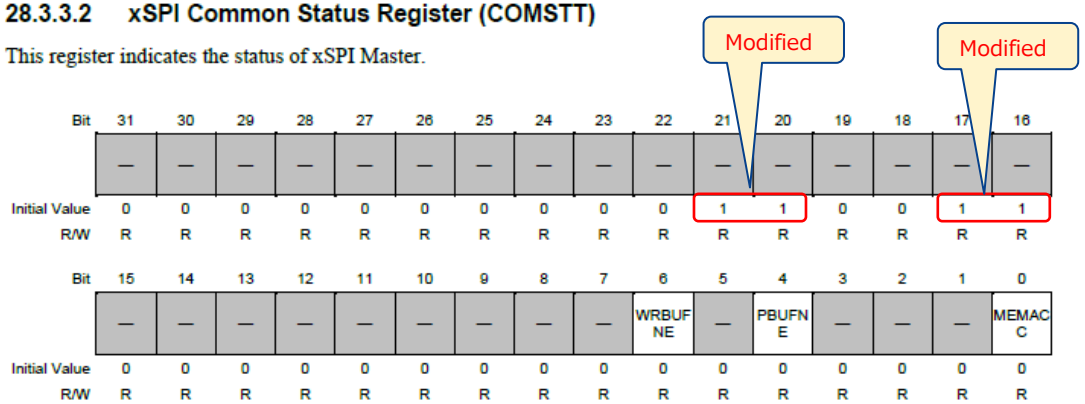


Bit	Bit Name	Initial Value	R/W	Description
31 to 7	—	All 0	R	Reserved When read, the initial value is read. When writing, be sure to write the initial value. Operation is not guaranteed if a value other than the initial value is written.
6	WRBUFNE	0b	R	Write Buffer Not Empty 0: Empty 1: Not empty
5	—	0b	R	Reserved This bit is read as 0.
4	PBUFNE	0b	R	Prefetch Buffer Not Empty 0: Empty 1: Not empty
3 to 1	—	000b	R	Reserved These bits are read as 0.
0	MEMACC	0b	R	Memory access ongoing 0: System bus channel is not accessing to memory. 1: System bus channel is accessing to memory.

After

28.3.3.2 xSPI Common Status Register (COMSTT)

This register indicates the status of xSPI Master.



Bit	Bit Name	Initial Value	R/W	Description
31 to 7	—	H'6600	R	Reserved When read, the initial value is read. When writing, be sure to write the initial value. Operation is not guaranteed if a value other than the initial value is written.
6	WRBUFNE	0b	R	Write Buffer Not Empty 0: Empty 1: Not empty
5	—	0b	R	Reserved This bit is read as 0.
4	PBUFNE	0b	R	Prefetch Buffer Not Empty 0: Empty 1: Not empty
3 to 1	—	000b	R	Reserved These bits are read as 0.
0	MEMACC	0b	R	Memory access ongoing 0: System bus channel is not accessing to memory. 1: System bus channel is accessing to memory.

Modified

Chapter 32B. USB2.0 Function - PHY Function Control Register

■ Update Background

- ✓ Correction of a documentation error related to the initial value of the PHY Function Control Register in the USB2.0 Function.

■ Impact on Customers(Details of the Issues or Issues Addressed)

- ✓ This update corrects a documentation error in the reserved bits of registers, which are not intended for customer use.

■ Details of the Fixes

- ✓ In 32B.2.20 USB2.0_Func PHY Function Control Register(Offset Address: H'104), the incorrect initial value description was corrected.

■ Affected Scope due to this Update

- ✓ This correction applies only to the UM description (initial value) and has no impact on product specifications.

Before

32B.2.20.1 PHY Function Control Register [PHYFUNCTR] <Address: H'104>

Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
	—	SusMon	—	—	—	—	—	—	—	—	—	—	—	—	—	—
Initial Value	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—
R/W	R	R	R	R	R	R	R	R	R	R	R	R	R	R	R	R

Bit	Bit Name	Initial Value	R/W	Description
15	—	0	R	Nothing is assigned to this bit. Fix this bit to 0.
14	SusMon	0	R	This bit allows reading of the status of the Suspend M signal.
13 to 0	—	All 0	R	Nothing is assigned to these bits. Fix these bits to 0.

After

32B.2.20.1 PHY Function Control Register [PHYFUNCTR] <Address: H'104>

Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
	—	SusMon	—	—	—	—	—	—	—	—	—	—	—	—	—	—
Initial Value	0	0	0	0	0	0	0	1	0	0	0	0	0	0	0	0
	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—
R/W	R	R	R	R	R	R	R	R	R	R	R	R	R	R	R	R

Modified

Bit	Bit Name	Initial Value	R/W	Description
15	—	0	R	Nothing is assigned to this bit. Fix this bit to 0.
14	SusMon	0	R	This bit allows reading of the status of the Suspend M signal.
13	—	0	R	Nothing is assigned to this bit. Fix this bit to 0.
12 to 8	—	H'01	R	Nothing is assigned to these bits. The read value is unknown.
7 to 0	—	All 0	R	Nothing is assigned to these bits. Fix these bits to 0.

Modified

Chapter 39. ADC - A/D Converter Mode Register 1(ADM1)

■ Update Background

- ✓ Improvement of clarity in the description of trigger settings for A/D Converter Mode Register 1 (ADM1).
- ✓ Correction of a documentation error related to the register access attribute.

■ Impact on Customers(Details of the Issues or Issues Addressed)

- ✓ This update corrects a documentation error related to register attributes(Read only → Read/Write).
- ✓ Also, this update adds supplementary notes on Software triggers, Hardware triggers, and various edge settings to improve the readability and ease of configuration of the UM.

■ Details of the Fixes

- ✓ In 39.3.2 A/D Converter Mode Register 1 (ADM1) (Offset Address: H'4), the following corrections were made:
  - ✓ The description of trigger settings in Table 39.4 TRGEN[5:0] Bits and Trigger Source was reorganized to improve readability and understanding of the trigger configuration.
  - ✓ Correction of the register access attribute from R to RW.

■

Affected Scope due to this Update

- ✓ This correction applies only to the UM description and has no impact on product specifications.

Before

39.3.2 A/D Converter Mode Register 1 (ADM1)

The ADM1 is a 32-bit register that controls A/D conversion and sets the mode for a hardware trigger. This register can be read from and written to in 32-bit units.

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
	—	—	—	—	—	—	—	—	—	—	TRGEN5	TRGEN4	TRGEN3	TRGEN2	TRGEN1	TRGEN0
Initial Value	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
R/W	R	R	R	R	R	R	R	R	R	R	R	R	R	R	R	R

Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
	—	—	EGA1	EGA0	—	—	—	—	—	—	—	BS	RPS	MS	TRGIN	TRG
Initial Value	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
R/W	R	R	R/W	R/W	R	R	R	R	R	R	R	R/W	R/W	R/W	R/W	R/W

After

39.3.2 A/D Converter Mode Register 1 (ADM1)

The ADM1 is a 32-bit register that controls A/D conversion and sets the mode for a hardware trigger. This register can be read from and written to in 32-bit units.

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
	—	—	—	—	—	—	—	—	—	—	TRGEN5	TRGEN4	TRGEN3	TRGEN2	TRGEN1	TRGEN0
Initial Value	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
R/W	R	R	R	R	R	R	R	R	R	R	R/W	R/W	R/W	R/W	R/W	R/W

Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
	—	—	EGA1	EGA0	—	—	—	—	—	—	—	BS	RPS	MS	TRGIN	TRG
Initial Value	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
R/W	R	R	R/W	R/W	R	R	R	R	R	R	R	R/W	R/W	R/W	R/W	R/W

Modified

Before

39.3.2 A/D Converter Mode Register 1 (ADM1)

Table 39.4 TRGEN[5:0] Bits and Trigger Source

Module	Source	Description	TRGEN[5:0] Bits					
			5	4	3	2	1	0
External pin	ADC_TRG	External trigger input	0	0	0	0	0	0
MTU	TRGA0N	Compare match with or input capture to MTU0.TGRA	0	0	0	0	0	1
	TRGA1N	Compare match with or input capture to MTU1.TGRA	0	0	0	0	1	0
	TRGA2N	Compare match with or input capture to MTU2.TGRA	0	0	0	0	1	1
	TRGA3N	Compare match with or input capture to MTU3.TGRA	0	0	0	1	0	0
	TRGA4N	Compare match with or input capture to MTU4.TGRA or underflow (trough) of MTU4.TCNT in complementary PWM mode	0	0	0	1	0	1
	TRGA6N	Compare match with or input capture to MTU6.TGRA	0	0	0	1	1	0
	TRGA7N	Compare match with or input capture to MTU7.TGRA or underflow (trough) of MTU7.TCNT in complementary PWM mode	0	0	0	1	1	1
	TRG0N	Compare match with MTU0.TGRE	0	0	1	0	0	0
	TRG4AN	Compare match between MTU4.TADCORA and MTU4.TCNT	0	0	1	0	0	1
	TRG4BN	Compare match between MTU4.TADCORB and MTU4.TCNT	0	0	1	0	1	0
	TRG4AN or TRG4BN	Compare match between MTU4.TADCORA and MTU4.TCNT or compare match between MTU4.TADCORB and MTU4.TCNT	0	0	1	0	1	1
	TRG4ABN	Compare match between MTU4.TADCORA and MTU4.TCNT and compare match between MTU4.TADCORB and MTU4.TCNT (when interrupt skipping function 2 is used)	0	0	1	1	0	0
	TRG7AN	Compare match between MTU7.TADCORA and MTU7.TCNT	0	0	1	1	0	1
	TRG7BN	Compare match between MTU7.TADCORB and MTU7.TCNT	0	0	1	1	1	0
	TRG7AN or TRG7BN	Compare match between MTU7.TADCORA and MTU7.TCNT or compare match between MTU7.TADCORB and MTU7.TCNT	0	0	1	1	1	1
	TRG7ABN	Compare match between MTU7.TADCORA and MTU7.TCNT and compare match between MTU7.TADCORB and MTU7.TCNT (when interrupt skipping function 2 is used)	0	1	0	0	0	0
GPT	ADTRGA0	Compare match with GPT0.GTADTRA	0	1	0	0	0	1
	ADTRGB0	Compare match with GPT0.GTADTRB	0	1	0	0	1	0
	ADTRGA1	Compare match with GPT1.GTADTRA	0	1	0	0	1	1
	ADTRGB1	Compare match with GPT1.GTADTRB	0	1	0	1	0	0
	ADTRGA2	Compare match with GPT2.GTADTRA	0	1	0	1	0	1
	ADTRGB2	Compare match with GPT2.GTADTRB	0	1	0	1	1	0
	ADTRGA3	Compare match with GPT3.GTADTRA	0	1	0	1	1	1
	ADTRGB3	Compare match with GPT3.GTADTRB	0	1	1	0	0	0
	ADTRGA0 or ADTRGB0	Compare match with GPT0.GTADTRA or GPT0.GTADTRB	0	1	1	0	0	1
	ADTRGA1 or ADTRGB1	Compare match with GPT1.GTADTRA or GPT1.GTADTRB	0	1	1	0	1	0
	ADTRGA2 or ADTRGB2	Compare match with GPT2.GTADTRA or GPT2.GTADTRB	0	1	1	0	1	1
	ADTRGA3 or ADTRGB3	Compare match with GPT3.GTADTRA or GPT3.GTADTRB	0	1	1	1	0	0

After

39.3.2 A/D Converter Mode Register 1 (ADM1)

Added

Added

Table 39.4 TRGEN[5:0] Bits and Trigger Source (1/2)

Trigger Mode	Module	Source	Description	TRG Bit	TRGEN[5:0] Bits						EGA[1:0] Bits	
					5	4	3	2	1	0	1	0
Software trigger mode				0	—	—	—	—	—	—	—	—
Hardware trigger mode	External pin	ADC_TRG	External trigger input	1	0	0	0	0	0	0	0	1
											1	0
											1	1
	MTU	TRGA0N	Compare match with or input capture to MTU0.TGRA		0	0	0	0	0	1	01 or 10 or 11	
		TRGA1N	Compare match with or input capture to MTU1.TGRA		0	0	0	0	1	0		
		TRGA2N	Compare match with or input capture to MTU2.TGRA		0	0	0	0	1	1		
		TRGA3N	Compare match with or input capture to MTU3.TGRA		0	0	0	1	0	0		
		TRGA4N	Compare match with or input capture to MTU4.TGRA or underflow (trough) of MTU4.TCNT in complementary PWM mode		0	0	0	1	0	1		
		TRGA6N	Compare match with or input capture to MTU6.TGRA		0	0	0	1	1	0		
		TRGA7N	Compare match with or input capture to MTU7.TGRA or underflow (trough) of MTU7.TCNT in complementary PWM mode		0	0	0	1	1	1		
		TRG0N	Compare match with MTU0.TGRE		0	0	1	0	0	0		
		TRG4AN	Compare match between MTU4.TADCORA and MTU4.TCNT		0	0	1	0	0	1		
		TRG4BN	Compare match between MTU4.TADCORB and MTU4.TCNT		0	0	1	0	1	0		
		TRG4AN or TRG4BN	Compare match between MTU4.TADCORA and MTU4.TCNT or compare match between MTU4.TADCORB and MTU4.TCNT		0	0	1	0	1	1		
		TRG4ABN	Compare match between MTU4.TADCORA and MTU4.TCNT and compare match between MTU4.TADCORB and MTU4.TCNT (when interrupt skipping function 2 is used)		0	0	1	1	0	0		
		TRG7AN	Compare match between MTU7.TADCORA and MTU7.TCNT		0	0	1	1	0	1		
		TRG7BN	Compare match between MTU7.TADCORB and MTU7.TCNT		0	0	1	1	1	0		
		TRG7AN or TRG7BN	Compare match between MTU7.TADCORA and MTU7.TCNT or compare match between MTU7.TADCORB and MTU7.TCNT		0	0	1	1	1	1		

Added

Added

Table 39.4 TRGEN[5:0] Bits and Trigger Source (2/2)

Trigger Mode	Module	Source	Description	TRG Bit	TRGEN[5:0] Bits						EGA[1:0] Bits	
					5	4	3	2	1	0	1	0
Hardware trigger mode	MTU	TRG7ABN	Compare match between MTU7.TADCORA and MTU7.TCNT and compare match between MTU7.TADCORB and MTU7.TCNT (when interrupt skipping function 2 is used)		0	1	0	0	0	0	01 or 10 or 11	
	GPT	ADTRGA0	Compare match with GPT0.GTADTRA		0	1	0	0	0	1		
		ADTRGB0	Compare match with GPT0.GTADTRB		0	1	0	0	1	0		
		ADTRGA1	Compare match with GPT1.GTADTRA		0	1	0	0	1	1		
		ADTRGB1	Compare match with GPT1.GTADTRB		0	1	0	1	0	0		
		ADTRGA2	Compare match with GPT2.GTADTRA		0	1	0	1	0	1		
		ADTRGB2	Compare match with GPT2.GTADTRB		0	1	0	1	1	0		
		ADTRGA3	Compare match with GPT3.GTADTRA		0	1	0	1	1	1		
		ADTRGB3	Compare match with GPT3.GTADTRB		0	1	1	0	0	0		
		ADTRGA0 or ADTRGB0	Compare match with GPT0.GTADTRA or GPT0.GTADTRB		0	1	1	0	0	1		
		ADTRGA1 or ADTRGB1	Compare match with GPT1.GTADTRA or GPT1.GTADTRB		0	1	1	0	1	0		
		ADTRGA2 or ADTRGB2	Compare match with GPT2.GTADTRA or GPT2.GTADTRB		0	1	1	0	1	1		
		ADTRGA3 or ADTRGB3	Compare match with GPT3.GTADTRA or GPT3.GTADTRB		0	1	1	1	0	0		

Chapter 22. Realtime Clock(RTC) - RTC Time Capture

■ Update Background
- ✓ Documentation correction to complete the RTC time capture configuration description.
- ✓ The previous UM description was incomplete, as it did not include the control register to enable the existing RTC time capture function.

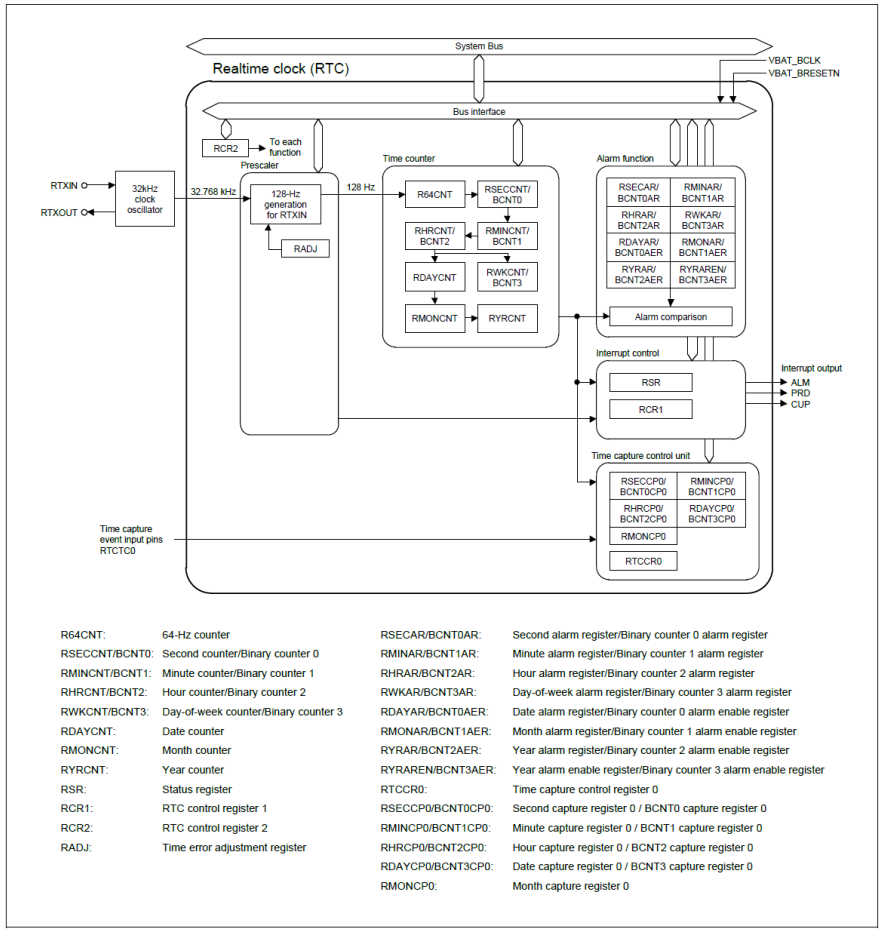
■ Impact on Customers (Details of the Issues or Issues Addressed)
- ✓ The RTC Timing Capture function may not operate correctly. An explanation of the register settings required for the time capture operation has been added to provide the necessary information for correct operation.
- ✓ There is no impact if the Timing Capture function is not used.

■ Details of the Fixes
- ✓ Clarified the RTC time capture configuration, including the required control registers and their operation, with the addition of the RCR3 register.
  - ✓ Added RCR3 to Figure 22.1 (RTC Block Diagram).
  - ✓ Added RCR3 to Table 22.3 (RTC Control Register List).
  - ✓ Added a new register description for RCR3 in section 22.3 (Register Description), with subsequent section numbers updated accordingly.
  - ✓ Updated Figure 22.3 (Clock and Count Mode Setting Procedure) to include configuration of the RCR3 register.
  - ✓ Added input external clock case to Figure 22.3 (Clock and Count Mode Setting Procedure) for clarification.
  - ✓ Updated the description of the RTCCR0.TCEN bit to clarify that RCR3 resister must also be set when using the RTC time capture function.

■ Affected Scope due to this Update
- ✓ For configurations where the Timing Capture function is used, a software update is typically required to add the RCR3 register configuration.
- ✓ There is no impact if the Timing Capture function is not used.

22.1.2 Block diagram

Figure 22.1 shows a block diagram of the RTC.

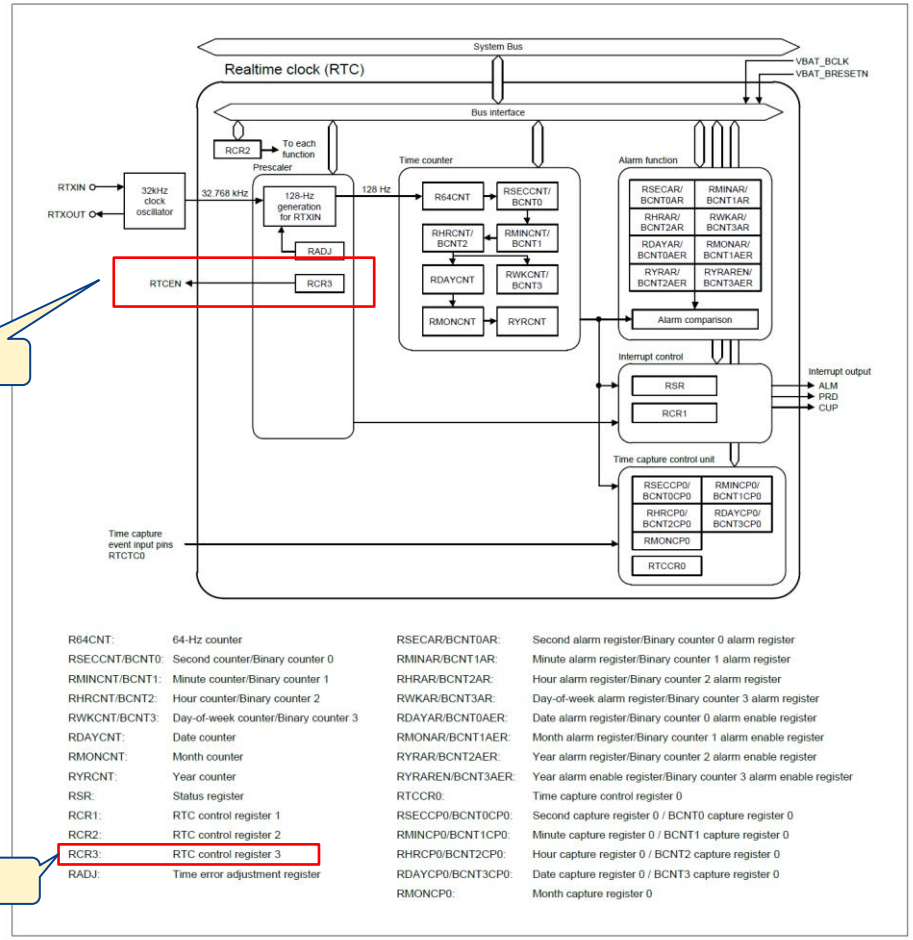


R64CNT:	64-Hz counter	RSECAR/BCNT0AR:	Second alarm register/Binary counter 0 alarm register
RSECCNT/BCNT0:	Second counter/Binary counter 0	RMINAR/BCNT1AR:	Minute alarm register/Binary counter 1 alarm register
RMINCNT/BCNT1:	Minute counter/Binary counter 1	RHRAR/BCNT2AR:	Hour alarm register/Binary counter 2 alarm register
RHRCNT/BCNT2:	Hour counter/Binary counter 2	RWKAR/BCNT3AR:	Day-of-week alarm register/Binary counter 3 alarm register
RWKCNT/BCNT3:	Day-of-week counter/Binary counter 3	RDAYAR/BCNT0AER:	Date alarm register/Binary counter 0 alarm enable register
RDAYCNT:	Date counter	RMONAR/BCNT1AER:	Month alarm register/Binary counter 1 alarm enable register
RMONCNT:	Month counter	RYRAR/BCNT2AER:	Year alarm register/Binary counter 2 alarm enable register
RYRCNT:	Year counter	RYRAREN/BCNT3AER:	Year alarm enable register/Binary counter 3 alarm enable register
RSR:	Status register	RTCCR0:	Time capture control register 0
RCR1:	RTC control register 1	RSECCP0/BCNT0CP0:	Second capture register 0 / BCNT0 capture register 0
RCR2:	RTC control register 2	RMINCP0/BCNT1CP0:	Minute capture register 0 / BCNT1 capture register 0
RADJ:	Time error adjustment register	RHRCP0/BCNT2CP0:	Hour capture register 0 / BCNT2 capture register 0
		RDAYCP0/BCNT3CP0:	Date capture register 0 / BCNT3 capture register 0
		RMONCP0:	Month capture register 0

Figure 22.1 Block Diagram of RTC

22.1.2 Block diagram

Figure 22.1 shows a block diagram of the RTC.



R64CNT:	64-Hz counter	RSECAR/BCNT0AR:	Second alarm register/Binary counter 0 alarm register
RSECCNT/BCNT0:	Second counter/Binary counter 0	RMINAR/BCNT1AR:	Minute alarm register/Binary counter 1 alarm register
RMINCNT/BCNT1:	Minute counter/Binary counter 1	RHRAR/BCNT2AR:	Hour alarm register/Binary counter 2 alarm register
RHRCNT/BCNT2:	Hour counter/Binary counter 2	RWKAR/BCNT3AR:	Day-of-week alarm register/Binary counter 3 alarm register
RWKCNT/BCNT3:	Day-of-week counter/Binary counter 3	RDAYAR/BCNT0AER:	Date alarm register/Binary counter 0 alarm enable register
RDAYCNT:	Date counter	RMONAR/BCNT1AER:	Month alarm register/Binary counter 1 alarm enable register
RMONCNT:	Month counter	RYRAR/BCNT2AER:	Year alarm register/Binary counter 2 alarm enable register
RYRCNT:	Year counter	RYRAREN/BCNT3AER:	Year alarm enable register/Binary counter 3 alarm enable register
RSR:	Status register	RTCCR0:	Time capture control register 0
RCR1:	RTC control register 1	RSECCP0/BCNT0CP0:	Second capture register 0 / BCNT0 capture register 0
RCR2:	RTC control register 2	RMINCP0/BCNT1CP0:	Minute capture register 0 / BCNT1 capture register 0
RCR3:	RTC control register 3	RHRCP0/BCNT2CP0:	Hour capture register 0 / BCNT2 capture register 0
RADJ:	Time error adjustment register	RDAYCP0/BCNT3CP0:	Date capture register 0 / BCNT3 capture register 0
		RMONCP0:	Month capture register 0

Figure 22.1 Block Diagram of RTC

Before

22.2 Register Configuration

Table 22.3 RTC Control Register List (1/2)

Register Name	Abbreviation	R/W	Initial Value	Address	Access Size
64-Hz Counter	R64CNT	R	H'xx	H'00	8
Second Counter/Binary Counter 0	RSECCNT/ BCNT0	R/W	H'xx	H'02	8
Minute Counter/Binary Counter 1	RMINCNT/ BCNT1	R/W	H'xx	H'04	8
Hour Counter/Binary Counter 2	RHRCNT/ BCNT2	R/W	H'xx	H'06	8
Day-of-Week Counter/Binary Counter 3	RWKCNT/ BCNT3	R/W	H'xx	H'08	8
Date Counter	RDAYCNT	R/W	H'xx	H'0A	8
Month Counter	RMONCNT	R/W	H'xx	H'0C	8
Year Counter	RYRCNT	R/W	H'00xx	H'0E	16
Second Alarm Register/ Binary Counter 0 Alarm Register	RSECAR/ BCNT0AR	R/W	H'xx	H'10	8
Minute Alarm Register/ Binary Counter 1 Alarm Register	RMINAR/ BCNT1AR	R/W	H'xx	H'12	8
Hour Alarm Register/ Binary Counter 2 Alarm Register	RHRAR/ BCNT2AR	R/W	H'xx	H'14	8
Day-of-Week Alarm Register/ Binary Counter 3 Alarm Register	RWKAR/ BCNT3AR	R/W	H'xx	H'16	8
Date Alarm Register/ Binary Counter 0 Alarm Enable Register	RDAYAR/ BCNT0AER	R/W	H'xx	H'18	8
Month Alarm Register/ Binary Counter 1 Alarm Enable Register	RMONAR/ BCNT1AER	R/W	H'xx	H'1A	8
Year Alarm Register/ Binary Counter 2 Alarm Enable Register	RYRAR/ BCNT2AER	R/W	H'00xx	H'1C	16
Year Alarm Enable Register/ Binary Counter 3 Alarm Enable Register	RYRAREN/ BCNT3AER	R/W	H'xx	H'1E	8
RTC Status Register	RSR	R/W	H'00*1*2	H'20	8
RTC Control Register 1	RCR1	R/W	H'xx*2	H'22	8
RTC Control Register 2	RCR2	R/W	H'xx*2	H'24	8
Time Error Adjustment Register	RADJ	R/W	H'xx	H'2E	8
Time Capture Control Register 0	RTCCR0	R/W	H'xx	H'40	8
Second Capture Register 0/ BCNT0 Capture Register 0	RSECCP0/ BCNT0CP0	R	H'xx	H'52	8

After

22.2 Register Configuration

Table 22.3 RTC Control Register List (1/2)

Register Name	Abbreviation	R/W	Initial Value	Address	Access Size
64-Hz Counter	R64CNT	R	H'xx	H'00	8
Second Counter/Binary Counter 0	RSECCNT/ BCNT0	R/W	H'xx	H'02	8
Minute Counter/Binary Counter 1	RMINCNT/ BCNT1	R/W	H'xx	H'04	8
Hour Counter/Binary Counter 2	RHRCNT/ BCNT2	R/W	H'xx	H'06	8
Day-of-Week Counter/Binary Counter 3	RWKCNT/ BCNT3	R/W	H'xx	H'08	8
Date Counter	RDAYCNT	R/W	H'xx	H'0A	8
Month Counter	RMONCNT	R/W	H'xx	H'0C	8
Year Counter	RYRCNT	R/W	H'00xx	H'0E	16
Second Alarm Register/ Binary Counter 0 Alarm Register	RSECAR/ BCNT0AR	R/W	H'xx	H'10	8
Minute Alarm Register/ Binary Counter 1 Alarm Register	RMINAR/ BCNT1AR	R/W	H'xx	H'12	8
Hour Alarm Register/ Binary Counter 2 Alarm Register	RHRAR/ BCNT2AR	R/W	H'xx	H'14	8
Day-of-Week Alarm Register/ Binary Counter 3 Alarm Register	RWKAR/ BCNT3AR	R/W	H'xx	H'16	8
Date Alarm Register/ Binary Counter 0 Alarm Enable Register	RDAYAR/ BCNT0AER	R/W	H'xx	H'18	8
Month Alarm Register/ Binary Counter 1 Alarm Enable Register	RMONAR/ BCNT1AER	R/W	H'xx	H'1A	8
Year Alarm Register/ Binary Counter 2 Alarm Enable Register	RYRAR/ BCNT2AER	R/W	H'00xx	H'1C	16
Year Alarm Enable Register/ Binary Counter 3 Alarm Enable Register	RYRAREN/ BCNT3AER	R/W	H'xx	H'1E	8
RTC Status Register	RSR	R/W	H'00*1*2	H'20	8
RTC Control Register 1	RCR1	R/W	H'xx*2	H'22	8
RTC Control Register 2	RCR2	R/W	H'xx*2	H'24	8
RTC Control Register 3	RCR3	R/W	H'xx	H'26	8
Time Error Adjustment Register	RADJ	R/W	H'xx	H'2E	8
Time Capture Control Register 0	RTCCR0	R/W	H'xx	H'40	8

Added

Before

None

After

Added

22.3.20 RTC Control Register 3 (RCR3)

Bit	7	6	5	4	3	2	1	0
	—	—	—	—	—	—	—	RTCEN
Initial Value	x	x	x	x	x	x	x	x
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W

x: Undefined

Bit	Bit Name	Initial Value	R/W	Description
0	RTCEN	x	R/W	This bit enables or disables RTC time capture function 0: RTC time capure function is disabled. 1: RTC time capure function is enabled. *Note*: Both the RCR3.RTCEN bit and the RTCCR0.TCEN bit must be set to 1 when using the RTC time capture function.
7 to 1	—	—	R/W	Reserved This bit is read as 0. The write value should be 0.

22.3.21 Time Capture Control Register (RTCCR0)

Bit	Bit Name	Initial Value	R/W	Description
7	TCEN	x	R/W	Time Capture Event Input Pin Enable This bit enables or disables the time capture event input pin (RTCTC0). To enable the time capture event input pin, set also the TAMPICR1.CH0EN bit*2 to 1. If the TCEN bit is set to 0, set also the TCCT[1:0] bits to 00b. 0: The RTCTC0 pin is disabled as the time capture event input. 1: The RTCTC0 pin is enabled as the time capture event input.

22.3.22 Time Capture Control Register (RTCCR0)

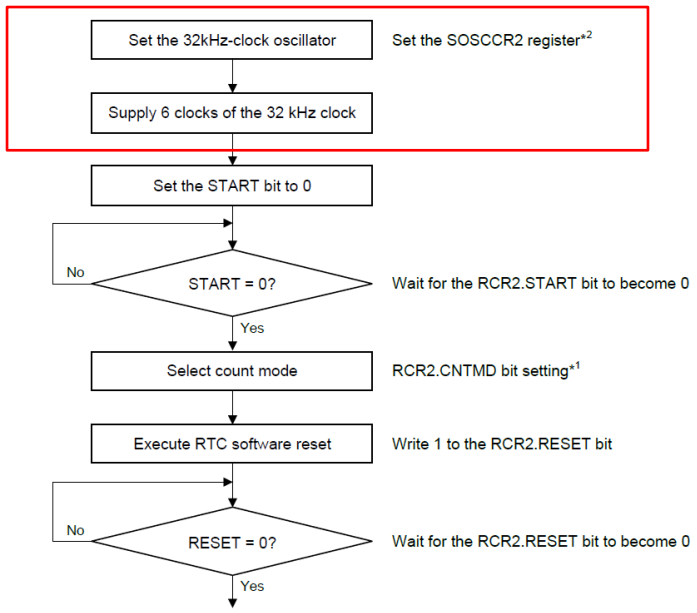
Bit	Bit Name	Initial Value	R/W	Description
7	TCEN	x	R/W	Time Capture Event Input Pin Enable This bit enables or disables the time capture event input pin (RTCTC0). To enable the time capture event input pin, set also the TAMPICR1.CH0EN bit*2 and RCR3.RTCEN bit to 1. If the TCEN bit is set to 0, set also the TCCT[1:0] bits to 00b. 0: The RTCTC0 pin is disabled as the time capture event input. 1: The RTCTC0 pin is enabled as the time capture event input.

Added

Before

22.4.2 Clock and Count Mode Setting Procedure

Figure 22.3 shows how to set the clock and the count mode.



Note 1. This step is not necessary if the count mode has been set concurrently with setting the START bit to 0. A value corresponding to the count mode setting must be written to the RCR2.CNTMD bit.

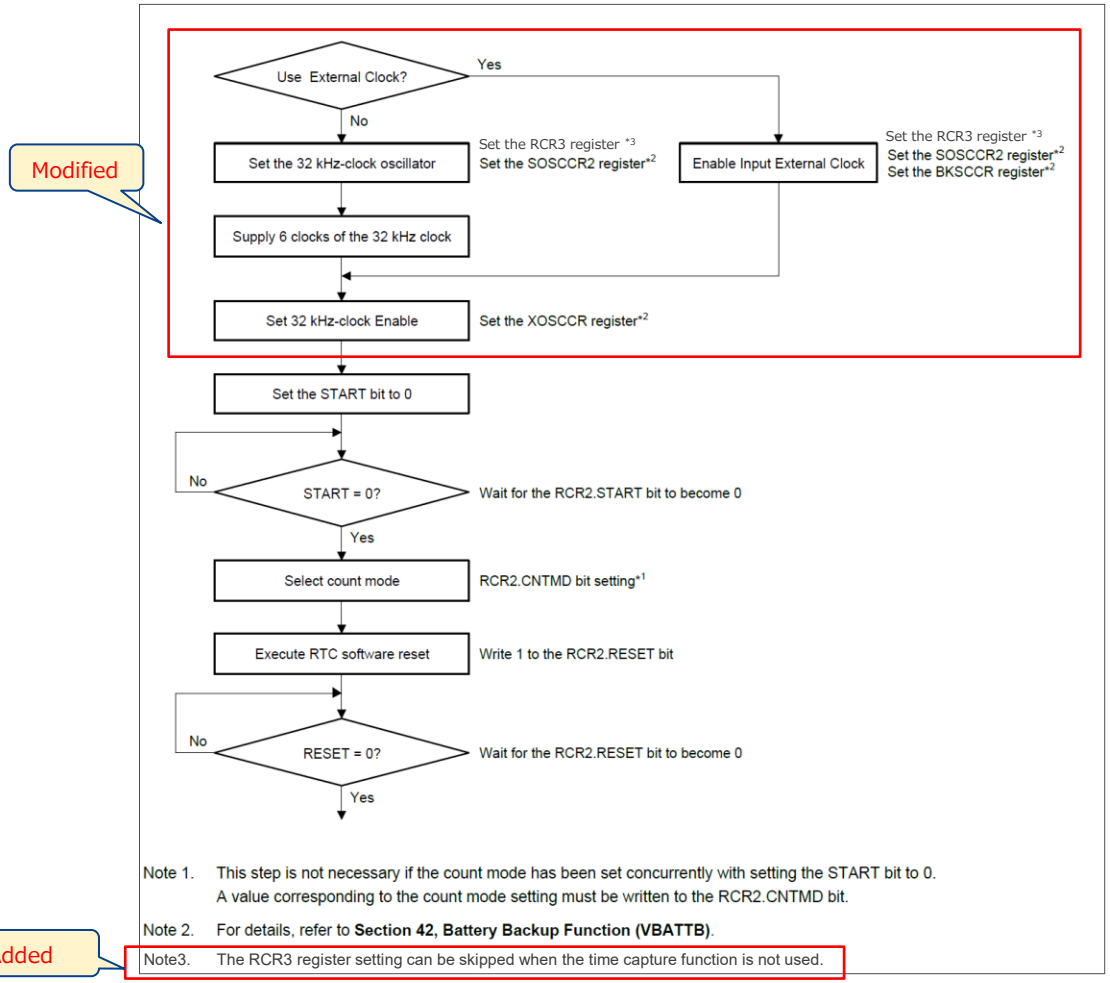
Note 2. For details, refer to **Section 42, Battery Backup Function (VBATTB)**.

Figure 22.3 Clock and Count Mode Setting Procedure

After

22.4.2 Clock and Count Mode Setting Procedure

Figure 22.3 shows how to set the clock and the count mode.



Note 1. This step is not necessary if the count mode has been set concurrently with setting the START bit to 0. A value corresponding to the count mode setting must be written to the RCR2.CNTMD bit.

Note 2. For details, refer to **Section 42, Battery Backup Function (VBATTB)**.

Added

Note3. The RCR3 register setting can be skipped when the time capture function is not used.

Figure 22.3 Clock and Count Mode Setting Procedure

Chapter 42. VBATTB – RTC Time Capture

■ Update Background
- ✓ Additional update associated with RTC.

■ Impact on Customers (Details of the Issues or Issues Addressed)
- ✓ Please refer to RTC for details.

■ Details of the Fixes
- ✓ Added the RCR3 register within the RTC in Figure 42.1 Block Diagram of VBATTB.

■ Affected Scope due to this Update
- ✓ Please refer to RTC for details.

Before

42.1 Overview

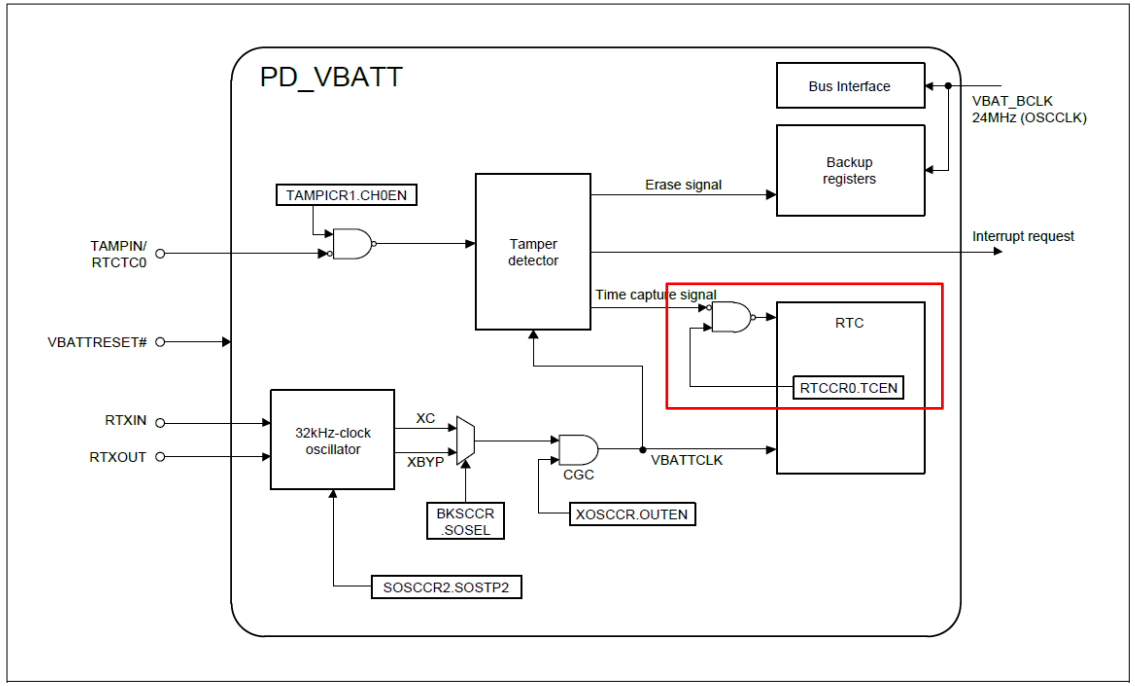


Figure 42.1 Block Diagram of VBATTB

After

42.1 Overview

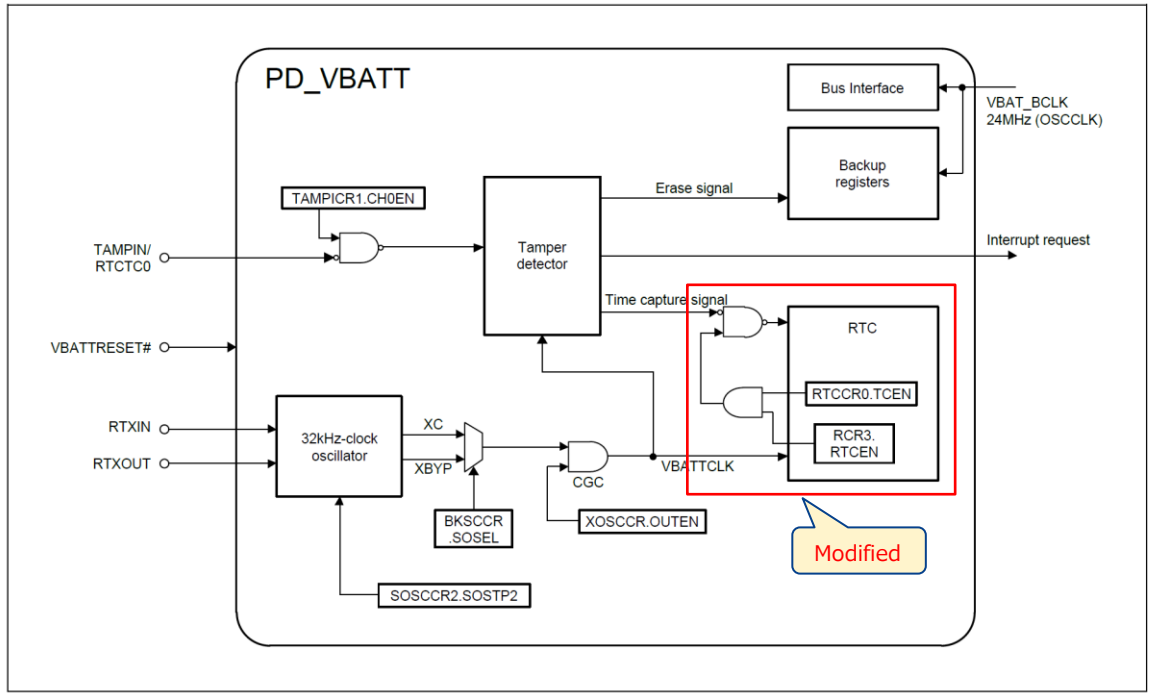


Figure 42.1 Block Diagram of VBATTB

MODIFICATION FOR CALCULATION EQUATIONS

Chapter 18. GPT – Automatic Dead time Setting correction

■ Update Background
- ✓ Documentation correction of the waveform transition conditions for the Automatic Dead Time Setting Function of GPT.

■ Impact on Customers (Details of the Issues or Issues Addressed)
- ✓ This issue affects only cases where the automatic dead-time insertion function is enabled and a dead-time error (DTEF) occurs.
- ✓ Because the dead-time error threshold formula described in the UM is incorrect.
  The Hardware implementation is correct and operates as specified.
- ✓ If the calculation formula in the User Manual is referenced, the estimated error occurrence conditions and timing may not match the actual hardware behavior.

■ Details of the Fixes
- ✓ In 18.3.4 Automatic Dead Time Setting Function, table 18.6: “Correction of waveform transition point at dead time error occurrence”, the documented dead time conditions for saw-wave one-shot pulse mode were corrected as follows.
  - ✓ Before (incorrect):
    - ✓ *GTCCRA - GTDVD > GTPR*
    - ✓ *GTCCRA - GTDVU > GTPR*
  - ✓ After (correct):
    - ✓ *GTCCRA + GTDVD > GTPR*
    - ✓ *GTCCRA + GTDVU > GTPR*

■ Affected Scope due to this Update
- ✓ No Impact on Existing and Mass-Produced Products

Before

18.3.4 Automatic Dead Time Setting Function

Table 18.6 Correction of waveform transition point at dead time error occurrence

Wave mode	Count direction	Interval	Dead time error condition	Positive-Phase waveform transition point with corrected	Negative-phase waveform transition point with corrected
saw-wave one-shot pulse mode	Up counting	first half	GTCCRA-GTDVU < 0	GTDVU	0
		second half	GTCCRA-GTDVD > GTPR	GTPR-GTDVD	GTPR
	Down counting	first half	GTCCRA-GTDVU > GTPR	GTPR-GTDVU	GTPR
		second half	GTCCRA-GTDVD < 0	GTDVD	0
triangle PWM mode 1/2/3	Up counting	(first half)	GTCCRA-GTDVU ≤ 0	GTDVU+1	1
	Down counting	(second half)	GTCCRA-GTDVD < 0	GTDVD	0

After

18.3.4 Automatic Dead Time Setting Function

Table 18.6 Correction of waveform transition point at dead time error occurrence

Wave mode	Count direction	Interval	Dead time error condition	Positive-Phase waveform transition point with corrected	Negative-phase waveform transition point with corrected
saw-wave one-shot pulse mode	Up counting	first half	GTCCRA-GTDVU < 0	GTDVU	0
		second half	GTCCRA+GTDVD > GTPR	GTPR-GTDVD	GTPR
	Down counting	first half	GTCCRA+GTDVU > GTPR	GTPR-GTDVU	GTPR
		second half	GTCCRA-GTDVD < 0	GTDVD	0
triangle PWM mode 1/2/3	Up counting	(first half)	GTCCRA-GTDVU ≤ 0	GTDVU+1	1
	Down counting	(second half)	GTCCRA-GTDVD < 0	GTDVD	0

Modified

Chapter 39. ADC - ADCR calculation formula

■ Update Background

- ✓ Correction of a documentation error in the calculation formula for the A/D Converter conversion result registers.
- ✓ Among multiple calculation formulas described in the UM, one formula was incorrect and has been corrected.

■ Impact on Customers(Details of the Issues or Issues Addressed)

- ✓ This update corrects calculation formula, the A/D conversion result may lead to unintended interpretation.
- ✓ When the correct calculation formula is used, the correct conversion result can be obtained.

■ Details of the Fixes

- ✓ In 39.3.9 A/D Conversion Result Registers (ADCR11 to ADCR0)(Offset Address: H'30 to H'5C), the calculation formula for the A/D conversion result was revised.

$$ADCR = INT\left[\frac{Vin}{ADC\_AVREF} \times 2^d \times 0.5\right]$$

or

$$(ADCR - 0.5) \times \frac{ADC\_AVREF}{2^d} \leq Vin < (ADCR + 0.5) \times \frac{ADC\_AVREF}{2^d}$$

$$ADCR = INT\left[\frac{Vin}{ADC\_AVREF} \times 2^d + 0.5\right]$$

Modified

or

$$(ADCR - 0.5) \times \frac{ADC\_AVREF}{2^d} \leq Vin < (ADCR + 0.5) \times \frac{ADC\_AVREF}{2^d}$$

■ Affected Scope due to this Update

- ✓ This correction applies only to the UM description (calculation formula) and has no impact on product specifications.

Before

39.3.9 A/D Conversion Result Registers11 to 0 (ADCR11 to ADCR0)

The following formula indicates the relationship between the analog input voltage that is input to analog input pins (ADC_CH8 to ADC_CH0) and the A/D conversion results (A/D conversion result registers (ADCR11 to ADCR0)).

$$ADCR = INT\left[\frac{Vin}{ADC\_AVREF} \times 2^d \times 0.5\right]$$

or

$$(ADCR - 0.5) \times \frac{ADC\_AVREF}{2^d} \leq Vin < (ADCR + 0.5) \times \frac{ADC\_AVREF}{2^d}$$

INT[ ]:	Function that returns the integer portion of the value enclosed in [ ]
Vin:	Analog input voltage
ADC_AVREF:	Voltage of power supply pin(ADC_AVDD18) for the analog unit
ADCR:	Value of A/D conversion result registers (ADCR11 to ADCR0)
d:	Resolution of A/D converter (d = 12 in this LSI)

After

39.3.9 A/D Conversion Result Registers11 to 0 (ADCR11 to ADCR0)

The following formula indicates the relationship between the analog input voltage that is input to analog input pins (ADC_CH8 to ADC_CH0) and the A/D conversion results (A/D conversion result registers (ADCR11 to ADCR0)).

$$ADCR = INT\left[\frac{Vin}{ADC\_AVREF} \times 2^d + 0.5\right]$$

Modified

or

$$(ADCR - 0.5) \times \frac{ADC\_AVREF}{2^d} \leq Vin < (ADCR + 0.5) \times \frac{ADC\_AVREF}{2^d}$$

INT[ ]:	Function that returns the integer portion of the value enclosed in [ ]
Vin:	Analog input voltage
ADC_AVREF:	Voltage of power supply pin(ADC_AVDD18) for the analog unit
ADCR:	Value of A/D conversion result registers (ADCR11 to ADCR0)
d:	Resolution of A/D converter (d = 12 in this LSI)

ADDED FOR SUPPLEMENTAL INFORMATION

Chapter 30. CAN-FD - DMA

■ Update Background

- ✓ Documentation clarification to prevent potential misunderstanding.
- ✓ The CAN-FD chapter could be interpreted as implying that the transmission DMA function is available, although the DMA chapter clarifies that this function is not supported on RZ/G3S. To prevent potential misunderstanding when referring to the CAN-FD chapter alone, a clarifying note has been added.

■ Impact on Customers (Details of the Issues or Issues Addressed)

- ✓ When referring only to the CAN-FD chapter, readers may mistakenly assume that the transmit DMA function is available.
- ✓ This update adds a note to clearly indicate that transmit DMA is not available.

■ Details of the Fixes

- ✓ The following NOTE has been added at the beginning of Chapter 30 (CAN-FD) for clarification

  **This LSI does not support the transmission DMA function for CAN-FD. Related descriptions of the transmission DMA function in this section should be ignored.*

■ Affected Scope due to this Update

- ✓ This update is limited to an additional note in the UM and does not affect functional specifications or existing products.

G2Lについても、補足追加要

Before

30. CAN-FD Interface (CAN-FD)

30.1 Overview

The LSI has a 2-channel CAN-FD module (CAN-FD) that complies with ISO 11898-1 (2015) Standards. CAN-FD transmits and receives both formats of messages, namely the standard identifier (11 bits) (identifier is hereafter referred to as ID) and extended ID (29 bits). **Table 30.1** lists the specifications of the CAN-FD, **Figure 30.1** shows a block diagram of the CAN-FD, and **Table 30.2** lists the I/O pins.

After

30. CAN-FD Interface (CAN-FD)

Added

NOTE

This LSI does not support the transmission DMA function for CAN-FD.
Related descriptions of the transmission DMA function in this section should be ignored.

30.1 Overview

The LSI has a 2-channel CAN-FD module (CAN-FD) that complies with ISO 11898-1 (2015) Standards. CAN-FD transmits and receives both formats of messages, namely the standard identifier (11 bits) (identifier is hereafter referred to as ID) and extended ID (29 bits). **Table 30.1** lists the specifications of the CAN-FD, **Figure 30.1** shows a block diagram of the CAN-FD, and **Table 30.2** lists the I/O pins.

Chapter 33. SD/MMC – SD card clock supply

■ Update Background

- ✓ Additional description regarding the clock requirements for the Card Detect and Write Protect functions of SD/MMC.

■ Impact on Customers(Details of the Issues or Issues Addressed)

- ✓ There is no change to the existing functional specifications; this update adds supplementary notes intended to further reduce power consumption.

■ Details of the Fixes

- ✓ In 33.3.2 Card Detect/Write Protect, the following explanation has been added at the beginning of the section:

33.3.2 Card Detect/Write Protect

For using the Card Detect and Write Protect functions, the IMCLK2 clock must be provided to this module.
In case of only Card Detect/Write Protect function is required, the IMCLK2 is required but the IMCLK can be stopped for reducing the power consumption. For example, in case of the SD card is not yet inserted to the slot and waiting for the card insertion by Card Detect function, only the IMCLK2 is required and IMCLK can be stopped. In case of data transfer is performed, both IMCLK and IMCLK2 should be provided to this module.

■ Affected Scope due to this Update

- ✓ This update only adds explanatory text to the UM and does not change product specifications.

Before

33.3.2 Card Detect/Write Protect

(1) Card Detect

The SD/MMC host interface has two types of card detect functions as described in the following.

- Card detect with ISDCD

Figure 33.6 shows the timing chart of card detect using ISDCD. ISDCD is connected to the card socket and pulled

After

Added

33.3.2 Card Detect/Write Protect

For using the Card Detect and Write Protect functions, the IMCLK2 clock must be provided to this module. In case of only Card Detect/Write Protect function is required, the IMCLK2 is required but the IMCLK can be stopped for reducing the power consumption. For example, in case of the SD card is not yet inserted to the slot and waiting for the card insertion by Card Detect function, only the IMCLK2 is required and IMCLK can be stopped. In case of data transfer is performed, both IMCLK and IMCLK2 should be provided to this module.

(1) Card Detect

The SD/MMC host interface has two types of card detect functions as described in the following.

- Card detect with ISDCD

Figure 33.6 shows the timing chart of card detect using ISDCD. ISDCD is connected to the card socket and pulled

UPDATE FOR PIN FUNCTION LIST

Chapter 1.4. Pin Function list - Condition at Reset (PRST_N="L")

- Update Background
  - ✓ Clarification of the DDR pin status under the reset condition where PRST# = L (PRST# = L).

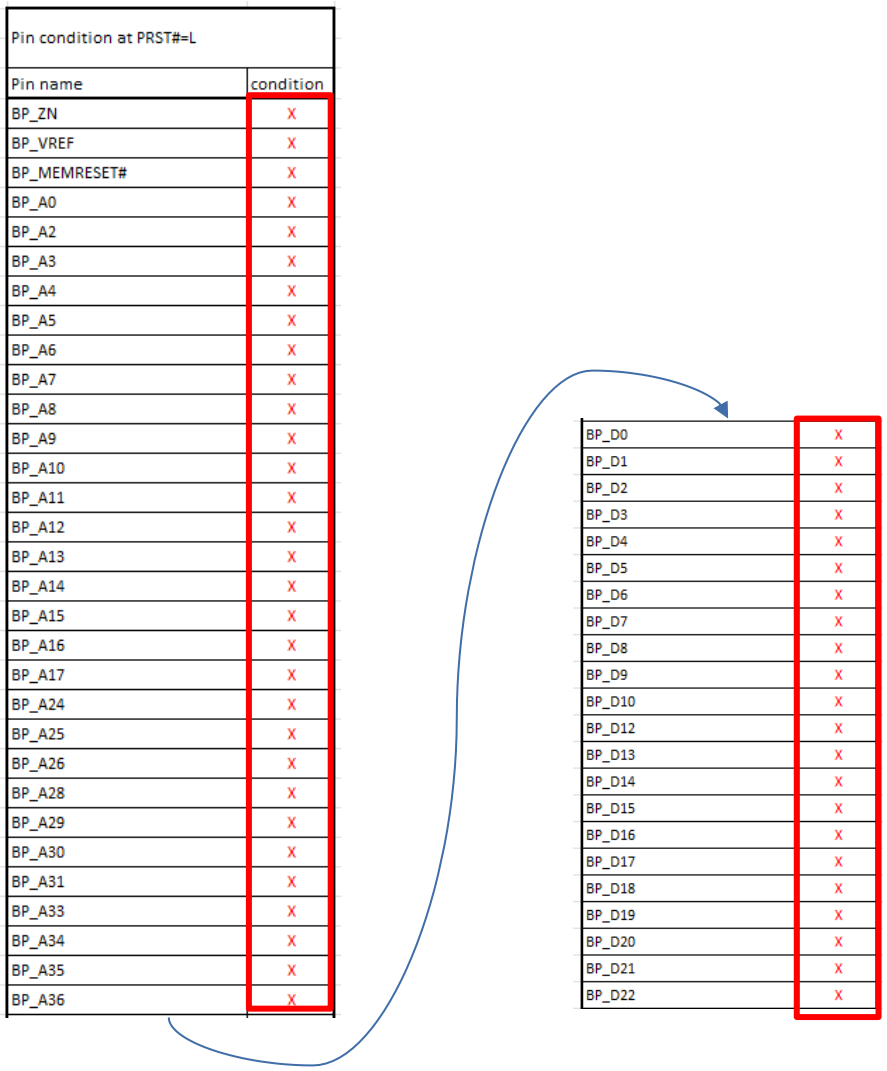
- Impact on Customers (Details of Issues or Issues Addressed)
  - ✓ This update clarifies the pin states during reset.
  - ✓ There is no impact on customers.

- Details of the Fixes
  - ✓ Update of "Pin condition at PRST_N = L" for DDR pins in the Pin Function List:
    - ✓ BP_MEMRESET# = L, BP_A0 = L, others = Z (Hi-Z)

- Affected Scope Due to This Update
  - ✓ None (clarification only)

Before

RZG3S_pinfunction_list (Excel file) attached in UM

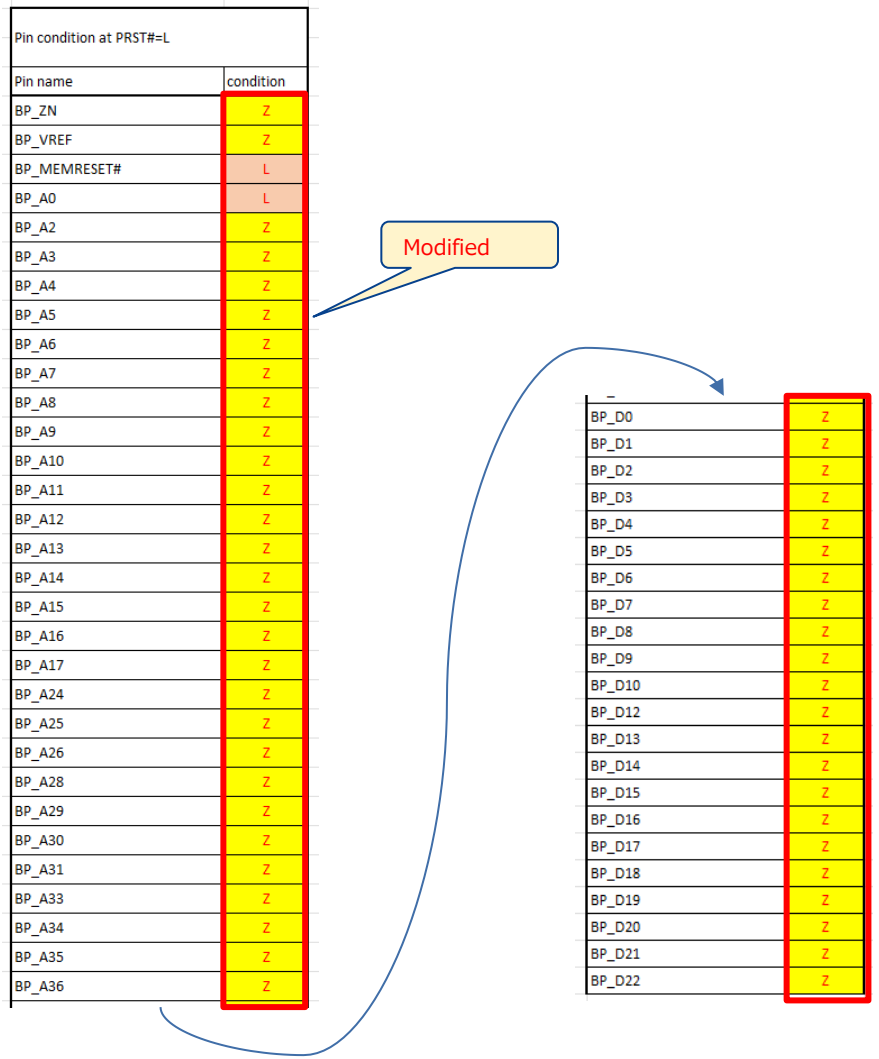


Pin condition at PRST#=L	
Pin name	condition
BP_ZN	X
BP_VREF	X
BP_MEMRESET#	X
BP_A0	X
BP_A2	X
BP_A3	X
BP_A4	X
BP_A5	X
BP_A6	X
BP_A7	X
BP_A8	X
BP_A9	X
BP_A10	X
BP_A11	X
BP_A12	X
BP_A13	X
BP_A14	X
BP_A15	X
BP_A16	X
BP_A17	X
BP_A24	X
BP_A25	X
BP_A26	X
BP_A28	X
BP_A29	X
BP_A30	X
BP_A31	X
BP_A33	X
BP_A34	X
BP_A35	X
BP_A36	X

BP_D0	X
BP_D1	X
BP_D2	X
BP_D3	X
BP_D4	X
BP_D5	X
BP_D6	X
BP_D7	X
BP_D8	X
BP_D9	X
BP_D10	X
BP_D12	X
BP_D13	X
BP_D14	X
BP_D15	X
BP_D16	X
BP_D17	X
BP_D18	X
BP_D19	X
BP_D20	X
BP_D21	X
BP_D22	X

After

RZG3S_pinfunction_list (Excel file) attached in UM



Pin condition at PRST#=L	
Pin name	condition
BP_ZN	Z
BP_VREF	Z
BP_MEMRESET#	L
BP_A0	L
BP_A2	Z
BP_A3	Z
BP_A4	Z
BP_A5	Z
BP_A6	Z
BP_A7	Z
BP_A8	Z
BP_A9	Z
BP_A10	Z
BP_A11	Z
BP_A12	Z
BP_A13	Z
BP_A14	Z
BP_A15	Z
BP_A16	Z
BP_A17	Z
BP_A24	Z
BP_A25	Z
BP_A26	Z
BP_A28	Z
BP_A29	Z
BP_A30	Z
BP_A31	Z
BP_A33	Z
BP_A34	Z
BP_A35	Z
BP_A36	Z

BP_D0	Z
BP_D1	Z
BP_D2	Z
BP_D3	Z
BP_D4	Z
BP_D5	Z
BP_D6	Z
BP_D7	Z
BP_D8	Z
BP_D9	Z
BP_D10	Z
BP_D12	Z
BP_D13	Z
BP_D14	Z
BP_D15	Z
BP_D16	Z
BP_D17	Z
BP_D18	Z
BP_D19	Z
BP_D20	Z
BP_D21	Z
BP_D22	Z

Chapter 1.4. Pin Function list - Handling for Unused Pins (xSPI, I3C)

■ Update Background
- ✓ Correction of a documentation error regarding “Handling when the Pin is not in Use” for the interface pins listed below.
  - ✓ XSPI_IO0−7, XSPI_DS
  - ✓ I3C_SDA/SCL

■ Impact on Customers (Details of Issues or Issues Addressed)
- ✓ If unused pins are left in an open-circuit (floating) state for an extended period without applying the software workaround described below, an associated shoot-through current flows internally, leading to increased power consumption and unintended heat generation.

■ Details of the Fixes

Update of “Handling when the Pin is not in Use” in the Pin Function List:
- ✓ XSPI_IO0−7, XSPI_DS : changed from open to pull-down/pull-up/XSPI_PVDD/VSS
- ✓ I3C_SDA/SCL : changed from open to pull-down/pull-up/I3C_PVDD/VSS

■ Affected Scope due to this Update
- ✓ Any effect is limited to the power-up/reset phase.
- ✓ For customer board designs where the listed interface pins are unused, appropriate handling (pull-up/pull-down) is recommended.

Before

RZG3S_pinfunction_list (Excel file) attached in UM

#Function0			Handling when the Pin is not in Use
Module	Pin Name	IO	
XSPI	XSPI_SPCLK	O	open
XSPI	XSPI_IO0	IO	open
XSPI	XSPI_IO1	IO	open
XSPI	XSPI_IO2	IO	open
XSPI	XSPI_IO3	IO	open
XSPI	XSPI_CS0#	O	open
XSPI	XSPI_CS1#	O	open
XSPI	XSPI_DS	IO	open
XSPI	XSPI_IO4	IO	open
XSPI	XSPI_IO5	IO	open
XSPI	XSPI_IO6	IO	open
XSPI	XSPI_IO7	IO	open
XSPI	XSPI_RESET0#	O	open
XSPI	XSPI_WP0#	O	open
	⋮		
I3C	I3C_SDA	IO	open
I3C	I3C_SCL	IO	open

After

RZG3S_pinfunction_list (Excel file) attached in UM

#Function0			Handling when the Pin is not in Use
Module	Pin Name	IO	
XSPI	XSPI_SPCLK	O	open
XSPI	XSPI_IO0	IO	pull-down/pull-up/XSPI_PVDD/VSS
XSPI	XSPI_IO1	IO	pull-down/pull-up/XSPI_PVDD/VSS
XSPI	XSPI_IO2	IO	pull-down/pull-up/XSPI_PVDD/VSS
XSPI	XSPI_IO3	IO	pull-down/pull-up/XSPI_PVDD/VSS
XSPI	XSPI_CS0#	O	open
XSPI	XSPI_CS1#	O	open
XSPI	XSPI_DS	IO	pull-down/pull-up/XSPI_PVDD/VSS
XSPI	XSPI_IO4	IO	pull-down/pull-up/XSPI_PVDD/VSS
XSPI	XSPI_IO5	IO	pull-down/pull-up/XSPI_PVDD/VSS
XSPI	XSPI_IO6	IO	pull-down/pull-up/XSPI_PVDD/VSS
XSPI	XSPI_IO7	IO	pull-down/pull-up/XSPI_PVDD/VSS
XSPI	XSPI_RESET0#	O	open
XSPI	XSPI_WP0#	O	open
	⋮		
I3C	I3C_SDA	IO	pull-down/pull-up/I3C_PVDD/VSS
I3C	I3C_SCL	IO	pull-down/pull-up/I3C_PVDD/VSS

Modified

Modified

Modified

Chapter 1.4. Pin Function list - Handling for Unused Pins (xSPI, I3C) Software workaround

■ Software workaround

If it is difficult to terminate unused pins with pull-down, pull-up, or tie them to *_PVDD/VSS,

Please apply following software workaround during the **initial phase of the user program executed after startup**.

■ Summary

Unused pins of XSPI_IO0-7, XSPI_DS

Configure GPIO pull-down settings.

Internal pull-down resistors are enabled via GPIO Pull-Up / Pull-Down Switching Registers.

Unused pins of I3C_SDA, I3C_SCL

Disable input enable via GPIO IEN register.

For unused I3C pins, input buffers are disabled via the Input Enable Control Register (IEN) within GPIO.

Chapter 1.4. Pin Function list - Handling for Unused Pins (xSPI, I3C) Software workaround

- Target Pins
  Unused pins of XSPI_IO0-7, XSPI_DS

- Setting
  Set the corresponding bits to 2'b10 (Pull Down) in the Pull Up/Down Switching registers. (PUPD_04, PUPD_05_L, PUPD_05_H)

- Base address
  The base address of the GPIO is shown below.

  Base address: H'0_1103_0000 (Cortex-A55 Address Space)
  Base address: H'4103_0000 (Cortex-M33 Address Space Non-Secure)
  Base address: H'5103_0000 (Cortex-M33 Address Space Secure)

- Register configuration

Register Name	Abbreviation	R/W	Initial Value	Offset Address	Access Size
PULL UP/PULL DOWN SWITCHING REGISTER 04	PUPD_04	R/W	H'0000_0000	H'1C20	8/16/32
PULL UP/PULL DOWN SWITCHING REGISTER 05_L	PUPD_05_L	R/W	H'0000_0000	H'1C28	8/16/32
PULL UP/PULL DOWN SWITCHING REGISTER 05_H	PUPD_05_H	R/W	H'0000_0000	H'1C2C	8/16/32

- Correspondence between Register and Each Terminal

Bit Name	bit25-24	bit17-16	bit9-8	bit1-0
PUPD_04	XSPI_DS	–	–	–
PUPD_05_L	XSPI_IO03	XSPI_IO02	XSPI_IO01	XSPI_IO00
PUPD_05_H	XSPI_IO07	XSPI_IO06	XSPI_IO05	XSPI_IO04

Note
These registers are private GPIO registers and are therefore not described in the User's Manual.
The functionality will be disclosed in the next User's Manual update.

Chapter 1.4. Pin Function list - Handling for Unused Pins (xSPI, I3C) Software workaround

- Target Pins
  I3C_SDA, I3C_SCL

- Setting
  Set the corresponding bits (bit8 and bit0) to 1'b0 in the Input Enable Control Register. (IEN_09)

- Base address
  The base address of the GPIO is shown below.

  Base address: H'0_1103_0000 (Cortex-A55 Address Space)
  Base address: H'4103_0000 (Cortex-M33 Address Space Non-Secure)
  Base address: H'5103_0000 (Cortex-M33 Address Space Secure)

Note
In the current User's Manual(Rev1.20), this is described as H'0000_0000; however, the correct value is H'0000_0101. This typo will be corrected in the next User's Manual update.

- Register configuration

Register Name	Abbreviation	R/W	Initial Value	Offset Address	Access Size
INPUT ENABLE CONTROL REGISTER 09	IEN_09	R/W	H'0000_0101	H'1848	8/16/32

- Correspondence between Register and Each Terminal

Bit Name	bit24	bit16	bit8	bit0
IEN_09	—	—	I3C_SCL	I3C_SDA

UPDATE FOR I3C

Chapter 26. I3C - *(An overall revision and update)

■ Update Background
- ✓ The updates to the I3C section are not due to changes in product functionality or hardware specifications.
- ✓ They were made to align the User's Manual with the latest I3C external specification, as an older version had been referenced previously. As a result, many descriptions - particularly those related to configuration procedures - have been revised.

■ Impact on Customers(Details of the Issues or Issues Addressed)
- ✓ The I3C functionality itself has not been replaced or re-implemented. However, if configuration procedures were understood or implemented based on the previous manual, differences may exist compared with the latest recommended descriptions.
- ✓ Customers are therefore requested to review the updated I3C configuration procedures, including the before-and-after comparisons, and revise their settings as necessary.

■ Details of the Fixes
- ✓ For further details of the updates and the before-and-after comparisons, please refer to the subsequent pages.

■ Affected Scope due to this Update
- ✓ This correction applies only to the UM description and has no impact on device functionality or silicon behavior.

Before

26.1.1 Functional Overview

The I3C bus interface (I3C) has 1 channel. The I3C module conform with and provide a subset of the NXP I²C (Inter-Integrated Circuit) bus interface functions and a subset of the MIPI I3C.

Table 26.1 lists the I²C specifications, and **Table 26.2** lists the I3C specifications.

Table 26.1 I²C Specifications

Item	Description
Operation mode	Master mode and slave mode selectable
Data handler	Single buffer transfer
⋮	⋮
Error detection	• NACK received • Arbitration lost error • Timeout error
Wake-Up Source	• Address detection of Slave Address
Operation mode	Master (main master/secondary master) mode and slave mode selectable
Data handler	[Master] Normal FIFO buffer transfer [Slave] Normal FIFO buffer transfer

Table 26.2 I3C Specifications

Item	Description
Communication protocol	• SDR (I3C single data rate) mode – Private message – Broadcast message (common command code) – Direct message (common command code) • Legacy I²C message – Fast-mode (Fm): up to 400 kbps – Fast-mode Plus (Fm+): up to 1 Mbps

After

26.1.1 Functional Overview

The I3C bus interface (I3C) has 1 channel. The I3C module conform with and provide a subset of the NXP I²C (Inter-Integrated Circuit) bus interface functions and a subset of the MIPI I3C.

Table 26.1 lists the I²C specifications, and **Table 26.2** lists the I3C specifications.

Table 26.1 I²C Specifications

Item	Description
Operation mode	Master mode and slave mode selectable
Data handler	Single buffer transfer
⋮	⋮
Error detection	• NACK received • Arbitration lost error • Timeout error
Wake-Up Source	• Address detection of Slave Address

moved

Table 26.2 I3C Specifications

Item	Description
Operation mode	Master (main master/secondary master) mode and slave mode selectable.
Data handler	• Master: Normal FIFO buffer transfer • Slave: Normal FIFO buffer transfer
Communication protocol	• SDR (I3C single data rate) mode – Private message – Broadcast message (common command code) – Direct message (common command code) • Legacy I²C message – Fast-mode (Fm): up to 400 kbps – Fast-mode Plus (Fm+): up to 1 Mbps

Before

Table 26.2 I3C Specifications

Item	Description
Communication protocol	• SDR (I3C single data rate) mode – Private message – Broadcast message (common command code) – Direct message (common command code) • Legacy I²C message – Fast-mode (Fm): up to 400 kbps – Fast-mode Plus (Fm+): up to 1 Mbps
⋮	⋮
Interrupt source	• Non-recoverable internal error • Transfer error • Transfer abort • Response queue full • Command queue empty • IBI status queue full • Receive data buffer full • Transmit data buffer empty • Receive status queue full • START condition detection • STOP condition detection • HDR exit pattern detection • Timeout detection • Wake-up condition detection
⋮	⋮

Deleted

After

Table 26.2 I3C Specifications

Item	Description
Communication protocol	• SDR (I3C single data rate) mode – Private message – Broadcast message (common command code) – Direct message (common command code) • Legacy I²C message – Fast-mode (Fm): up to 400 kbps – Fast-mode Plus (Fm+): up to 1 Mbps
⋮	⋮
Interrupt source	• Non-recoverable internal error • Transfer error • Transfer abort • Response queue full • Command queue empty • IBI status queue full • Receive data buffer full • Transmit data buffer empty • Receive status queue full • START condition detection • STOP condition detection • Timeout detection • Wake-up condition detection
⋮	⋮

Before

Table 26.3 I3C I/O Pins

Function	Pin name	I/O	Description
I3C	I3C_SCL	I/O	Input/output pins for clock
	I3C_SDA	I/O	Input/output pins for data

After

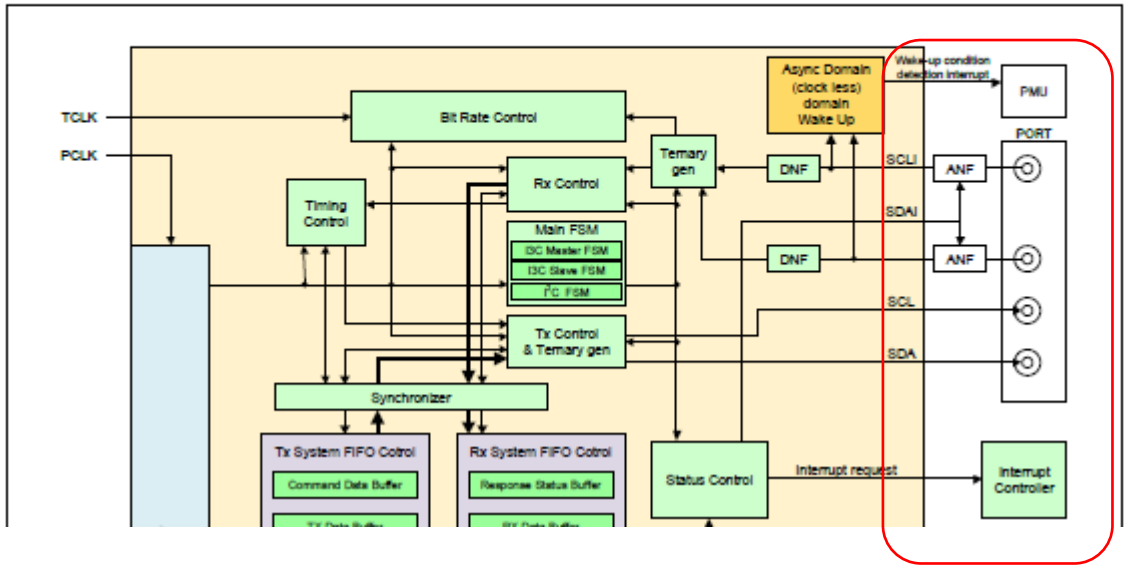
Pin Name	Signal Name in This Section	Input/Output	Functional Description
I3C_SCL	SCL	I/O	Input/output pins for clock
I3C_SDA	SDA	I/O	Input/output pins for data

Modified

Before

26.1.2 Block Diagram [I²C/I3C common]

Figure 26.1 shows the main components of this I3C.



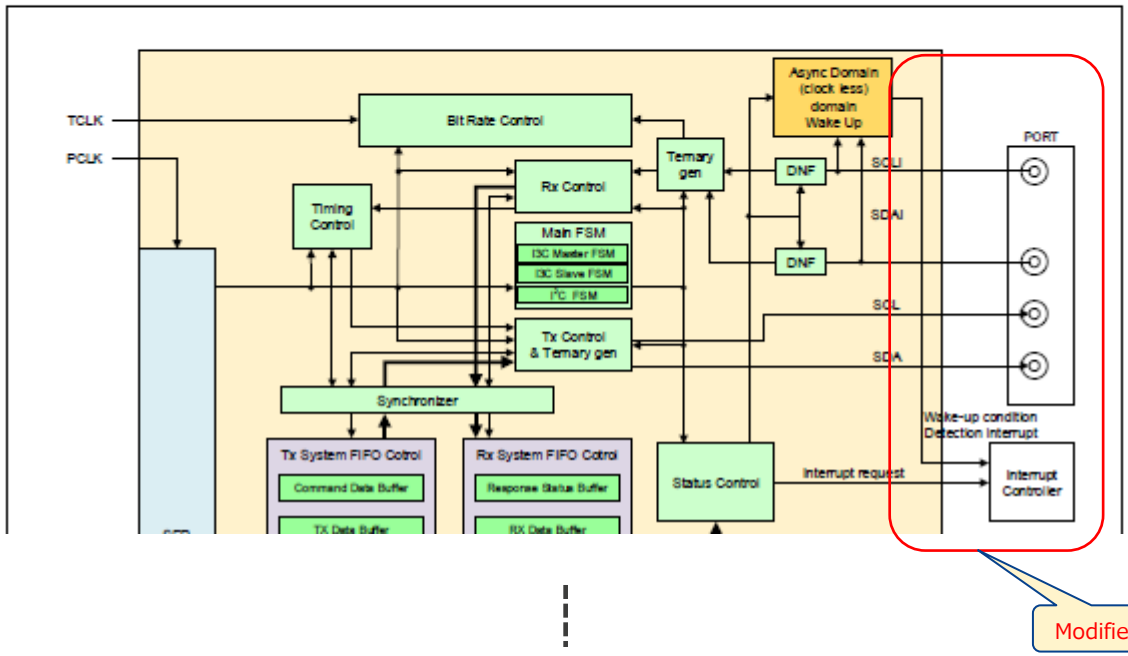
Note: TCLK (I3C_TCLK) = P5ϕ = PCLKD
PCLK (I3C_PCLK) = TSUϕ = PCLKB

Figure 26.1 I3C Block Diagram

After

26.1.2 Block Diagram [I²C/I3C common]

Figure 26.1 shows the main components of this I3C.



Note: TCLK (I3C_TCLK) = P5ϕ = PCLKD
PCLK (I3C_PCLK) = TSUϕ = PCLKB

Figure 26.1 I3C Block Diagram

Before

26.2.1 List of Registers

Table 26.4 List of I3C Registers (2/3)

Register	Symbol	Offset Address
Device Address Table Basic Register 6	DATBAS6	H'254
Device Address Table Basic Register 7	DATBAS7	H'25C
Slave Device Address Table Basic Register 0	SDATBAS0	H'2B0
Slave Device Address Table Basic Register 1	SDATBAS1	H'2B4
Slave Device Address Table Basic Register 2	SDATBAS2	H'2B8
Master Device Characteristic Table Register 0	MSDCT0	H'2D0
Master Device Characteristic Table Register 1	MSDCT1	H'2D4
Master Device Characteristic Table Register 2	MSDCT2	H'2D8
Master Device Characteristic Table Register 3	MSDCT3	H'2DC
Master Device Characteristic Table Register 4	MSDCT4	H'2E0
Master Device Characteristic Table Register 5	MSDCT5	H'2E4
Master Device Characteristic Table Register 6	MSDCT6	H'2E8
Master Device Characteristic Table Register 7	MSDCT7	H'2EC
Extended Device Address Table Basic Register	EXDATBAS	H'310
Slave Device Characteristic Table Register	SVDCT	H'320

After

26.2.1 List of Registers

Table 26.4 List of I3C Registers (2/3)

Register	Symbol	Offset Address
Device Address Table Basic Register 6	DATBAS6	H'254
Device Address Table Basic Register 7	DATBAS7	H'25C
Extended Device Address Table Basic Register	EXDATBAS	H'2A0
Slave Device Address Table Basic Register 0	SDATBAS0	H'2B0
Slave Device Address Table Basic Register 1	SDATBAS1	H'2B4
Slave Device Address Table Basic Register 2	SDATBAS2	H'2B8
Master Device Characteristic Table Register 0	MSDCT0	H'2D0
Master Device Characteristic Table Register 1	MSDCT1	H'2D4
Master Device Characteristic Table Register 2	MSDCT2	H'2D8
Master Device Characteristic Table Register 3	MSDCT3	H'2DC
Master Device Characteristic Table Register 4	MSDCT4	H'2E0
Master Device Characteristic Table Register 5	MSDCT5	H'2E4
Master Device Characteristic Table Register 6	MSDCT6	H'2E8
Master Device Characteristic Table Register 7	MSDCT7	H'2EC
Slave Device Characteristic Table Register	SVDCT	H'320

Modified

Moved

Before

26.2.24 Wake Up Unit Control Register (WUCTL)

Bit	Bit Name	Initial Value	R/W	Description
31 to 8	—	All 0	R	Reserved These bits are read as 0. The write value should be 0.
7	WUFE	0b	R/W	Wake Up function enable 0: Wake-up function disables 1: Wake-up function enables. Do not set WUFE = 0 during WakeUp operation.
6	WUFSYNE	1b	R/W	Wake-Up function Synchronous Enable 0: This IP asynchronous circuit enable 1: This IP synchronous circuit enable
5	—	0b	R	Reserved These bits are read as 0. The write value should be 0.
4	WUANFS	0b	R/W	Wake-Up Analog Noise Filter Selection 0: Do n1ot add the Wake-Up analog filter. 1: Add the Wake-Up analog filter.
3 to 1	—	000b	R	Reserved These bits are read as 0. The write value should be 0.
0	WUACKS	1b	R/W	Wake-Up Acknowledge Selection Choice of four response mode with a combination of RSTCTL.INTLRST bit and WUACKS bit. Shown in the **Table 26.7**.

After

26.2.24 Wake Up Unit Control Register (WUCTL)

Bit	Bit Name	Initial Value	R/W	Description
31 to 8	—	All 0	R	Reserved These bits are read as 0. The write value should be 0.
7	WUFE	0b	R/W	Wake Up function enable 0: Wake-up function disables 1: Wake-up function enables. Do not set WUFE = 0 during WakeUp operation.
6	WUFSYNE	1b	R/W	Wake-Up function Synchronous Enable 0: This IP asynchronous circuit enable 1: This IP synchronous circuit enable
5	—	0b	R	Reserved These bits are read as 0. The write value should be 0.
4	WUANFS	0b	R/W	Wake-Up Analog Noise Filter Selection*1 0: Do not add the Wake-Up analog filter. 1: Add the Wake-Up analog filter.
3 to 1	—	000b	R	Reserved These bits are read as 0. The write value should be 0.
0	WUACKS	1b	R/W	Wake-Up Acknowledge Selection Choice of four response mode with a combination of RSTCTL.INTLRST bit and WUACKS bit. Shown in the **Table 26.7**.

Note 1. This bit supports I²C mode.

Addition

Modified

Addition

Before

26.2.39 Normal Queue Threshold Control Register (NQTHCTL)

Bit	Bit Name	Initial Value	R/W	Description
31 to 24	IBIQTH[7:0]	H'01	R/W	Normal IBI Queue Threshold*1 H'00: I3C Protocol mode (Master): Interrupt is generated when the Outstanding IBI Status count is 1 or more. I3C Protocol mode (Slave): Interrupt is issued when IBI Data Buffer is completely empty. Others: I3C Protocol mode (Master): Interrupt is generated when the Outstanding IBI Status count is N + 1 or more. (N = CMDQTH[7:0]) I3C Protocol mode (Slave): Interrupt is issued when IBI Data Buffer contains N empties.
23 to 16	IBIDSSZ[7:0]	H'01	R/W	Normal IBI Data Segment Size*2 Supported Values: Minimum: 1 (4 bytes) Maximum: 63 (252 bytes), provided that the configured IBI Queue depth is 64 or more. When ATCCNTE.ATCE = 1, restrict to the number of slices ≥ 2.
15 to 8	RSPQTH[7:0]	H'01	R/W	Normal Response Queue Threshold*1 H'00: Interrupt is issued when Response Queue contains 1 entry (DWORD). Others: Interrupt is triggered when Response Queue contains N + 1 entries (DWORD). (N = CMDQTH[7:0])
7 to 0	CMDQTH[7:0]	H'01	R/W	Normal Command Ready Queue Threshold*1 H'00: Interrupt is issued when Command Queue is completely empty. Others: Interrupt is issued when Command Queue contains N empties. (N = CMDQTH[7:0])

Note: This register supports for I3C secondary master mode and I3C slave mode.

Note 1. These bits support for all I3C mode.

Note 2. These bits support for I3C master mode and I3C secondary master mode.

Deleted

After

26.2.39 Normal Queue Threshold Control Register (NQTHCTL)

Bit	Bit Name	Initial Value	R/W	Description
31 to 24	IBIQTH[7:0]	H'01	R/W	Normal IBI Queue Threshold*1 H'00: I3C Protocol mode (Master): Interrupt is generated when the Outstanding IBI Status count is 1 or more. I3C Protocol mode (Slave): Interrupt is issued when IBI Data Buffer is completely empty. Others: I3C Protocol mode (Master): Interrupt is generated when the Outstanding IBI Status count is N + 1 or more. (N = CMDQTH[7:0]) I3C Protocol mode (Slave): Interrupt is issued when IBI Data Buffer contains N empties.
23 to 16	IBIDSSZ[7:0]	H'01	R/W	Normal IBI Data Segment Size*2 Supported Values: Minimum: 1 (4 bytes) Maximum: 63 (252 bytes), provided that the configured IBI Queue depth is 64 or more. When ATCCNTE.ATCE = 1, restrict to the number of slices ≥ 2.
15 to 8	RSPQTH[7:0]	H'01	R/W	Normal Response Queue Threshold*1 H'00: Interrupt is issued when Response Queue contains 1 entry (DWORD). Others: Interrupt is triggered when Response Queue contains N + 1 entries (DWORD). (N = CMDQTH[7:0])
7 to 0	CMDQTH[7:0]	H'01	R/W	Normal Command Ready Queue Threshold*1 H'00: Interrupt is issued when Command Queue is completely empty. Others: Interrupt is issued when Command Queue contains N empties. (N = CMDQTH[7:0])

Note 1. These bits support for all I3C mode.

Note 2. These bits support for I3C master mode and I3C secondary master mode.

Before

26.2.42 Bus Status Register (BST)

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
	—	—	—	—	—	—	—	WUCNDDF	—	—	—	TODF	—	—	—	ALF
Initial Value	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
R/W	R	R	R	R	R	R	R	R/W	R	R	R	R/W	R	R	R	R/W

Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
	—	—	—	—	—	—	—	TENDF	—	—	—	NACKDF	—	HDREXDF	SPCNDDF	STCNDDF
Initial Value	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
R/W	R	R	R	R	R	R	R	R/W	R	R	R	R/W	R	R/W	R/W	R/W

Bit	Bit Name	Initial Value	R/W	Description
31 to 25	—	All 0	R	Reserved These bits are read as 0. The write value should be 0.
24	WUCNDDF	0b	R/W*3	Wake-Up Condition Detection Flag 0: Wake-Up Condition is not detected. 1: Wake-Up Condition is detected.
23 to 21	—	All 0	R	Reserved These bits are read as 0. The write value should be 0.
20	TODF	0b	R/W*3	Timeout Detection Flag 0: Timeout is not detected. 1: Timeout is detected.
19 to 17	—	All 0	R	Reserved These bits are read as 0. The write value should be 0.
16	ALF	0b	R/W*3	Arbitration Lost Flag*2 0: Arbitration is not lost 1: Arbitration is lost.
⋮				
8	TENDF	0b	R/W*3	Transmit End Flag*2 0: Data is being transmitted. 1: Data has been transmitted.
7 to 5	—	000b	R	Reserved These bits are read as 0. The write value should be 0.
4	NACKDF	0b	R/W*3	NACK Detection Flag*2 0: NACK is not detected. 1: NACK is detected.
3	—	0b	R	Reserved This bit is read as 0. The write value should be 0.
2	HDREXDF	0b	R/W*3	HDR Exit Pattern Detection Flag*1 0: HDR Exit Pattern Detection Interrupt does not occur. 1: HDR Exit Pattern Detection Interrupt occurs.
1	SPCNDDF	0b	R/W*3	STOP Condition Detection Flag 0: STOP condition is not detected. 1: STOP condition is detected.
0	STCNDDF	0b	R/W*3	START Condition Detection Flag 0: START condition is not detected. 1: START condition is detected.

Note 1. This bit supports for all I3C mode.

Note 2. This bit supports for I²C mode.

Note 3. Clearing (to 0) condition: Writing 0 after 1 is read.

Deleted

After

26.2.42 Bus Status Register (BST)

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
	—	—	—	—	—	—	—	WUCNDDF	—	—	—	TODF	—	—	—	ALF
Initial Value	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
R/W	R	R	R	R	R	R	R	R/W	R	R	R	R/W	R	R	R	R/W

Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
	—	—	—	—	—	—	—	TENDF	—	—	—	NACKDF	—	—	SPCNDDF	STCNDDF
Initial Value	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
R/W	R	R	R	R	R	R	R	R/W	R	R	R	R/W	R	R/W	R/W	R/W

Modified

Bit	Bit Name	Initial Value	R/W	Description
31 to 25	—	All 0	R	Reserved These bits are read as 0. The write value should be 0.
24	WUCNDDF	0b	R/W*2	Wake-Up Condition Detection Flag 0: Wake-Up Condition is not detected. 1: Wake-Up Condition is detected.
23 to 21	—	All 0	R	Reserved These bits are read as 0. The write value should be 0.
20	TODF	0b	R/W*2	Timeout Detection Flag 0: Timeout is not detected. 1: Timeout is detected.
19 to 17	—	All 0	R	Reserved These bits are read as 0. The write value should be 0.
16	ALF	0b	R/W*2	Arbitration Lost Flag*1 0: Arbitration is not lost 1: Arbitration is lost.
⋮				
8	TENDF	0b	R/W*2	Transmit End Flag*1 0: Data is being transmitted. 1: Data has been transmitted.
7 to 5	—	000b	R	Reserved These bits are read as 0. The write value should be 0.
4	NACKDF	0b	R/W*2	NACK Detection Flag*1 0: NACK is not detected. 1: NACK is detected.
3	—	0b	R	Reserved This bit is read as 0. The write value should be 0.
2	—	0b	R/W	Reserved This bit is read as 0. The write value should be 0.
1	SPCNDDF	0b	R/W*2	STOP Condition Detection Flag 0: STOP condition is not detected. 1: STOP condition is detected.
0	STCNDDF	0b	R/W*2	START Condition Detection Flag 0: START condition is not detected. 1: START condition is detected.

Modified (in red frames)

Note 1. This bit supports for I²C mode.

Note 2. Clearing (to 0) condition: Writing 0 after 1 is read.

Modified

Before

26.2.42 Bus Status Register (BST)

SPCNDDF bit (STOP Condition Detection Flag)

[Setting conditions]

- All of the followings are satisfied:
  1. The BSTE.SPCNDDE bit = 1.
  2. When a STOP condition is detected.

[Clearing condition]

- When 0 is written to the SPCNDDF flag after reading SPCNDDF flag = 1.

HDREXDF bit (HDR Exit Pattern Detection Flag)

[Setting conditions]

- All of the followings are satisfied:
  1. The BSTE.HDREXDE bit = 1.
  2. When a HDR EXIT pattern is detected.

[Clearing condition]

- When 0 is written to the HDREXDF flag after reading HDREXDF flag = 1.

Deleted

NACKDF bit (NACK Detection Flag)

[Setting conditions]

- All of the followings are satisfied:
  1. The PRTS.PRTMD bit = 1 (I^2C protocol mode).
  2. The BSTE.NACKDE bit = 1 (Enables NACK detection interrupt status logging).
  3. When acknowledge is not received (NACK is received) from the receive device in transmit mode.

[Clearing condition]

- When 0 is written to the NACKDF flag after reading NACKDF flag = 1.

After

26.2.42 Bus Status Register (BST)

SPCNDDF bit (STOP Condition Detection Flag)

[Setting conditions]

- All of the followings are satisfied:
  1. The BSTE.SPCNDDE bit = 1.
  2. When a STOP condition is detected.

[Clearing condition]

- When 0 is written to the SPCNDDF flag after reading SPCNDDF flag = 1.

NACKDF bit (NACK Detection Flag)

[Setting conditions]

- All of the followings are satisfied:
  1. The PRTS.PRTMD bit = 1 (I^2C protocol mode).
  2. The BSTE.NACKDE bit = 1 (Enables NACK detection interrupt status logging).
  3. When acknowledge is not received (NACK is received) from the receive device in transmit mode.

[Clearing condition]

- When 0 is written to the NACKDF flag after reading NACKDF flag = 1.

Before

26.2.43 Bus Status Enable Register (BSTE)

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
	—	—	—	—	—	—	—	WUCNDDE	—	—	—	TODE	—	—	—	ALE
Initial Value	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
R/W	R	R	R	R	R	R	R	R/W	R	R	R	R/W	R	R	R	R/W

Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
	—	—	—	—	—	—	—	TENDE	—	—	—	NACKDE	—	HDREXDE	SPCNDDE	STCNDDE
Initial Value	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
R/W	R	R	R	R	R	R	R	R/W	R	R	R	R/W	R	R/W	R/W	R/W

Bit	Bit Name	Initial Value	R/W	Description
⋮				
16	ALE	0b	R/W	Arbitration Lost Enable*2 0: Disables Arbitration Lost Interrupt Status logging. 1: Enables Arbitration Lost Interrupt Status logging.
15 to 9	—	All 0	R	Reserved These bits are read as 0. The write value should be 0.
8	TENDE	0b	R/W	Transmit End Enable*2 0: Disables Transmit End Interrupt Status logging. 1: Enables Transmit End Interrupt Status logging.
7 to 5	—	000b	R	Reserved These bits are read as 0. The write value should be 0.
4	NACKDE	0b	R/W	NACK Detection Enable*2 0: Disables NACK Detection Interrupt Status logging. 1: Enables NACK Detection Interrupt Status logging.
3	—	0b	R	Reserved This bit is read as 0. The write value should be 0.
2	HDREXDE	0b	R/W	HDR Exit Pattern Detection Enable*1 0: Disables HDR Exit Pattern Detection Interrupt Status logging. 1: Enables HDR Exit Pattern Detection Interrupt Status logging.
1	SPCNDDE	0b	R/W	STOP Condition Detection Enable 0: Disables STOP condition Detection Interrupt Status logging. 1: Enables STOP condition Detection Interrupt Status logging.
0	STCNDDE	0b	R/W	START Condition Detection Enable 0: Disables START condition Detection Interrupt Status logging. 1: Enables START condition Detection Interrupt Status logging.

Note 1. This bit supports for all I3C mode.
Note 2. This bit supports for I²C mode.

Deleted

After

26.2.43 Bus Status Enable Register (BSTE)

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
	—	—	—	—	—	—	—	WUCNDDE	—	—	—	TODE	—	—	—	ALE
Initial Value	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
R/W	R	R	R	R	R	R	R	R/W	R	R	R	R/W	R	R	R	R/W

Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
	—	—	—	—	—	—	—	TENDE	—	—	—	NACKDE	—	—	SPCNDDE	STCNDDE
Initial Value	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
R/W	R	R	R	R	R	R	R	R/W	R	R	R	R/W	R	R/W	R/W	R/W

Modified

Bit	Bit Name	Initial Value	R/W	Description
⋮				
16	ALE	0b	R/W	Arbitration Lost Enable*1 0: Disables Arbitration Lost Interrupt Status logging. 1: Enables Arbitration Lost Interrupt Status logging.
15 to 9	—	All 0	R	Reserved These bits are read as 0. The write value should be 0.
8	TENDE	0b	R/W	Transmit End Enable*1 0: Disables Transmit End Interrupt Status logging. 1: Enables Transmit End Interrupt Status logging.
7 to 5	—	000b	R	Reserved These bits are read as 0. The write value should be 0.
4	NACKDE	0b	R/W	NACK Detection Enable*1 0: Disables NACK Detection Interrupt Status logging. 1: Enables NACK Detection Interrupt Status logging.
3	—	0b	R	Reserved This bit is read as 0. The write value should be 0.
2	—	0b	R/W	Reserved This bit is read as 0. The write value should be 0.
1	SPCNDDE	0b	R/W	STOP Condition Detection Enable 0: Disables STOP condition Detection Interrupt Status logging. 1: Enables STOP condition Detection Interrupt Status logging.
0	STCNDDE	0b	R/W	START Condition Detection Enable 0: Disables START condition Detection Interrupt Status logging. 1: Enables START condition Detection Interrupt Status logging.

Modified (in red frames)

Note 1. This bit supports for I²C mode.

Modified

Before

26.2.43 Bus Status Enable Register (BSTE)

STCNDDE bit (START Condition Detection Enable)

When this bit is 1, operation of BST.STCNDDF is enabled. For the setting conditions and clearing conditions of the BST.STCNDDF flag, see the details of BST.STCNDDF.

SPCNDDE bit (STOP Condition Detection Enable)

When this bit is 1, operation of BST.SPCNDDF is enabled. For the setting conditions and clearing conditions of the BST.SPCNDDF flag, see the details of BST.SPCNDDF.

HDREXDE bit (HDR Exit Pattern Detection Enable)

When this bit is 1, the operation of BST.HDREXDF is enabled. For the setting conditions and clearing conditions of the BST.HDREXDF flag, see the details of BST.HDREXDF.

NACKDE bit (NACK Detection Enable)

When this bit is 1, the operation of BST.NACKDF is enabled. This bit is used to specify whether to continue or discontinue the transfer operation when NACK is received from the slave device in transmit mode. Normally, set this bit to 1. For the setting conditions and clearing conditions of the BST.NACKDF flag, see the details of BST.NACKDF.

Deleted

After

26.2.43 Bus Status Enable Register (BSTE)

STCNDDE bit (START Condition Detection Enable)

When this bit is 1, operation of BST.STCNDDF is enabled. For the setting conditions and clearing conditions of the BST.STCNDDF flag, see the details of BST.STCNDDF.

SPCNDDE bit (STOP Condition Detection Enable)

When this bit is 1, operation of BST.SPCNDDF is enabled. For the setting conditions and clearing conditions of the BST.SPCNDDF flag, see the details of BST.SPCNDDF.

NACKDE bit (NACK Detection Enable)

When this bit is 1, the operation of BST.NACKDF is enabled. This bit is used to specify whether to continue or discontinue the transfer operation when NACK is received from the slave device in transmit mode. Normally, set this bit to 1. For the setting conditions and clearing conditions of the BST.NACKDF flag, see the details of BST.NACKDF.

Before

26.2.44 Bus Interrupt Enable Register (BIE)

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
	—	—	—	—	—	—	—	WUCNDDIE	—	—	—	TODIE	—	—	—	ALIE
Initial Value	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
R/W	R	R	R	R	R	R	R	R/W	R	R	R	R/W	R	R	R	R/W

Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
	—	—	—	—	—	—	—	TENDIE	—	—	—	NACKDIE	—	HDREXDIE	SPCNDDIE	STCNDDIE
Initial Value	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
R/W	R	R	R	R	R	R	R	R/W	R	R	R	R/W	R	R/W	R/W	R/W

Bit	Bit Name	Initial Value	R/W	Description
⋮				
20	TODIE	0b	R/W	Timeout Detection Interrupt Enable*2 0: Disables Timeout Detection Interrupt Signal. 1: Enables Timeout Detection Interrupt Signal.
19 to 17	—	All 0	R	Reserved This bit is read as 0. The write value should be 0.
16	ALIE	0b	R/W	Arbitration Lost Interrupt Enable*2 0: Disables Arbitration Lost Interrupt Signal. 1: Enables Arbitration Lost Interrupt Signal.
15 to 9	—	All 0	R	Reserved This bit is read as 0. The write value should be 0.
8	TENDIE	0b	R/W	Transmit End Interrupt Enable*2 0: Disables Transmit End Interrupt Signal. 1: Enables Transmit End Interrupt Signal.
7 to 5	—	000b	R	Reserved This bit is read as 0. The write value should be 0.
4	NACKDIE	0b	R/W	NACK Detection Interrupt Enable*2 0: Disables NACK Detection Interrupt Signal. 1: Enables NACK Detection Interrupt Signal.
3	—	0b	R	Reserved This bit is read as 0. The write value should be 0.
2	HDREXDIE	0b	R/W	HDR Exit Pattern Detection Interrupt Enable*1 0: Disables HDR Exit Pattern Detection Interrupt Signal. 1: Enables HDR Exit Pattern Detection Interrupt Signal.
1	SPCNDDIE	0b	R/W	STOP Condition Detection Interrupt Enable 0: Disables STOP condition Detection Interrupt Signal. 1: Enables STOP condition Detection Interrupt Signal.
0	STCNDDIE	0b	R/W	START Condition Detection Interrupt Enable 0: Disables START condition Detection Interrupt Signal. 1: Enables START condition Detection Interrupt Signal.

Note 1. This bit supports for all I3C mode.
Note 2. This bit supports for I²C mode.

Deleted

After

26.2.44 Bus Interrupt Enable Register (BIE)

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
	—	—	—	—	—	—	—	WUCNDDIE	—	—	—	TODIE	—	—	—	ALIE
Initial Value	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
R/W	R	R	R	R	R	R	R	R/W	R	R	R	R/W	R	R	R	R/W

Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
	—	—	—	—	—	—	—	TENDIE	—	—	—	NACKDIE	—	—	SPCNDDIE	STCNDDIE
Initial Value	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
R/W	R	R	R	R	R	R	R	R/W	R	R	R	R/W	R	R/W	R/W	R/W

Modified

Bit	Bit Name	Initial Value	R/W	Description
⋮				
20	TODIE	0b	R/W	Timeout Detection Interrupt Enable*1 0: Disables Timeout Detection Interrupt Signal. 1: Enables Timeout Detection Interrupt Signal.
19 to 17	—	All 0	R	Reserved This bit is read as 0. The write value should be 0.
16	ALIE	0b	R/W	Arbitration Lost Interrupt Enable*1 0: Disables Arbitration Lost Interrupt Signal. 1: Enables Arbitration Lost Interrupt Signal.
15 to 9	—	All 0	R	Reserved This bit is read as 0. The write value should be 0.
8	TENDIE	0b	R/W	Transmit End Interrupt Enable*1 0: Disables Transmit End Interrupt Signal. 1: Enables Transmit End Interrupt Signal.
7 to 5	—	000b	R	Reserved This bit is read as 0. The write value should be 0.
4	NACKDIE	0b	R/W	NACK Detection Interrupt Enable*1 0: Disables NACK Detection Interrupt Signal. 1: Enables NACK Detection Interrupt Signal.
3	—	0b	R	Reserved This bit is read as 0. The write value should be 0.
2	—	0b	R/W	Reserved This bit is read as 0. The write value should be 0.
1	SPCNDDIE	0b	R/W	STOP Condition Detection Interrupt Enable 0: Disables STOP condition Detection Interrupt Signal. 1: Enables STOP condition Detection Interrupt Signal.
0	STCNDDIE	0b	R/W	START Condition Detection Interrupt Enable 0: Disables START condition Detection Interrupt Signal. 1: Enables START condition Detection Interrupt Signal.

Modified (in red frames)

Note 1. This bit supports for I²C mode.

Modified

Before

26.2.44 Bus Interrupt Enable Register (BIE)

STCNDDIE bit (START Condition Detection Interrupt Enable)

This bit enables or disables the START Condition Detection interrupt requests when the BST.STCNDDF flag is set to 1.

SPCNDDIE bit (STOP Condition Detection Interrupt Enable)

This bit enables or disables the STOP Condition Detection interrupt requests when the BST.SPCNDDF flag is set to 1.

HDREXDIE bit (HDR Exit Pattern Detection Interrupt Enable)

This bit enables or disables the HDR Exit Pattern Detection interrupt requests when the BST.HDREXDF flag is set to 1.

NACKDIE bit (NACK Detection Interrupt Enable)

This bit enables or disables the NACK Detection interrupt requests when the BST.NACKDF flag is set to 1.

TENDIE bit (Transmit End Interrupt Enable)

This bit enables or disables the Transmit End interrupt (I3C_TEND) requests when the BST.TENDF flag is set to 1.

Deleted

After

26.2.44 Bus Interrupt Enable Register (BIE)

STCNDDIE bit (START Condition Detection Interrupt Enable)

This bit enables or disables the START Condition Detection interrupt requests when the BST.STCNDDF flag is set to 1.

SPCNDDIE bit (STOP Condition Detection Interrupt Enable)

This bit enables or disables the STOP Condition Detection interrupt requests when the BST.SPCNDDF flag is set to 1.

NACKDIE bit (NACK Detection Interrupt Enable)

This bit enables or disables the NACK Detection interrupt requests when the BST.NACKDF flag is set to 1.

TENDIE bit (Transmit End Interrupt Enable)

This bit enables or disables the Transmit End interrupt (I3C_TEND) requests when the BST.TENDF flag is set to 1.

Before

26.2.45 Bus Status Force Register (BSTFC)

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
	—	—	—	—	—	—	—	WUCNDDFC	—	—	—	TODFC	—	—	—	ALFC
Initial Value	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
R/W	R	R	R	R	R	R	R	W	R	R	R	W	R	R	R	W

Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
	—	—	—	—	—	—	—	TENDFC	—	—	—	NACKDFC	—	HDREXDFC	SPCNDDFC	STCNDDFC
Initial Value	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
R/W	R	R	R	R	R	R	R	W	R	R	R	W	R	W	W	W

Bit	Bit Name	Initial Value	R/W	Description
20	TODFC	0b	W	Timeout Detection Force*2 0: Not Force Timeout Detection Interrupt for software testing. 1: Force Timeout Detection Interrupt for software testing.
19 to 17	—	All 0	R	Reserved These bits are read as 0. The write value should be 0.
16	ALFC	0b	W	Arbitration Lost Force*2 0: Not Force Arbitration Lost Interrupt for software testing. 1: Force Arbitration Lost Interrupt for software testing.
15 to 9	—	All 0	R	Reserved These bits are read as 0. The write value should be 0.
8	TENDFC*3	0b	W	Transmit End Force*2 0: Not Force Transmit End Interrupt for software testing. 1: Force Transmit End Interrupt for software testing.
7 to 5	—	000b	R	Reserved These bits are read as 0. The write value should be 0.
4	NACKDFC	0b	W	NACK Detection Force*2 0: Not Force NACK Detection Interrupt for software testing. 1: Force NACK Detection Interrupt for software testing.
3	—	0b	R	Reserved These bits are read as 0. The write value should be 0.
2	HDREXDFC	0b	W	HDR Exit Pattern Detection Force*1 0: Not Force HDR Exit Pattern Detection Interrupt for software testing. 1: Force HDR Exit Pattern Detection Interrupt for software testing.
1	SPCNDDFC	0b	W	STOP condition Detection Force 0: Not Force STOP condition Detection Interrupt for software testing. 1: Force STOP condition Detection Interrupt for software testing.
0	STCNDDFC	0b	W	START condition Detection Force 0: Not Force START condition Detection Interrupt for software testing. 1: Force START condition Detection Interrupt for software testing.

Note 1. This bit supports for all I3C mode.
Note 2. This bit supports for I²C mode.
Note 3. TENDFC does not work unless TDBEF0 = 1.

Deleted

After

26.2.45 Bus Status Force Register (BSTFC)

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
	—	—	—	—	—	—	—	WUCNDDFC	—	—	—	TODFC	—	—	—	ALFC
Initial Value	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
R/W	R	R	R	R	R	R	R	W	R	R	R	W	R	R	R	W

Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
	—	—	—	—	—	—	—	TENDFC	—	—	—	NACKDFC	—	—	SPCNDDFC	STCNDDFC
Initial Value	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
R/W	R	R	R	R	R	R	R	W	R	R	R	W	R	W	W	W

Bit	Bit Name	Initial Value	R/W	Description
20	TODFC	0b	W	Timeout Detection Force*1 0: Not Force Timeout Detection Interrupt for software testing. 1: Force Timeout Detection Interrupt for software testing.
19 to 17	—	All 0	R	Reserved These bits are read as 0. The write value should be 0.
16	ALFC	0b	W	Arbitration Lost Force*1 0: Not Force Arbitration Lost Interrupt for software testing. 1: Force Arbitration Lost Interrupt for software testing.
15 to 9	—	All 0	R	Reserved These bits are read as 0. The write value should be 0.
8	TENDFC*2	0b	W	Transmit End Force*1 0: Not Force Transmit End Interrupt for software testing. 1: Force Transmit End Interrupt for software testing.
7 to 5	—	000b	R	Reserved These bits are read as 0. The write value should be 0.
4	NACKDFC	0b	W	NACK Detection Force*1 0: Not Force NACK Detection Interrupt for software testing. 1: Force NACK Detection Interrupt for software testing.
3	—	0b	R	Reserved These bits are read as 0. The write value should be 0.
2	—	0b	W	Reserved These bits are read as 0. The write value should be 0.
1	SPCNDDFC	0b	W	STOP condition Detection Force 0: Not Force STOP condition Detection Interrupt for software testing. 1: Force STOP condition Detection Interrupt for software testing.
0	STCNDDFC	0b	W	START condition Detection Force 0: Not Force START condition Detection Interrupt for software testing. 1: Force START condition Detection Interrupt for software testing.

Note 1. This bit supports for I²C mode.
Note 2. TENDFC does not work unless TDBEF0 = 1.

Modified

Modified (in red frames)

Before

26.2 Registers

26.2.54 Device Address Table Basic Register m (DATBASm) (m = 0 to 7)

DVSIRRJ bit (Device In-Band Slave Interrupt Request Reject)

Controls whether this Device, when operating in the Master role, will accept vs. reject Slave Interrupt Requests from other Devices.

DVMRRJ bit (Device In-Band Master Request Reject)

Controls whether this Device, when operating in the Master role, will accept vs. reject Master requests from other Devices. This bit is only valid if I3C declares Non-Current Master Capability.

DVIBITS bit (Device IBI Time-stamp)

Enables or disables IBI time-stamping for a specific Device.

Note: The IBI Status Descriptor for each IBI event indicates whether or not the individual IBI event was actually time- stamped. Set to 0 except for Async mode 0 and Async mode 1 of timing control.

DVNACK[1:0] bits (Device NACK Retry Count)

These bits set the number of retries when a NACK response is received from the slave for the transaction set in the Command Descriptor.

Note: When ENTDAA is executed by Address Assign Command, the setting of this bit is ignored and the transaction ends when NACK is received once.

After

26.2 Registers

26.2.54 Device Address Table Basic Register m (DATBASm) (m = 0 to 7)

DVSIRRJ bit (Device In-Band Slave Interrupt Request Reject)

Controls whether this Device, when operating in the Master role, will accept vs. reject Slave Interrupt Requests from other Devices.

DVMRRJ bit (Device In-Band Master Request Reject)

Controls whether this Device, when operating in the Master role, will accept vs. reject Master requests from other Devices. This bit is only valid if I3C declares Non-Current Master Capability.

DVIBITS bit (Device IBI Time-stamp)

Enables or disables IBI time-stamping for a specific Device.

Note: The IBI Status Descriptor for each IBI event indicates whether or not the individual IBI event was actually time- stamped. Set to 0 except for Async mode 0 and Async mode 1 of timing control.

DVNACK[1:0] bits (Device NACK Retry Count)

These bits set the number of retries when a NACK response is received from the slave for the transaction set in the Command Descriptor.

Modified

Note 1. When ENTDAA is executed by Address Assign Command, the setting of this bit is ignored and the transaction ends when NACK is received once.

Note 2: I3C will retry according to the setting of DVNACK[1:0], even if it receives a NACK for the broadcast address.

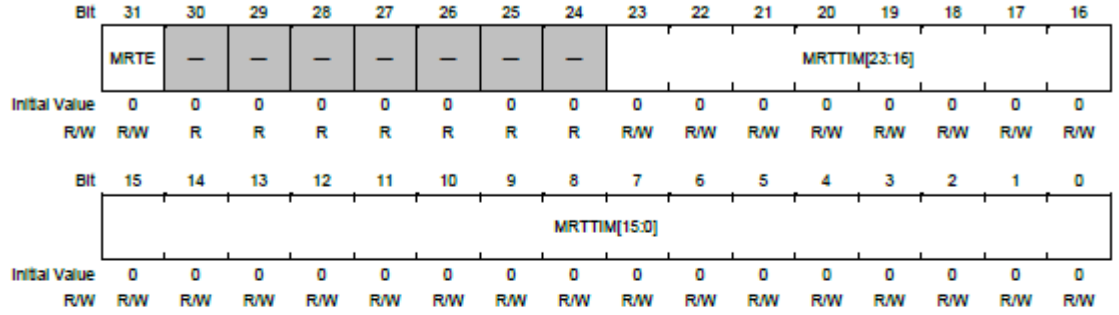
Note 3. If DVNACK[1:0] is 00b, I3C will not retry even for Direct CCCs.

Addition

Before

26.2 Registers

26.2.70 CCC Max Data Speed T (Turnaround) Register (CMDSPT)



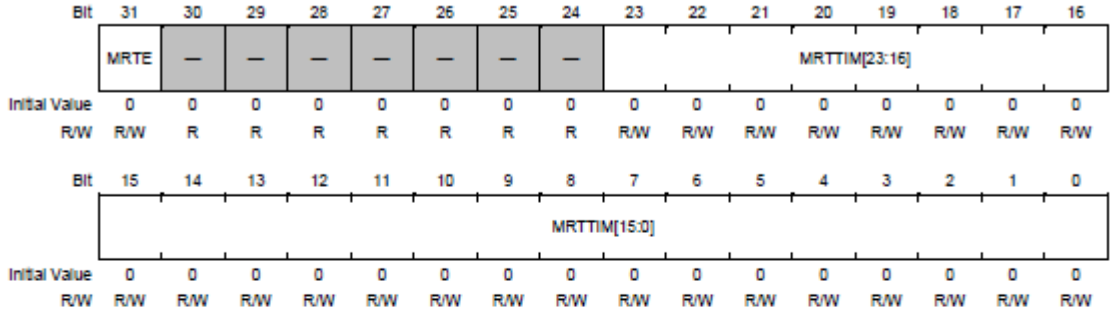
Bit	Bit Name	Initial Value	R/W	Description
31	MRTE	0b	R/W	Maximum Read Turnaround Time Enable 0: Disables transmission of the Maximum Read Turnaround Time. (GETMXDS Format 1: Without Turnaround) 1: Enables transmission of the Maximum Read Turnaround Time. (GETMXDS Format 2: With Turnaround)
30 to 24	—	All 0	R	Reserved These bits are read as 0. The write value should be 0.
23 to 0	MRTTIM [23:0]	All 0	R/W	Maximum Read Turnaround Time 24-bit field can encode turnaround times from 0.0 seconds to 16 seconds. H'F4_0000: 0 µs (minimum value) H'F4_0001: 1 µs (resolution) ⋮ H'F4_2400: 16 seconds (maximum value) H'F4_2401: Setting prohibited ⋮ H'FF_FFFF: Setting prohibited

Note: This register supports for I3C secondary master mode and I3C slave mode.

After

26.2 Registers

26.2.70 CCC Max Data Speed T (Turnaround) Register (CMDSPT)



Bit	Bit Name	Initial Value	R/W	Description
31	MRTE	0b	R/W	Maximum Read Turnaround Time Enable 0: Disables transmission of the Maximum Read Turnaround Time. (GETMXDS Format 1: Without Turnaround) 1: Enables transmission of the Maximum Read Turnaround Time. (GETMXDS Format 2: With Turnaround)
30 to 24	—	All 0	R	Reserved These bits are read as 0. The write value should be 0.
23 to 0	MRTTIM [23:0]	All 0	R/W	Maximum Read Turnaround Time 24-bit field can encode turnaround times from 0.0 seconds to 16 seconds. H'00_0000: 0 µs (minimum value) H'00_0001: 1 µs (resolution) ⋮ H'F4_2400: 16 seconds (maximum value) H'F4_2401: Setting prohibited ⋮ H'FF_FFFF: Setting prohibited

Modified

Note: This register supports for I3C secondary master mode and I3C slave mode.

Before

26.2 Registers

26.2.73 Bit Count Register (BITCNT)

Table 26.9 I3C transfer

	SDR*1		HDR-DDR		
BCNT[4:0]	Transmission	Reception	Command/Data	CRC	HDR-TS
H'00	1 bit	2 to 1 bits	19, 1 bits	11, 1 bits	1 Symbol
H'01	2 bits	3 bits	20, 2 bits	12, 2 bits	2 Symbols
H'02	3 bits	4 bits	3 bits	3 bits	3 Symbols
H'03	4 bits	5 bits	4 bits	4 bits	4 Symbols
H'04	5 bits	6 bits	5 bits	5 bits	5 Symbols
H'05	6 bits	7 bits	6 bits	6 bits	6 Symbols
H'06	7 bits	8 bits	7 bits	7 bits	7 Symbols
H'07	8 bits	9 bits	8 bits	8 bits	8 Symbols
H'08	9 bits	—	9 bits	9 bits	9 Symbols
H'09	—	—	10 bits	10 bits	10 Symbols
H'0A	—	—	11 bits	—	11 Symbols
H'0B	—	—	12 bits	—	12 Symbols
H'0C	—	—	13 bits	—	—
H'0D	—	—	14 bits	—	—
H'0E	—	—	15 bits	—	—
H'0F	—	—	16 bits	—	—
H'10	—	—	17 bits	—	—
H'11	—	—	18 bits	—	—

Note 1. The address phase is the same as in **Table 26.8**.

Deleted

After

26.2 Registers

26.2.73 Bit Count Register (BITCNT)

Table 26.9 I3C transfer

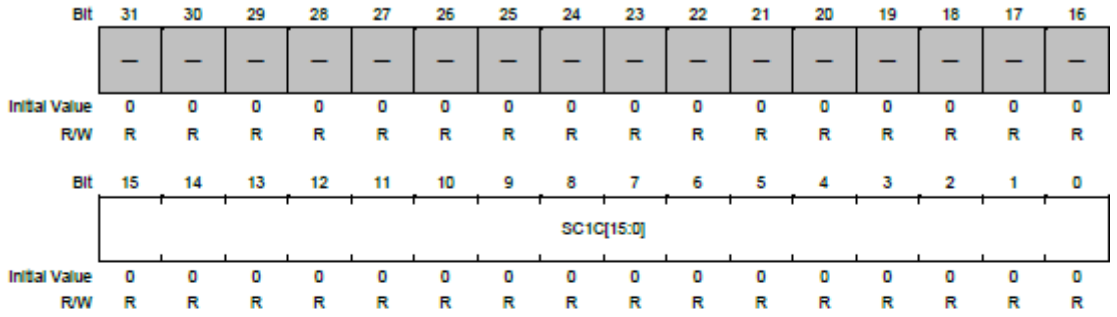
	SDR*1	
BCNT[4:0]	Transmission	Reception
H'00	1 bit	2 to 1 bits
H'01	2 bits	3 bits
H'02	3 bits	4 bits
H'03	4 bits	5 bits
H'04	5 bits	6 bits
H'05	6 bits	7 bits
H'06	7 bits	8 bits
H'07	8 bits	9 bits
H'08	9 bits	—
H'09	—	—
H'0A	—	—
H'0B	—	—
H'0C	—	—
H'0D	—	—
H'0E	—	—
H'0F	—	—
H'10	—	—
H'11	—	—

Note 1. The address phase is the same as in **Table 26.8**.

Before

26.2 Registers

26.2.79 SC1 Capture monitor Register (SC1CPT)



Bit	Bit Name	Initial Value	R/W	Description
31 to 16	—	All 0	R	Reserved These bits are read as 0.
15 to 0	SC1C[15:0]	All 0	R	SC1 Capture

Note: This register supports for all I3C mode.

SC1C[15:0] Bits

- Async Mode 0 (Asynchronous Basic Mode)

  After enabling ATCCNTE.ATCE, SC1 Counter counts up from SC1 count trigger*1 to SCL rise edge next to ACK for the IBI and capture it as SC1.

- Async Mode 1 (Asynchronous Advanced Mode)

  After enabling ATCCNTE.ATCE, SC1 Counter counts up from SC1 count trigger*1 to the first aME and capture it as SC1.

Note 1. SW or external trigger can be selected by selection bits.

Deleted

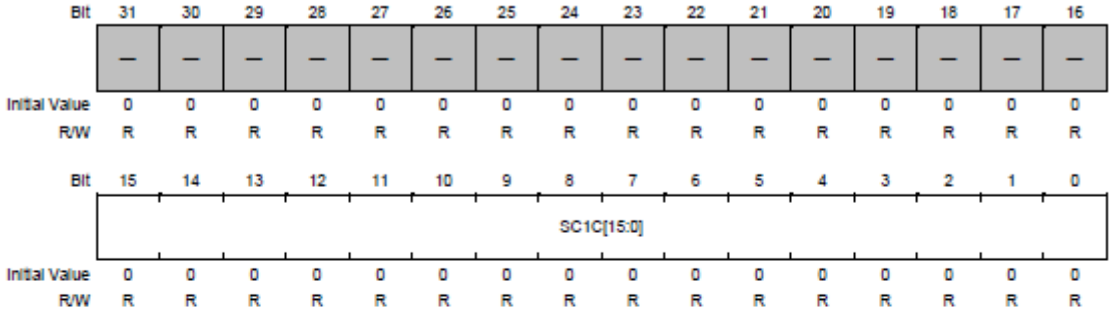
CAUTION

As the timing control specification, the SC1 counter value is included in the IBI frame as IBI data and is sent to I3C Master, therefore it is not necessary for the I3C Slave to read this register. If the I3C Slave needs to read this register, read it after completing the IBI frame.

After

26.2 Registers

26.2.79 SC1 Capture monitor Register (SC1CPT)



Bit	Bit Name	Initial Value	R/W	Description
31 to 16	—	All 0	R	Reserved These bits are read as 0.
15 to 0	SC1C[15:0]	All 0	R	SC1 Capture

Note: This register supports for all I3C mode.

SC1C[15:0] Bits

- Async Mode 0 (Asynchronous Basic Mode)

  After enabling ATCCNTE.ATCE, SC1 Counter counts up from SC1 count trigger to SCL rise edge next to ACK for the IBI and capture it as SC1.

- Async Mode 1 (Asynchronous Advanced Mode)

  After enabling ATCCNTE.ATCE, SC1 Counter counts up from SC1 count trigger to the first aME and capture it as SC1.

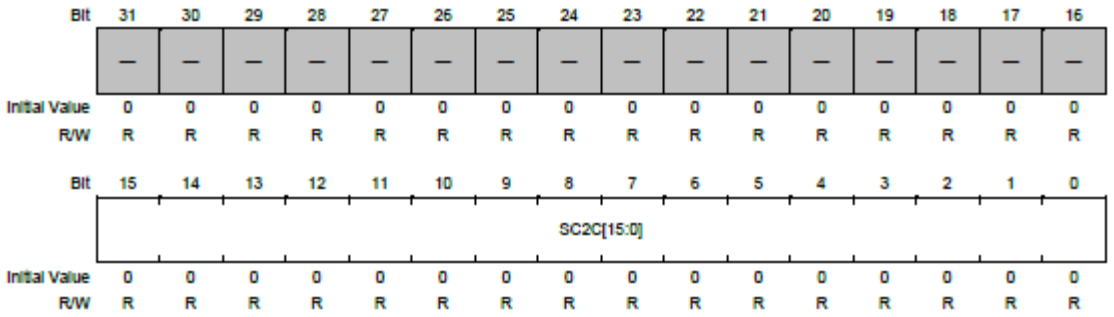
CAUTION

As the timing control specification, the SC1 counter value is included in the IBI frame as IBI data and is sent to I3C Master, therefore it is not necessary for the I3C Slave to read this register. If the I3C Slave needs to read this register, read it after completing the IBI frame.

Before

26.2 Registers

26.2.80 SC2 Capture monitor Register (SC2CPT)



Bit	Bit Name	Initial Value	R/W	Description
31 to 16	—	All 0	R	Reserved These bits are read as 0.
15 to 0	SC2C[15:0]	All 0	R	SC2 Capture

Note: This register supports for all I3C mode.

SC2C[15:0] Bits

- Async Mode 0 (Asynchronous Basic Mode)

After enabling ATCCNTE.ATCE, SC2 Counter counts up from SC2 count trigger*1 to SCL rise edge next to ACK for the IBI and capture it as SC2.

- Async Mode 1 (Asynchronous Advanced Mode)

After enabling ATCCNTE.ATCE, SC2 Counter counts up from SC2 count trigger*1 to the first aME and capture it as SC2.

Note 1. SW or external trigger can be selected by selection bits.

Deleted

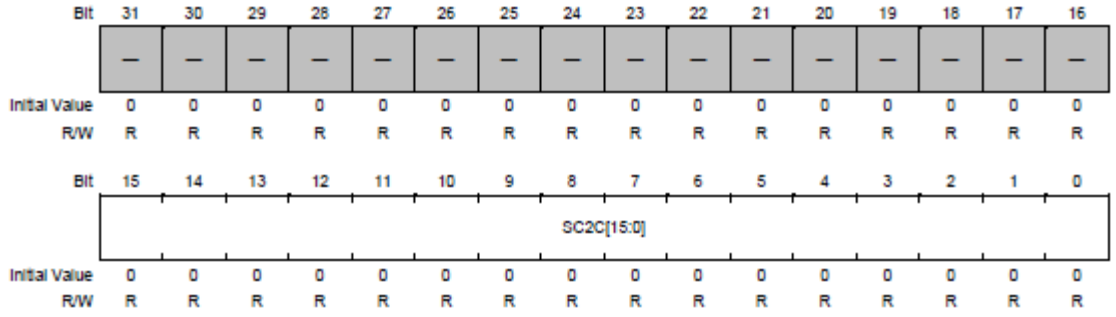
CAUTION

As the timing control specification, the SC2 counter value is included in the IBI frame as IBI data and is sent to I3C Master, therefore it is not necessary for the I3C Slave to read this register. If the I3C Slave needs to read this register, read it after completing the IBI frame.

After

26.2 Registers

26.2.80 SC2 Capture monitor Register (SC2CPT)



Bit	Bit Name	Initial Value	R/W	Description
31 to 16	—	All 0	R	Reserved These bits are read as 0.
15 to 0	SC2C[15:0]	All 0	R	SC2 Capture

Note: This register supports for all I3C mode.

SC2C[15:0] Bits

Modified

- Async Mode 0 (Asynchronous Basic Mode)

After enabling ATCCNTE.ATCE, SC2 Counter counts up from SCL rise edge next to ACK for the IBI transmitted from I3C Slave to SCL rise edge next to Tbit after Mandatory Byte, and capture it as SC2.

- Async Mode 1 (Asynchronous Advanced Mode)

After enabling ATCCNTE.ATCE, SC2 Counter counts up from SCL rise edge next to ACK for the IBI transmitted from I3C Slave to SCL rise edge next to Tbit after Mandatory Byte, and capture it as SC2

Modified

CAUTION

As the timing control specification, the SC2 counter value is included in the IBI frame as IBI data and is sent to I3C Master, therefore it is not necessary for the I3C Slave to read this register. If the I3C Slave needs to read this register, read it after completing the IBI frame.

Before

26.3.2.1 Operation Mode

(1) Master Mode Operation

(b) I3C Master Operation

2) SDR Data Write Transfer

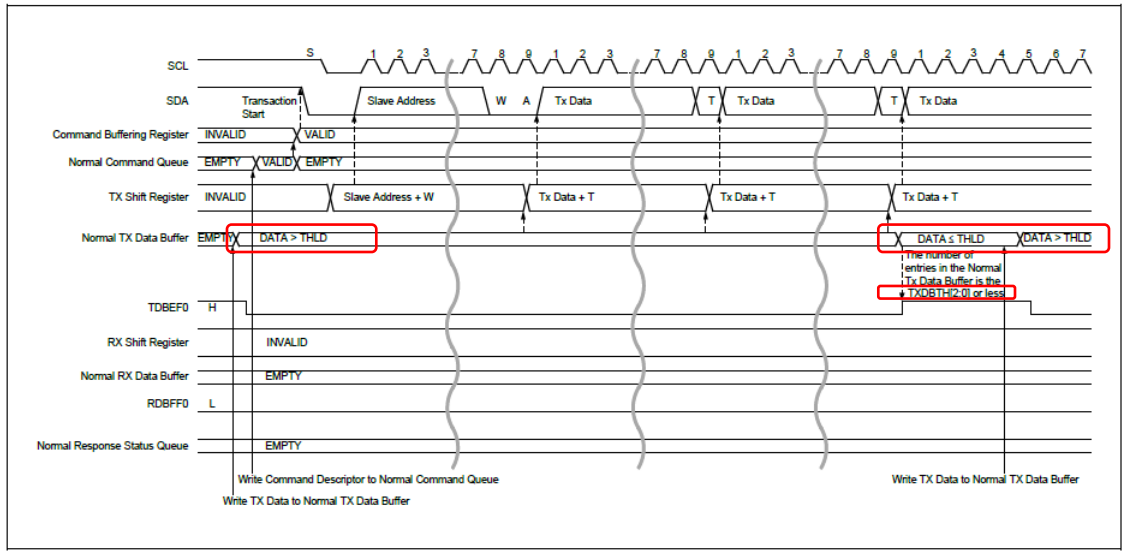


Figure 26.16 SDR Data Write Transfer Timing (1/2)

After

26.3.2.1 Operation Mode

(1) Master Mode Operation

(b) I3C Master Operation

2) SDR Data Write Transfer

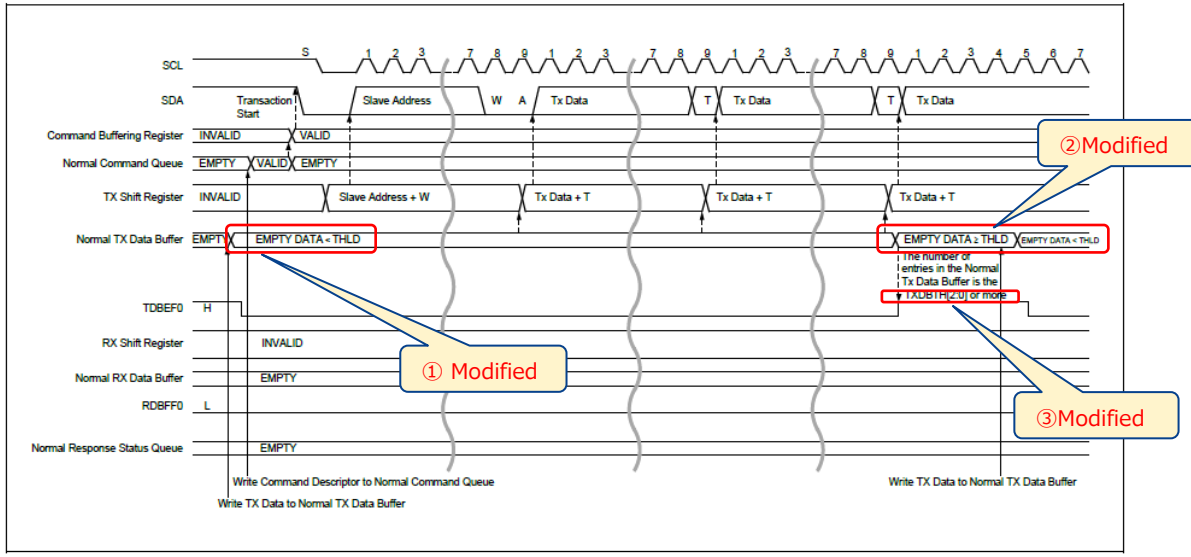


Figure 26.16 SDR Data Write Transfer Timing (1/2)

Before

26.3.2.1 Operation Mode

(1) Master Mode Operation

(b) I3C Master Operation

2) SDR Data Write Transfer

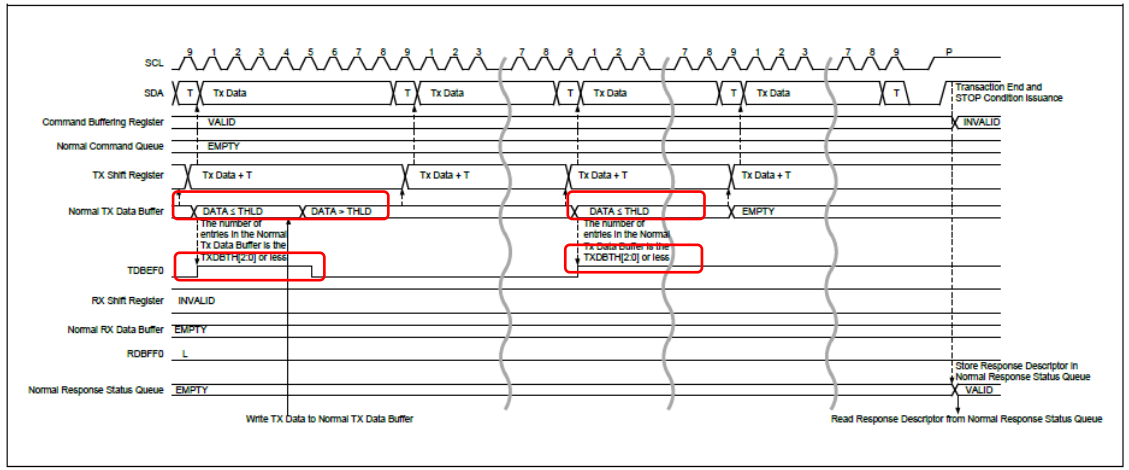


Figure 26.17 SDR Data Write Transfer Timing (2/2)

After

26.3.2.1 Operation Mode

(1) Master Mode Operation

(b) I3C Master Operation

2) SDR Data Write Transfer

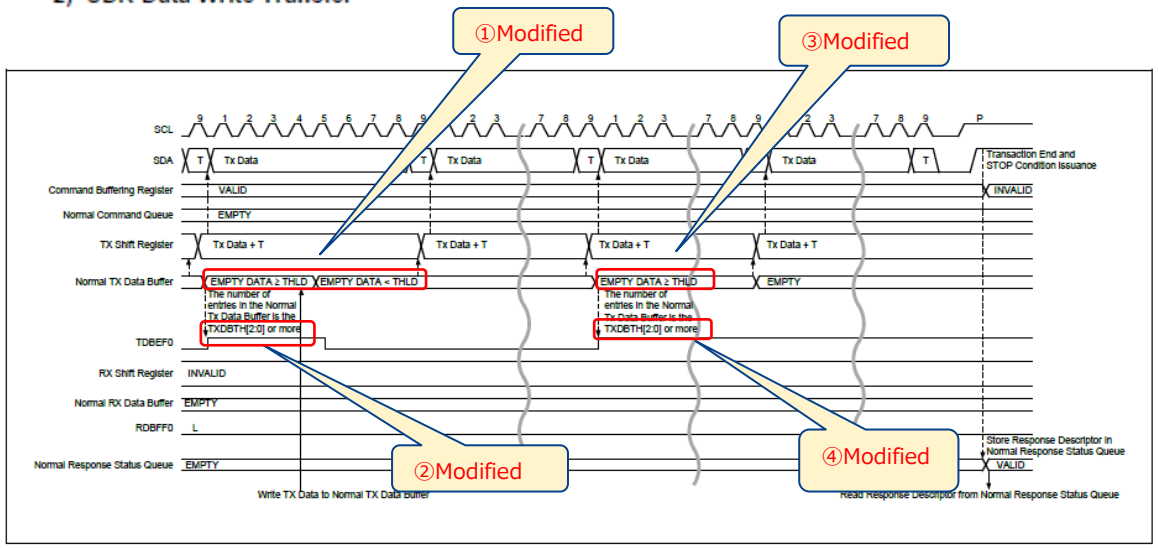


Figure 26.17 SDR Data Write Transfer Timing (2/2)

Before

26.3.2.1 Operation Mode

(1) Master Mode Operation

(b) I3C Master Operation

2) SDR Data Write Transfer

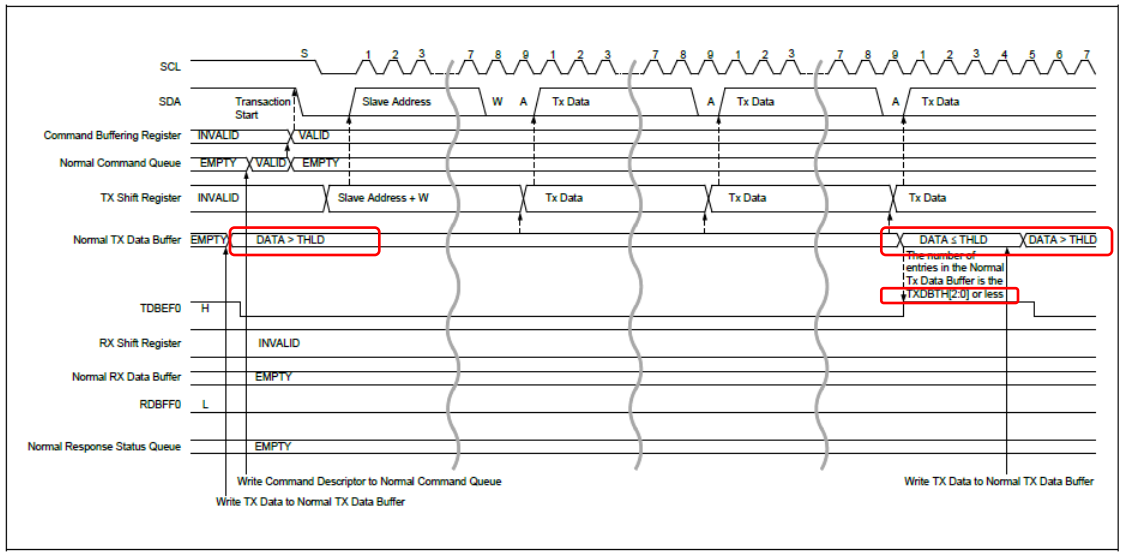


Figure 26.18 Legacy I²C Message Data Write Timing (1/2)

After

26.3.2.1 Operation Mode

(1) Master Mode Operation

(b) I3C Master Operation

2) SDR Data Write Transfer

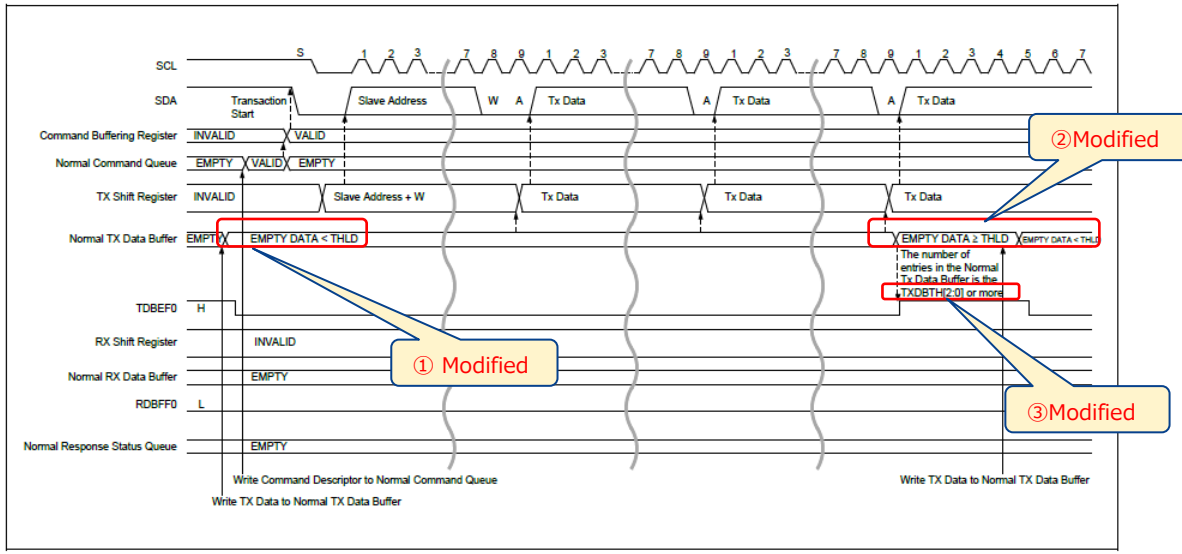


Figure 26.18 Legacy I²C Message Data Write Timing (1/2)

Before

26.3.2.1 Operation Mode

(1) Master Mode Operation

(b) I3C Master Operation

2) SDR Data Write Transfer

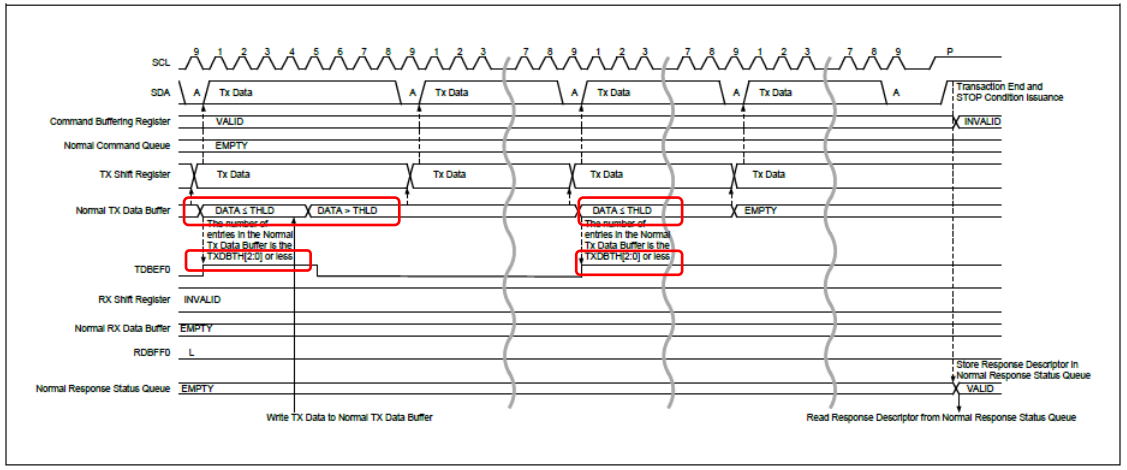


Figure 26.19 Legacy I²C Message Data Write Timing (2/2)

After

26.3.2.1 Operation Mode

(1) Master Mode Operation

(b) I3C Master Operation

2) SDR Data Write Transfer

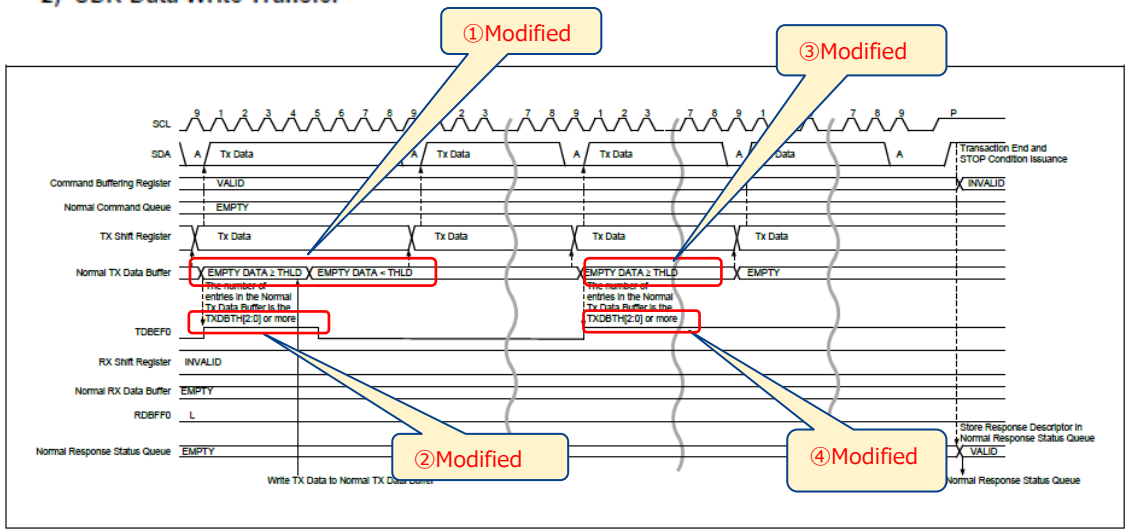


Figure 26.19 Legacy I²C Message Data Write Timing (2/2)

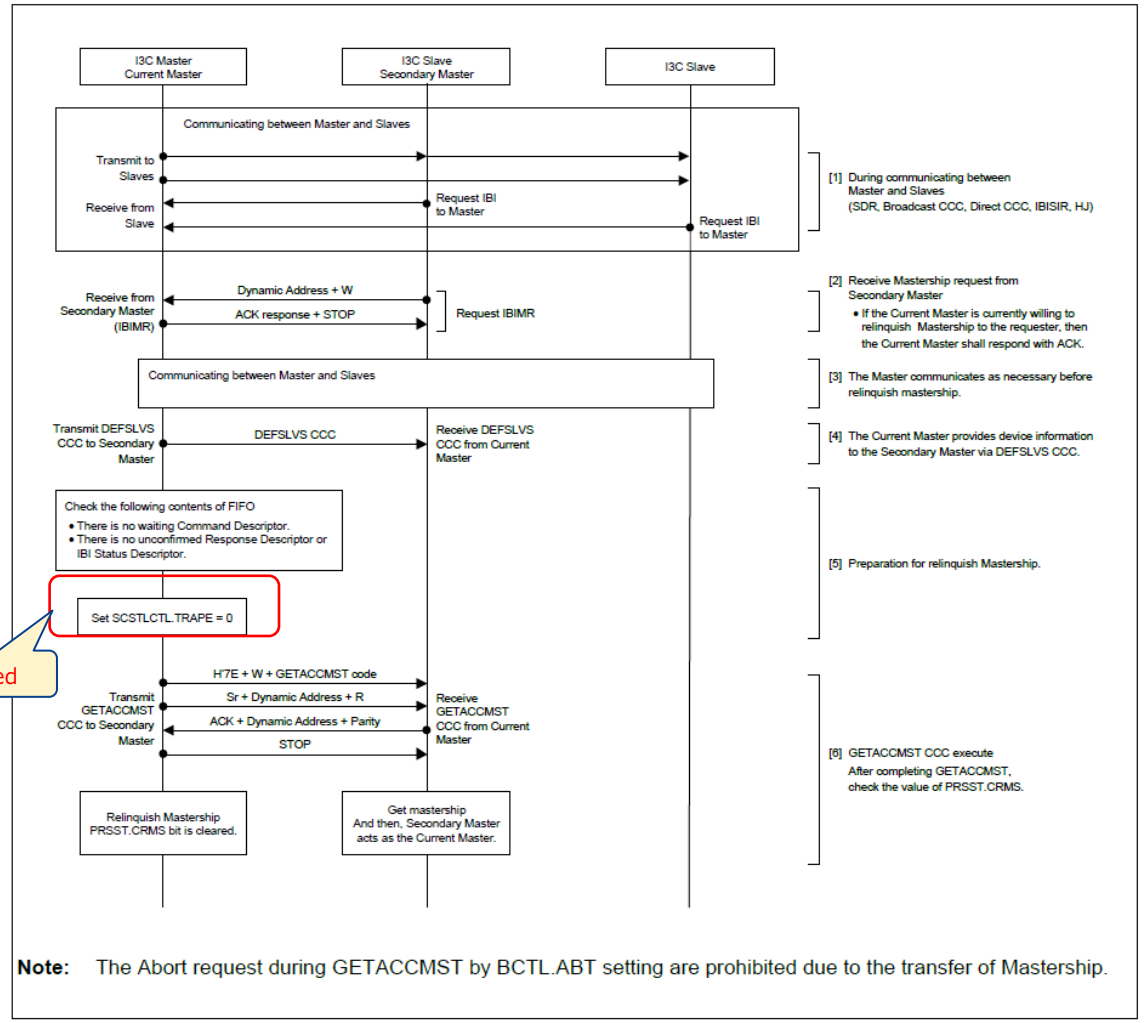
Before

26.3.2 Details of Function

26.3.2.1 Operation Mode

(b) I3C Master Operation

4) IBI Transfer



Note: The Abort request during GETACCMST by BCTL.ABT setting are prohibited due to the transfer of Mastership.

Figure 26.26 I3C Master Mastership Processing Flow

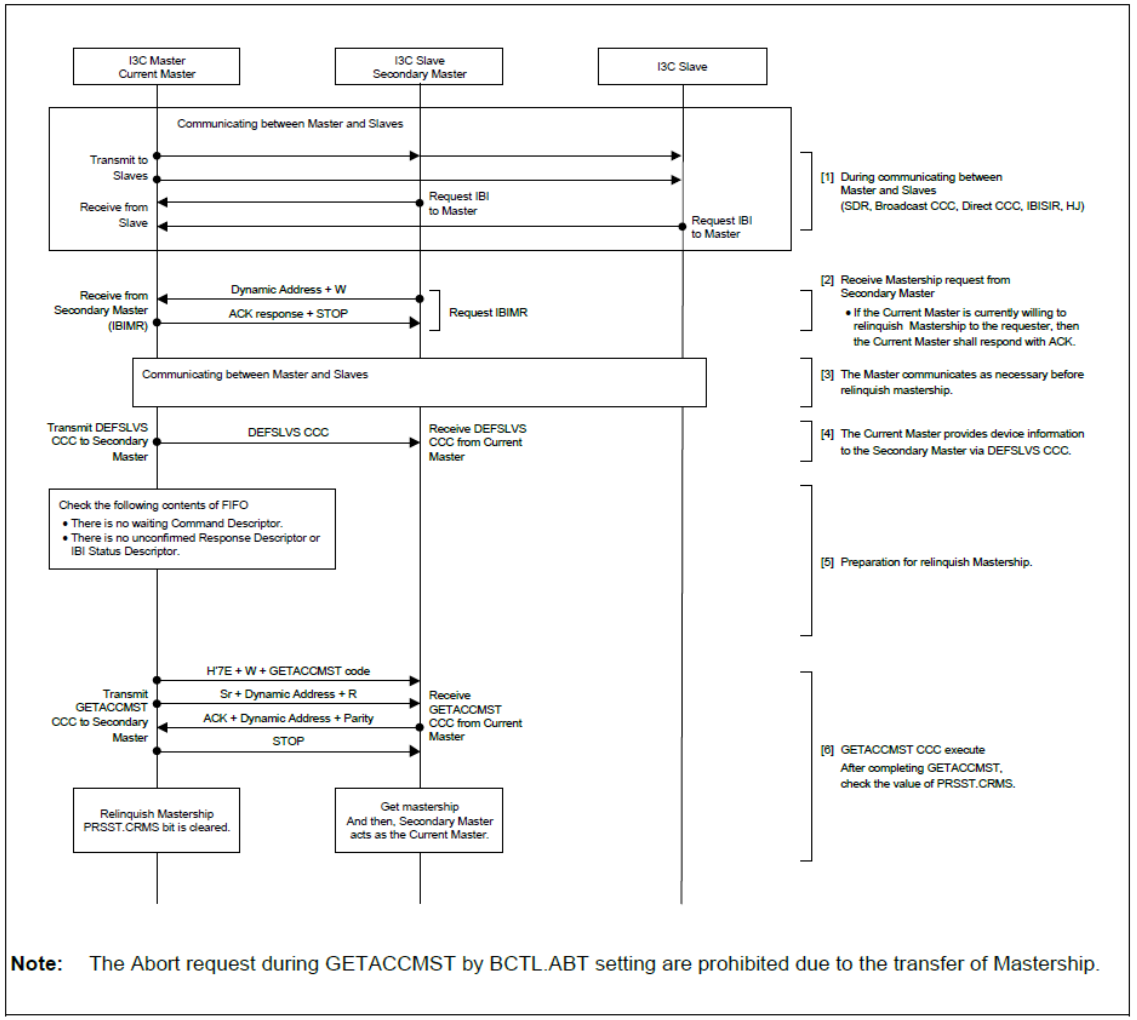
After

26.3.2 Details of Function

26.3.2.1 Operation Mode

(b) I3C Master Operation

4) IBI Transfer



Note: The Abort request during GETACCMST by BCTL.ABT setting are prohibited due to the transfer of Mastership.

Figure 26.26 I3C Master Mastership Processing Flow

Before

26.3.2.1 Operation Mode

(2) Slave Mode Operation

(a) I²C Slave Operation

2) Data Read Transfer (Single Buffer transfer)

1. Initial settings. For details, refer to **Section 26.3.3.1, Initial Setting Flow**.
   After initial settings, I3C will stay in the standby state until it receives a slave address that it matches.
2. After receiving a matching slave address, I3C sets one of the corresponding bits SVST.HOAF, GCAF, and SVAFy (y = 0 to 2) to 1 on the rising edge of the ninth cycle of SCL clock (the clock signal) and outputs the acknowledge bit (ACK) on the ninth cycle of SCL clock. If the value of the R/W# bit that was also received at this time is 1, I3C automatically places itself in slave transmit mode by setting both the PRSST.TRMD bit and the NTST.TDBEF0 flag to 1.
3. After the NTST.TDBEF0 flag is confirmed to be 1, write the data for transmission to the NTDTBP0 register. At this time, if I3C does not receive acknowledge from the master device (receives an NACK signal) while the BSTE.NACKDE bit = 1, I3C aborts transfer of the next data.
4. Wait until the following (a) or (b) condition.
   (a) The BST.NACKDF flag is set to 1.
   (b) The BST.TENDF flag is set to 1 while the NTST.TDBEF0 flag = 1, after the last byte for transmission is written to the NTDTBP0 register.

   When the BST.NACKDF flag or the TENDF flag = 1, I3C drives the SCLn line low on the ninth falling edge of SCL clock.
5. When the BST.NACKDF flag or the BST.TENDF flag = 1, dummy read the NTDTBP0 register to complete t processing. This releases the SCLn line.
6. Upon detecting the STOP condition, I3C automatically sets bits SVST.HOAF, GCAF, and SVAFy (y = 0 to 2), flags NTST.TDBEF0 and BST.TE DF, and the PRSST.TRMD bit to 0, and enters slave receive mode.
7. After checking that the BST.SPCN F flag = 1, set the BST.NACKDF and SPCNDDF flags to 0 for the next transfer operation.

Deleted

Deleted

After

26.3.2.1 Operation Mode

(2) Slave Mode Operation

(a) I²C Slave Operation

2) Data Read Transfer (Single Buffer transfer)

1. Initial settings. For details, refer to **Section 26.3.3.1, Initial Setting Flow**.
   After initial settings, I3C will stay in the standby state until it receives a slave address that it matches.
2. After receiving a matching slave address, I3C sets one of the corresponding bits SVST.HOAF, GCAF, and SVAFy (y = 0 to 2) to 1 on the rising edge of the ninth cycle of SCL clock (the clock signal) and outputs the acknowledge bit (ACK) on the ninth cycle of SCL clock. If the value of the R/W# bit that was also received at thi time is 1, I3C automatically places itself in slave transmit mode by setting both the PRSST.TRMD bit and the NTST.TDBEF0 flag to 1.
3. After the NTST.TDBEF0 flag is confirmed to be 1, write the data for transmission to the NTDTBP0 register. At this time, if I3C does not receive acknowledge from the master device (receives an NACK signal) while the BSTE.NACKDE bit = 1, I3C aborts transfer of the next data.
4. Wait until the following (a) or (b) condition.
   (a) The BST.NACKDF flag is set to 1.
   (b) The BST.TENDF flag is set to 1 while the NTST.TDBEF0 flag = 1, after the last byte for transmission is written to the NTDTBP0 register.
5. When the BST.NACKDF flag or the BST.TENDF flag = 1, dummy read the NTDTBP0 register to complete the processing.
6. Upon detecting the STOP condition, I3C automatically sets bits SVST.HOAF, GCAF, and SVAFy (y = 0 to 2), flags NTST.TDBEF0 and BST.TENDF, and the PRSST.TRMD bit to 0, and enters slave receive mode.
7. After checking that the BST.SPCNDDF flag = 1, set the BST.NACKDF and SPCNDDF flags to 0 for the next transfer operation.

Before

26.3.2.1 Operation Mode

(2) Slave Mode Operation

(a) I²C Slave Operation

2) Data Read Transfer (Single Buffer transfer)

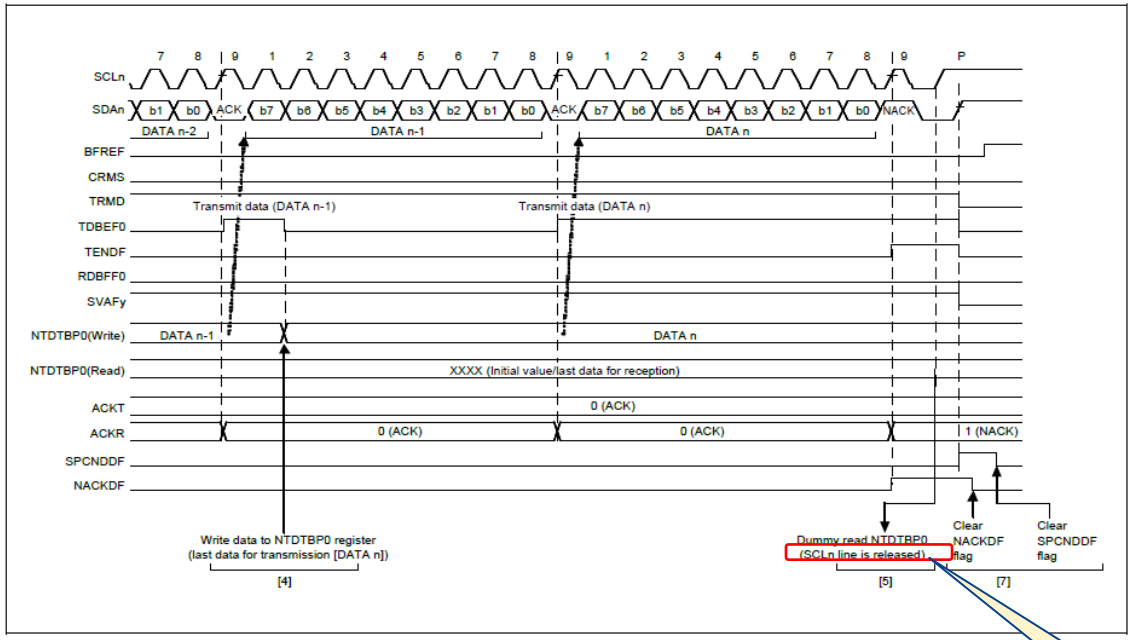


Figure 26.30 Slave Transmit Operation Timing (2)

After

26.3.2.1 Operation Mode

(2) Slave Mode Operation

(a) I²C Slave Operation

2) Data Read Transfer (Single Buffer transfer)

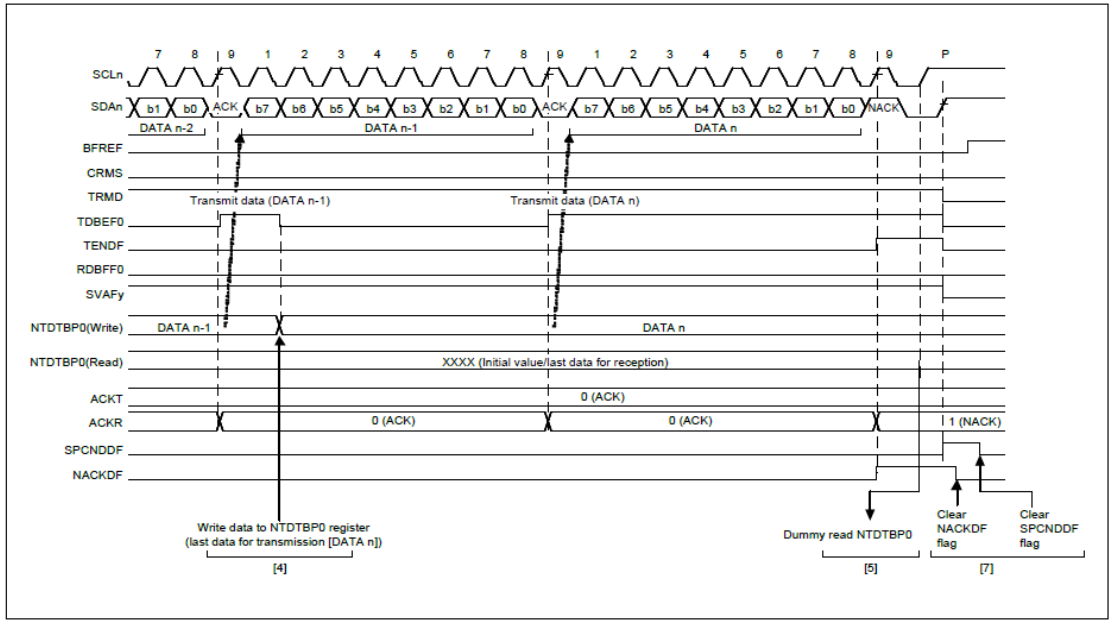


Figure 26.30 Slave Transmit Operation Timing (2)

Before

26.3.2.1 Operation Mode

(2) Slave Mode Operation

(b) I3C Slave Operation

3) SDR Data Read Transfer

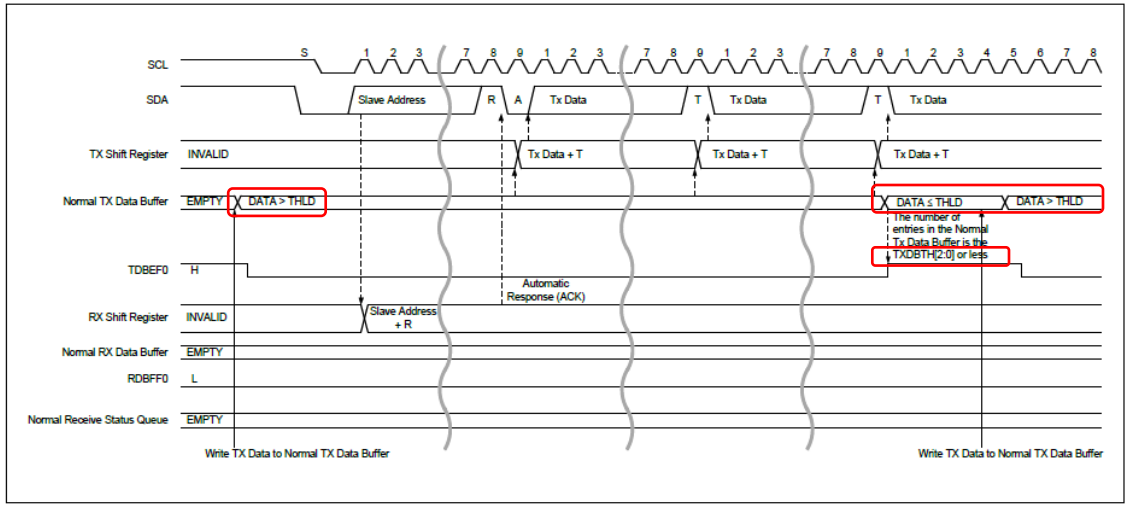


Figure 26.41 SDR Data Read Transfer Timing (1/2)

After

26.3.2.1 Operation Mode

(2) Slave Mode Operation

(b) I3C Slave Operation

3) SDR Data Read Transfer

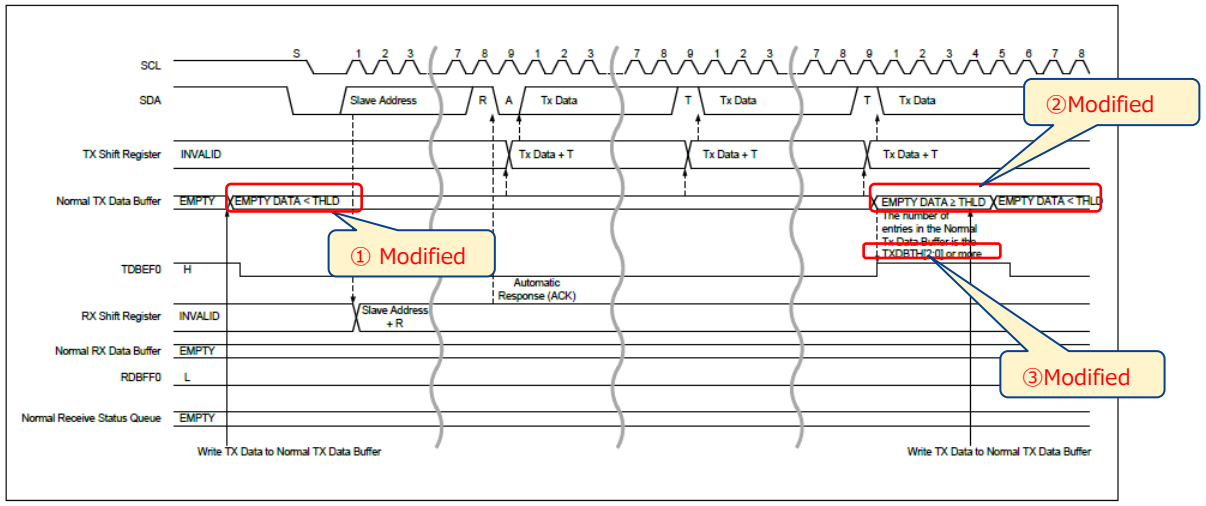


Figure 26.41 SDR Data Read Transfer Timing (1/2)

Before

26.3.2.1 Operation Mode

(2) Slave Mode Operation

(b) I3C Slave Operation

3) SDR Data Read Transfer

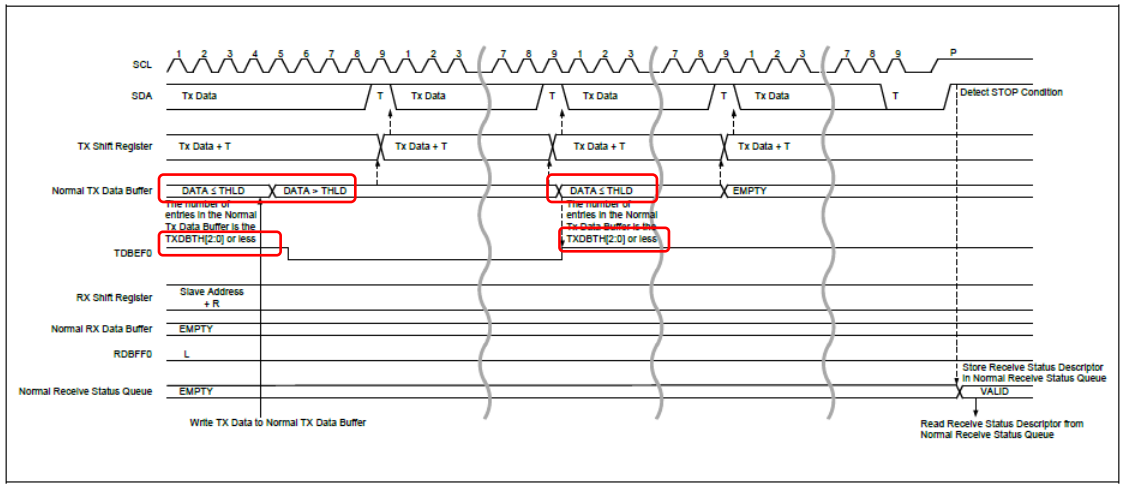


Figure 26.42 SDR Data Read Transfer Timing (2/2)

After

(2) Slave Mode Operation

(b) I3C Slave Operation

3) SDR Data Read Transfer

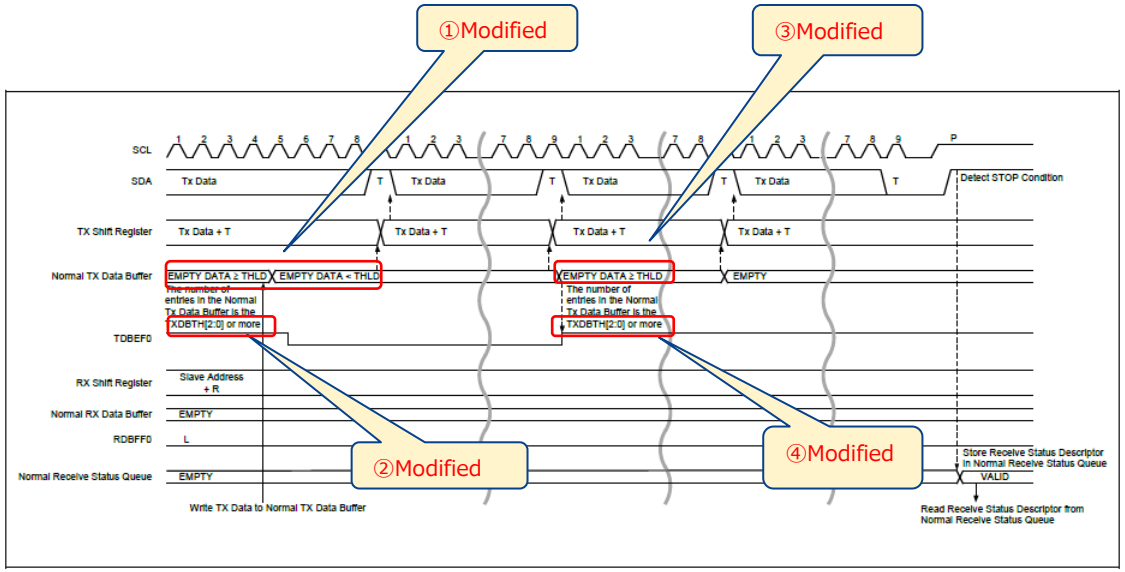


Figure 26.42 SDR Data Read Transfer Timing (2/2)

Before

26.3.2.1 Operation Mode

(2) Slave Mode Operation

(b) I3C Slave Operation

3) SDR Data Read Transfer

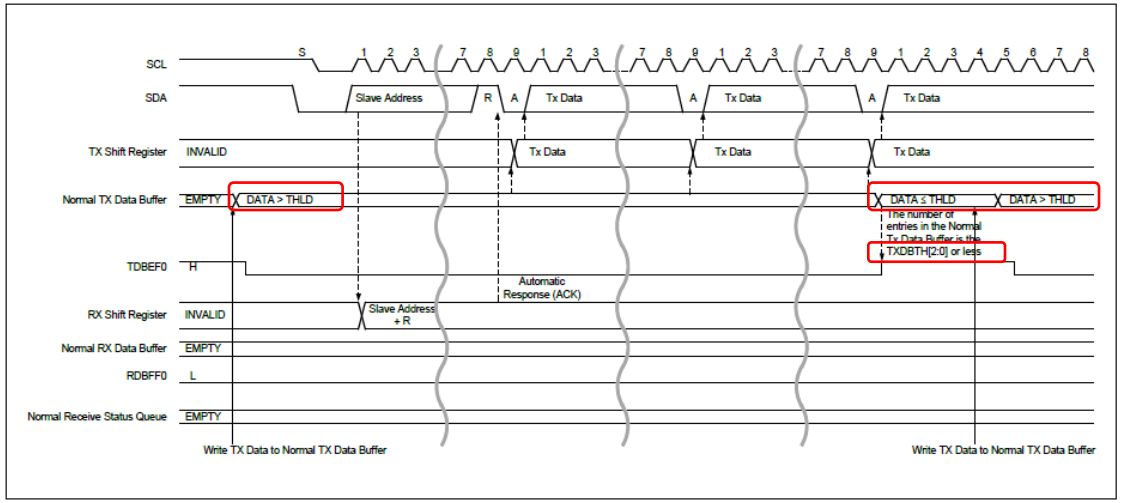


Figure 26.43 Legacy I²C Message Data Read Transfer Timing (1/2)

After

(2) Slave Mode Operation

(b) I3C Slave Operation

3) SDR Data Read Transfer

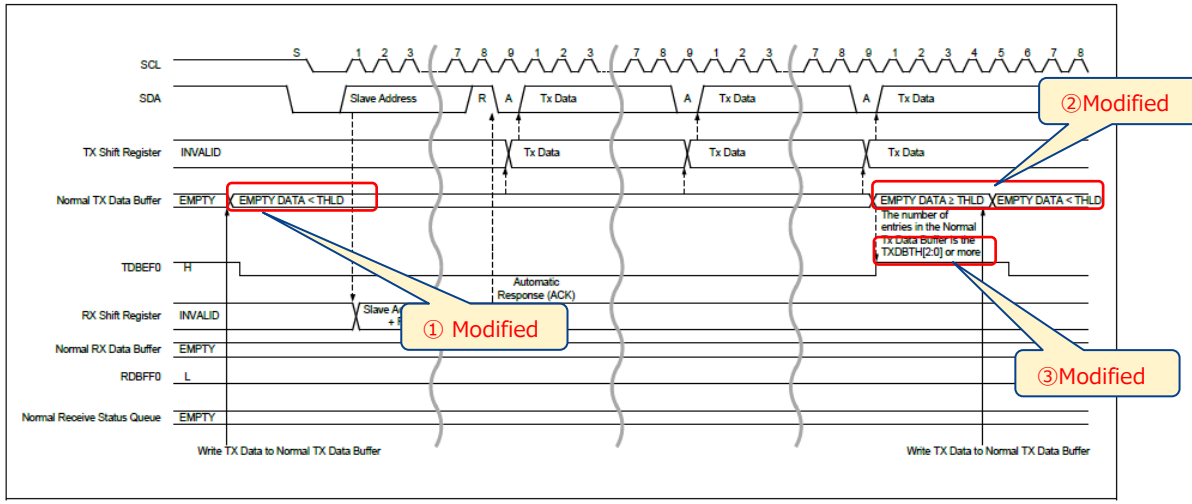


Figure 26.43 Legacy I²C Message Data Read Transfer Timing (1/2)

Before

26.3.2.1 Operation Mode

(2) Slave Mode Operation

(b) I3C Slave Operation

3) SDR Data Read Transfer

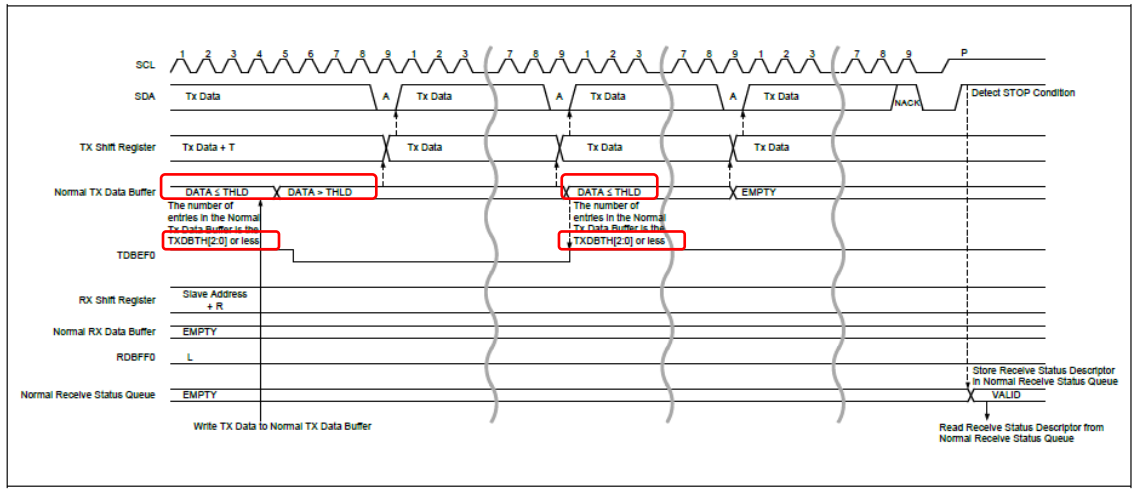


Figure 26.44 Legacy I²C Message Data Read Transfer Timing (2/2)

After

(2) Slave Mode Operation

(b) I3C Slave Operation

3) SDR Data Read Transfer

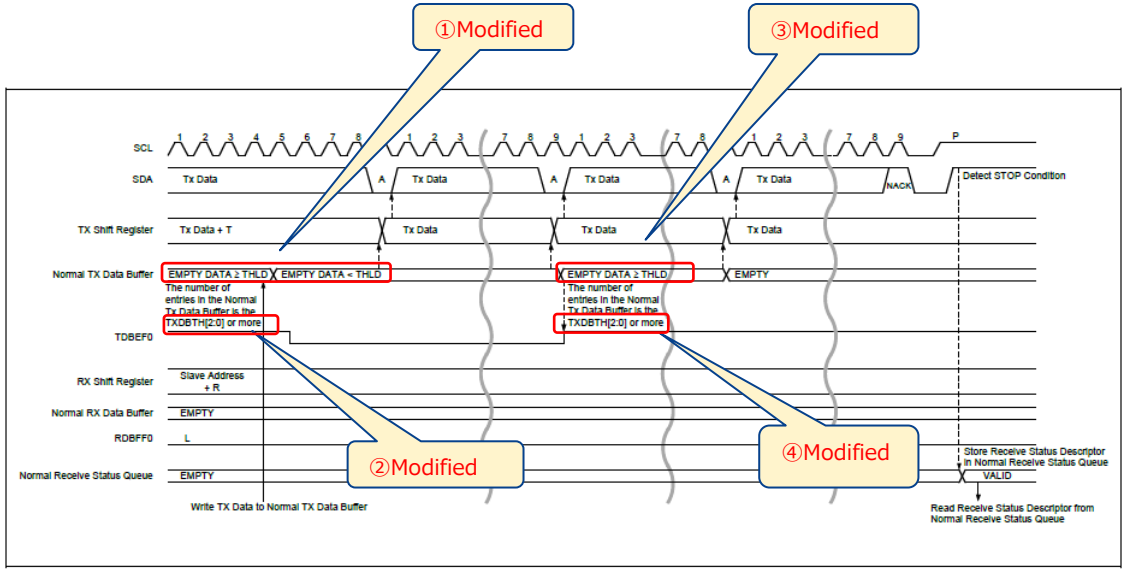


Figure 26.44 Legacy I²C Message Data Read Transfer Timing (2/2)

Before

26.3.2.1 Operation Mode

(2) Slave Mode Operation

(b) I3C Slave Operation

4) IBI Transfer

1. When sending Slave Interrupt Request.
   When transmitting IBI Data, write IBI Data to the IBI Data Buffer via the NIBIQP register.
2. Write Command Descriptor (Immediate Transfer Command or Regular Transfer Command) to the Command Buffer for IBI Transfer via the NCMDQP register.
3. When Command Descriptor is written to Command Buffer, IBI Transaction is issued under the following conditions.
   - Detect a START condition. (Does not apply a Repeated START condition)
   - If no START is forthcoming within the following Bus Condition, then this module issue a START Request by pulling the SDA line Low.
     a) Slave Interrupt Request, Mastership Request: Bus Available
     b) Hot-Join Event: Bus Idle
4. In Slave Address with RnW of the Address Header, if losing Arbitration by issuing a Transaction from I3C Master, stop issuing Transaction.
   When detecting Repeated START condition or STOP condition, store the Response Descriptor into the Response Buffer.

After

26.3.2.1 Operation Mode

(2) Slave Mode Operation

(b) I3C Slave Operation

4) IBI Transfer

1. When sending Slave Interrupt Request.
   When transmitting IBI Data, write IBI Data to the IBI Data Buffer via the NIBIQP register.
2. Write Command Descriptor (Immediate Transfer Command or Regular Transfer Command) to the Command Buffer for IBI Transfer via the NCMDQP register.
3. When Command Descriptor is written to Command Buffer, IBI Transaction is issued under the following conditions.
   - When START condition is detected in Slave Interrupt Request or Mastership Request. (Does not apply a Repeated START condition)
   - If no START is forthcoming within the following Bus Condition, then this module issue a START Request by pulling the SDA line Low.
     a) Slave Interrupt Request, Mastership Request: Bus Available
     b) Hot-Join Event: Bus Idle
4. In Slave Address with RnW of the Address Header, if losing Arbitration by issuing a Transaction from I3C Master, stop issuing Transaction.
   When detecting Repeated START condition or STOP condition, store the Response Descriptor into the Response Buffer.

Modified

Before

26.3.2.1 Operation Mode

(2) Slave Mode Operation

(b) I3C Slave Operation

4) IBI Transfer

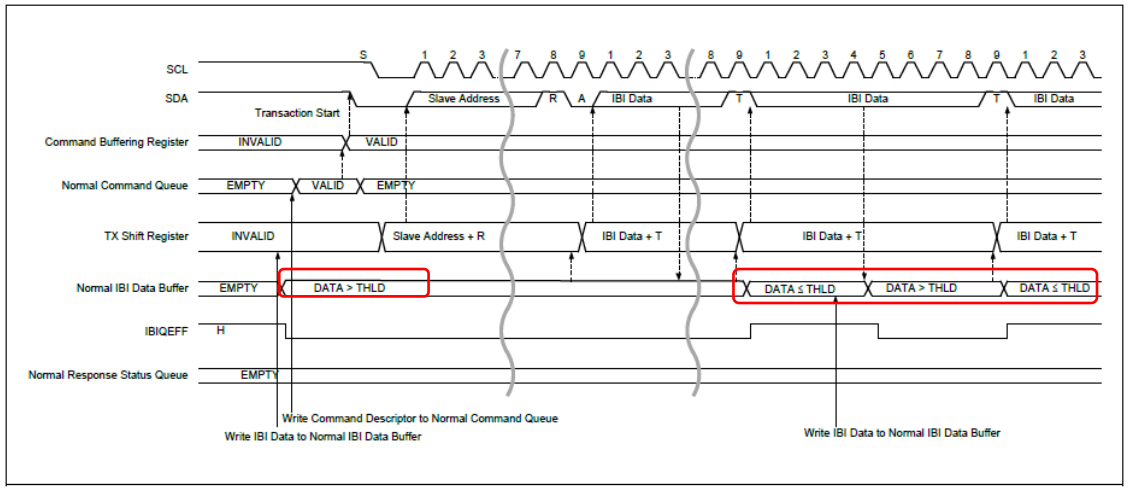


Figure 26.45 I3C Slave IBI Transfer Timing (1/2)

After

26.3.2.1 Operation Mode

(2) Slave Mode Operation

(b) I3C Slave Operation

4) IBI Transfer

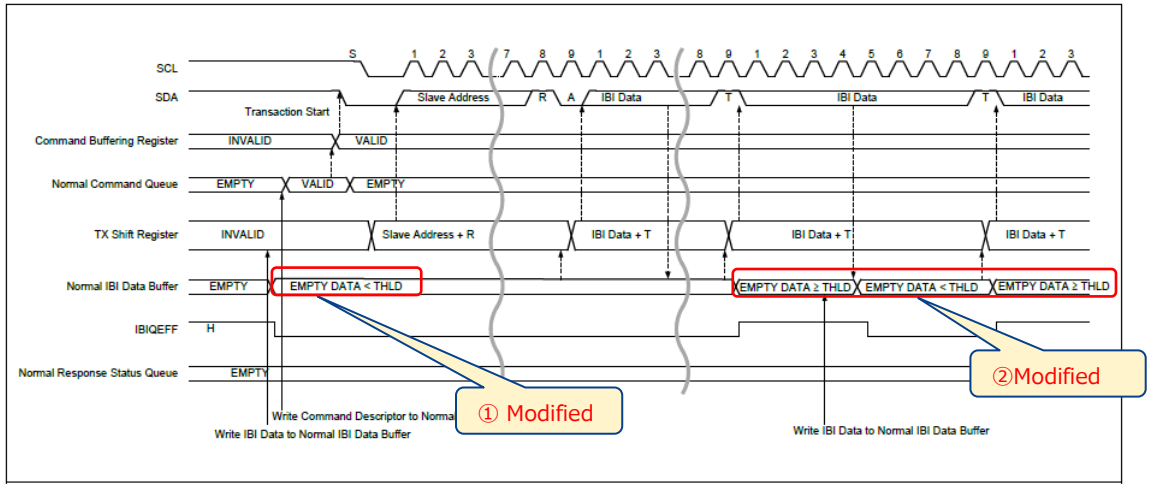


Figure 26.45 I3C Slave IBI Transfer Timing (1/2)

Before

26.3.2.1 Operation Mode

(2) Slave Mode Operation

(b) I3C Slave Operation

4) IBI Transfer

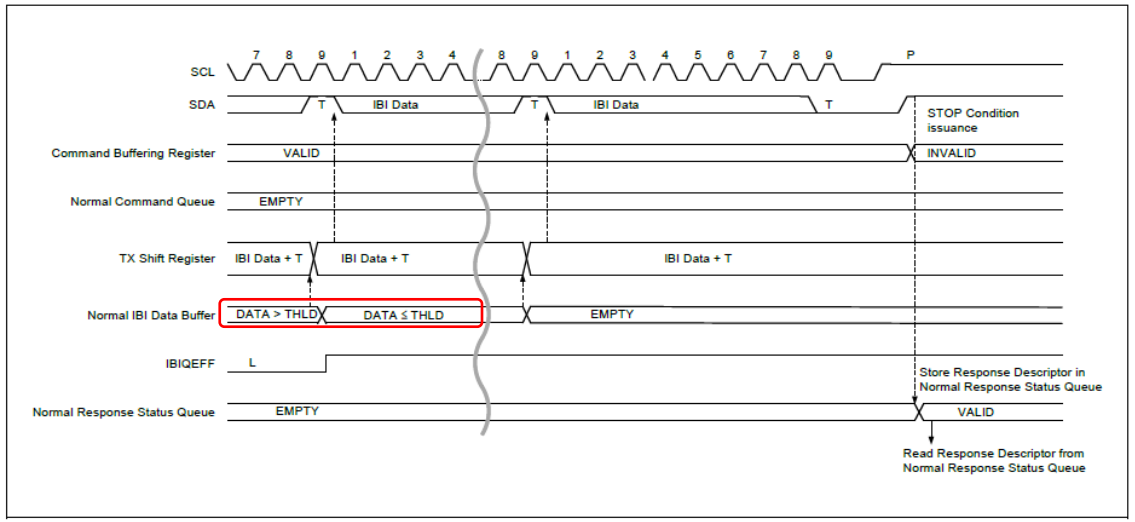


Figure 26.46 I3C Slave IBI Transfer Timing (2/2)

After

26.3.2.1 Operation Mode

(2) Slave Mode Operation

(b) I3C Slave Operation

4) IBI Transfer

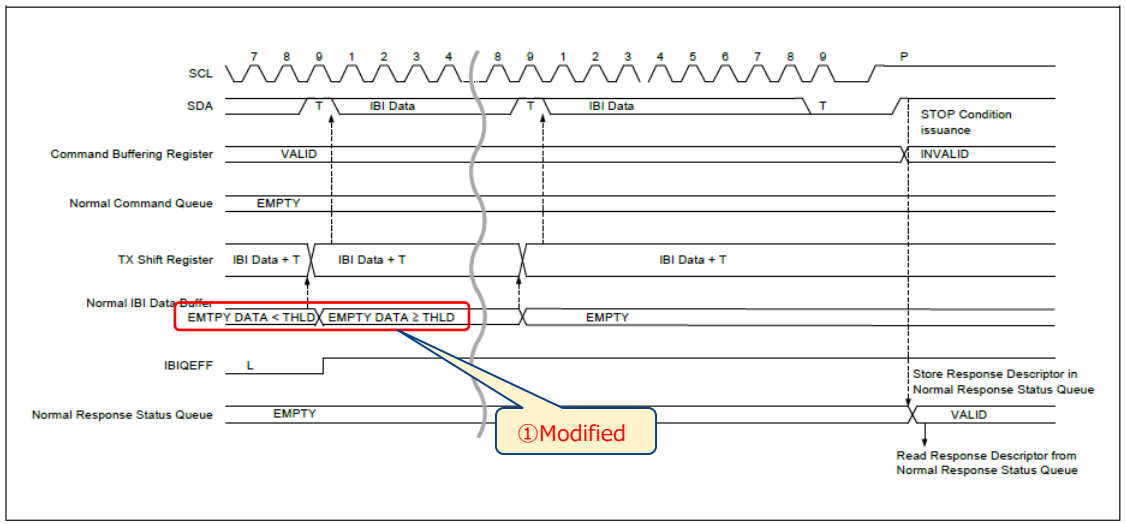


Figure 26.46 I3C Slave IBI Transfer Timing (2/2)

Before

26.3.2.3 I²C/I3C Protocol

(3) START Condition / Repeated START Condition / STOP Condition Issuing Function

(b) Issuing a Repeated START Condition

I3C issues a Repeated START condition when the CNDCTL.SRCND bit is set to 1.

When the SRCND bit is set to 1, a Repeated START condition issuance request is made and I3C issues a Repeated START condition when the BCST.BFREF flag = 0 (bus busy state) and the PRSST.CRMS bit = 1 (master mode).

A Repeated START condition is issued in the following sequence. [Repeated START condition issuance]

- Release the SDAn line.
- Ensure the low-level period of SCLn line set in STDBR.SBRLO[7:0].
- Release the SCLn line (low level to high level).
- Detect a high level of the SCLn line and ensure the time set in STDBR.SBRLO[7:0] and the Repeated START condition setup time.
- Drive the SDAn line low (high level to low level).
- Ensure the time set in STDBR.SBRHO[7:0] and the Repeated START condition hold time.
- Drive the SCLn line low (high level to low level).
- Detect a low level of the SCLn line and ensure the low-level period of SCLn line set in STDBR.SBRLO[7:0].

NOTE

When issuing Repeated START conditions request, please write the slave address to NTDTBP0 after confirming CNDCTL.SRCND = 0. Data written in the period of CNDCTL.SRCND = 1 is not forwarded because retransmission condition before the occurrence.

After

26.3.2.3 I²C/I3C Protocol

(3) START Condition / Repeated START Condition / STOP Condition Issuing Function

(b) Issuing a Repeated START Condition

I3C issues a Repeated START condition when the CNDCTL.SRCND bit is set to 1.

When the SRCND bit is set to 1, a Repeated START condition issuance request is made and I3C issues a Repeated START condition when the BCST.BFREF flag = 0 (bus busy state) and the PRSST.CRMS bit = 1 (master mode).

A Repeated START condition is issued in the following sequence. [Repeated START condition issuance]

- Release the SDAn line.
- Ensure the low-level period of SCLn line set in STDBR.SBRLO[7:0] or EXTBR.EBRLO[7:0] (Addition)
- Release the SCLn line (low level to high level).
- Detect a high level of the SCLn line and ensure the time set in STDBR.SBRLO[7:0] or EXTBR.EBRLO[7:0] and the Repeated START condition setup time. (Addition)
- Drive the SDAn line low (high level to low level).
- Ensure the time set in STDBR.SBRHO[7:0] or EXTBR.EBRHO[7:0] and the Repeated START condition hold time. (Addition)
- Drive the SCLn line low (high level to low level).
- Detect a low level of the SCLn line and ensure the low-level period of SCLn line set in STDBR.SBRLO[7:0] or EXTBR.EBRLO[7:0] (Addition) (Addition)

NOTE

When issuing Repeated START conditions request, please write the slave address to NTDTBP0 after confirming CNDCTL.SRCND = 0. Data written in the period of CNDCTL.SRCND = 1 is not forwarded because retransmission condition before the occurrence.

To issue a Repeated START condition in Hs-mode, follow the steps below. (Addition)

1. Wait until PRSTDBG.SCOLV = 0b.
2. Set EXTBR.EBRHO[7:0] to satisfy the hold time of the Repeated START condition.
3. Set the CNDCTL.SRCND bit to 1b.
4. After confirming CNDCTL.SRCND = 0b, wait until PRSTDBG.SCOLV = 0b.
5. Set EXTBR.EBRHO[7:0] according to the High period of the SCL clock in Hs-mode.
6. Write the slave address to NTDTBP0.

Before

26.3.2.3 I²C/I3C Protocol

(3) START Condition / Repeated START Condition / STOP Condition Issuing Function

(b) Issuing a Repeated START Condition

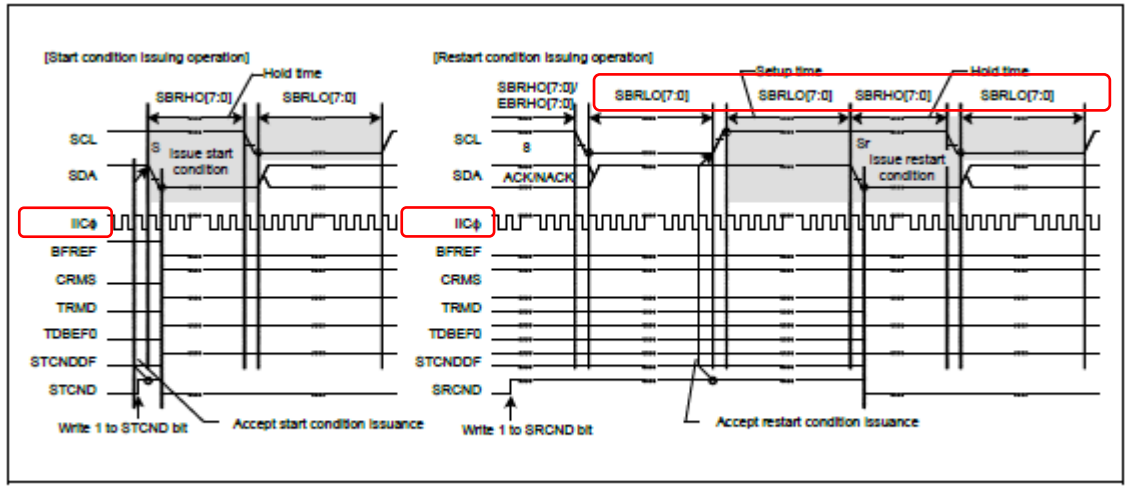


Figure 26.57 START Condition / Repeated START Condition Issue Timing (STCND and SRCND bits)

Figure 26.58 shows the operation to issue a Repeated START condition after the master transmission. [Repeated START condition issuance after the master transmission]

- Initial setting. For details, refer to **Section 26.3.3.1, Initial Setting Flow**.

After

26.3.2.3 I²C/I3C Protocol

(3) START Condition / Repeated START Condition / STOP Condition Issuing Function

(b) Issuing a Repeated START Condition

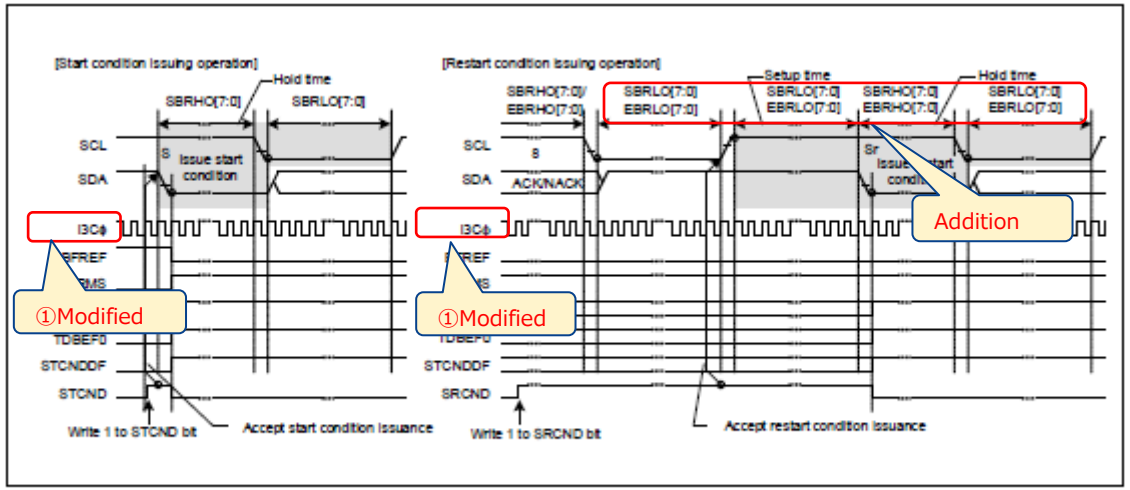


Figure 26.57 START Condition / Repeated START Condition Issue Timing (STCND and SRCND bits)

Figure 26.58 shows the operation to issue a Repeated START condition after the master transmission.
[Repeated START condition issuance after the master transmission]

- Initial setting. For details, refer to **Section 26.3.3.1, Initial Setting Flow**.

Modified

Before

26.3.2.3 I²C/I3C Protocol

(3) START Condition / Repeated START Condition / STOP Condition Issuing Function

(c) Issuing a STOP Condition

I3C issues a STOP condition when the SPCND bit in CNDCTL is set to 1.

When the SPCND bit is set to 1, a STOP condition issuance request is made and I3C issues a STOP condition when the BCST.BFREF flag = 0 (bus busy state) and the PRSST.MST bit = 1 (master mode).

A STOP condition is issued in the following sequence.

[STOP condition issuance]

- Drive the SDAn line low (high level to low level).
- Ensure the low-level period of SCLn line set in STDBR.SBRLO[7:0].
- Release the SCLn line (low level to high level).
- Detect a high level of the SCLn line and ensure the time set in STDBR.SBRHO[7:0] and the STOP condition setup time.
- Release the SDAn line (low level to high level).
- Ensure the time set in STDBR.SBRLO[7:0] and the bus free time.
- Set the BFREF flag to 1 (to release the bus mastership).

After

26.3.2.3 I²C/I3C Protocol

(3) START Condition / Repeated START Condition / STOP Condition Issuing Function

(c) Issuing a STOP Condition

I3C issues a STOP condition when the SPCND bit in CNDCTL is set to 1.

When the SPCND bit is set to 1, a STOP condition issuance request is made and I3C issues a STOP condition when the BCST.BFREF flag = 0 (bus busy state) and the PRSST.MST bit = 1 (master mode).

A STOP condition is issued in the following sequence.

[STOP condition issuance]

- Drive the SDAn line low (high level to low level).
- Ensure the low-level period of SCLn line set in STDBR.SBRLO[7:0] or EXTBR.EBRLO[7:0]. (Addition)
- Release the SCLn line (low level to high level).
- Detect a high level of the SCLn line and ensure the time set in STDBR.SBRHO[7:0] or EXTBR.EBRHO[7:0] and the STOP condition setup time. (Addition)
- Release the SDAn line (low level to high level).
- Ensure the time set in BFRECDT.FRECYC[8:0] and the bus free time. (Modified)
- Set the BFREF flag to 1 (to release the bus mastership).

NOTE

To issue a STOP condition in Hs-mode, follow the steps below

1. Wait until PRSTDBG.SCOLV = 0b.
2. Set EXTBR.EBRHO[7:0] to satisfy the setup time for the STOP condition.
3. Set the CNDCTL.SPCND bit to 1b.
4. Wait until CNDCTL.SPCND = 0b.
5. Set EXTBR.EBRHO [7:0] according to the High period of the SCL clock in Hs-mode.

(Addition)

Before

26.3 Operation

26.3.2 Details of Function

26.3.2.3 I²C/I3C Protocol

(3) START Condition / Repeated START Condition / STOP Condition Issuing Function

(c) Issuing a STOP Condition

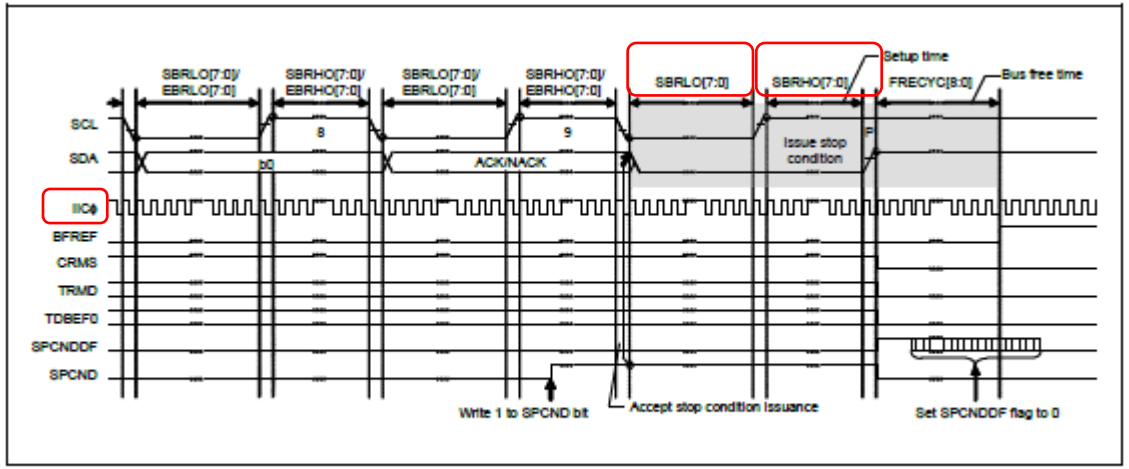


Figure 26.59 STOP Condition Issue Timing (SPCND bit)

After

26.3 Operation

26.3.2 Details of Function

26.3.2.3 I²C/I3C Protocol

(3) START Condition / Repeated START Condition / STOP Condition Issuing Function

(c) Issuing a STOP Condition

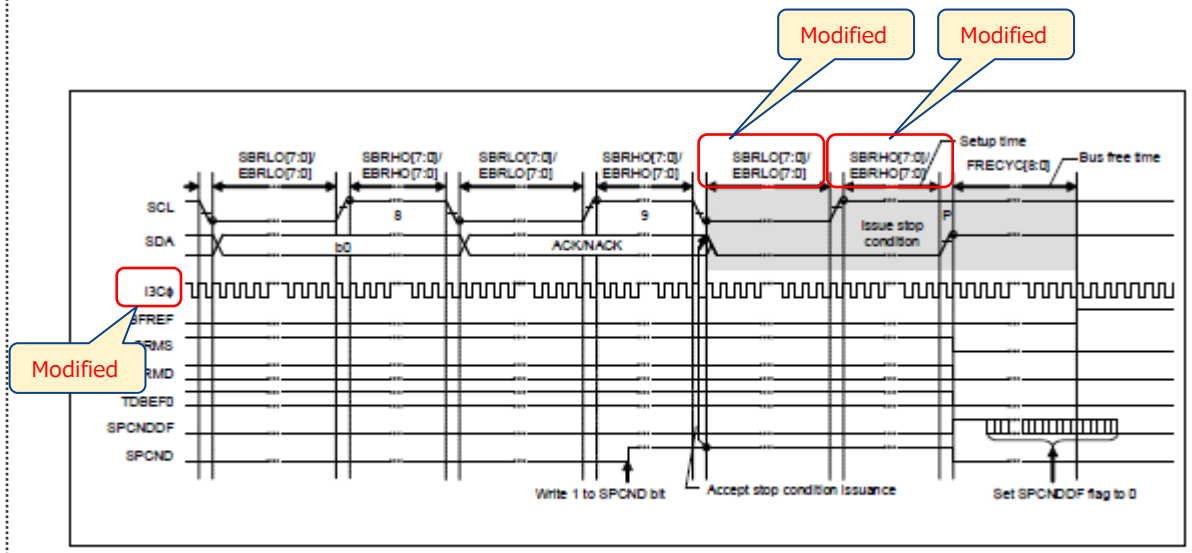


Figure 26.59 STOP Condition Issue Timing (SPCND bit)

Before

(10) Async Mode 1 (Asynchronous Advanced Mode)

For timing control in Async Mode 1, set the ATCTL register if necessary.

(a) I3C Master

This IP has counters of MREF (32 bits), MSyncCNT (32 bits) and MC2 (16 bits) for Async Mode 1.

- MREF Counter

  When ATCCNTE.ATCE is enabled, it starts counting.
  It captures as MREF at the SCL rise edge next to ACK for the IBI transmitted from the I3C Slave.
  The MREF extension method described in "1) I3C Master" of **Section 26.3.2.3(9)(b), Async Mode 0 (Asynchronous Basic Mode)** is also possible in Async Mode 1.

- MSyncCNT Counter

  When ATCCNTE.ATCE is enabled, it starts counting.
  It captures as MSyncCNT for each aME (SDA falling edge of START condition) and store it in the capture register.

- MC2 Counter

  After enabling ATCCNTE.ATCE, it counts up from the SCL rise edge next to ACK for the IBI transmitted from the I3C Slave to the SCL rise edge next to the Tbit after Mandatory Byte and capture it as MC2.

The MREF and MC2 capture values are stored next to the IBI Status Descriptor when the IBI is received from the I3C Slave with the DATBASm.DVIBITS bit set to 1. (Same as Async Mode 0)

(b) I3C Slave

This IP has counters of SC1 (16 bits), SC2 (8 bits) and aME_TICK (8 bits) for Async Mode 1.

- SC1 Counter

  After enabling ATCCNTE.ATCE, it counts up from SC1 count trigger*1 to the first aME and capture it as SC1.

Note 1. SW or external trigger can be selected by selection bits.
The SC1 count trigger select method described in "2) I3C Slave" of **Section 26.3.2.3(9)(b), Async Mode 0 (Asynchronous Basic Mode)** is also possible in Async Mode 1.

- SC2 Counter

  After enabling ATCCNTE.ATCE, it counts up from SCL rise edge next to ACK for the IBI transmitted from I3C Slave to SCL rise edge next to Tbit after Mandatory Byte and capture it as SC2.

After

Modified

(c) Async Mode 1 (Asynchronous Advanced Mode)

Modified

For timing control in Async Mode 1, set the ATCTL register if necessary.

1) I3C Master

This IP has counters of MREF (32 bits), MSyncCNT (32 bits) and MC2 (16 bits) for Async Mode 1.

- MREF Counter

  When ATCCNTE.ATCE is enabled, it starts counting.
  It captures as MREF at the SCL rise edge next to ACK for the IBI transmitted from the I3C Slave.
  The MREF extension method described in "1) I3C Master" of **Section 26.3.2.3(9)(b), Async Mode 0 (Asynchronous Basic Mode)** is also possible in Async Mode 1.

- MSyncCNT Counter

  When ATCCNTE.ATCE is enabled, it starts counting.
  It captures as MSyncCNT for each aME (SDA falling edge of START condition) and store it in the capture register.

- MC2 Counter

  After enabling ATCCNTE.ATCE, it counts up from the SCL rise edge next to ACK for the IBI transmitted from the I3C Slave to the SCL rise edge next to the Tbit after Mandatory Byte and capture it as MC2.

The MREF and MC2 capture values are stored next to the IBI Status Descriptor when the IBI is received from the I3C Slave with the DATBASm.DVIBITS bit set to 1. (Same as Async Mode 0)

Modified

2) I3C Slave

This IP has counters of SC1 (16 bits), SC2 (8 bits) and aME_TICK (8 bits) for Async Mode 1.

- SC1 Counter

  After enabling ATCCNTE.ATCE, it counts up from SC1 count trigger to the first aME and capture it as SC1.

Deleted

- SC2 Counter

  After enabling ATCCNTE.ATCE, it counts up from SCL rise edge next to ACK for the IBI transmitted from I3C Slave to SCL rise edge next to Tbit after Mandatory Byte and capture it as SC2.

Before

26.3.2.4 Error Detection

Deleted

(1) SDR Error Detection and Recovery Methods for I3C Slave Devices [I3C mode]

The seven error types summarized in **Table 26.14** are supported for all I3C slave devices. Each error type is further explained below the table.

Table 26.14 SDR Slave Error Types

Error Type	Description	Error Detection Method	Error Recovery Method
S0	Broadcast address/W (= H'7E/W) or Dynamic address/RW	Detect any of the following: H'3E/W H'5E/W H'6E/W H'76/W H'7A/W H'7C/W H'7F/W H'7E/R	Enable HDR EXIT Detector and ignore all other patterns
S1	CCC code	Parity check, using T-Bit	Enable HDR EXIT detector and neglect other patterns
S2	Write data	Parity check, using T-Bit	Enable STOP detector and neglect other patterns
S3	Assigned address during Dynamic address arbitration	Parity check, using PAR Bit	Generate NACK (after PAR), then wait for another Repeated START and 7E/R to re-transmit the Provisional ID
S4	H'7E/R after Sr during Dynamic address arbitration	Detect any value other than H'7E/R after Sr during Dynamic Address Arbitration	Generate NACK (after H'7E/R), then enable STOP Detector and ignore all other patterns
S5	Transaction after detecting CCC	Detect illegally formatted CCC	Generate NACK (after Slave Address), then enable STOP Detector and ignore all other patterns
S6 (optional)	Monitoring error	Slave detects (through monitoring) that transmitted Data differs from what it intended to transmit (Does not apply during Dynamic address arbitration)	Stop the transmission, then enable STOP Detector and ignore all other patterns

Deleted

After

26.3.2.4 Error Detection

(1) SDR Error Detection for I3C Slave Devices [I3C mode]

The seven error types summarized in **Table 26.14** are supported for all I3C slave devices. Each error type is further explained below the table.

Table 26.14 SDR Slave Error Types

Error Type	Description	Error Detection Method
S0	Broadcast address/W (= H'7E/W) or Dynamic address/RW	Detect any of the following: H'3E/W H'5E/W H'6E/W H'76/W H'7A/W H'7C/W H'7F/W H'7E/R
S1	CCC code	Parity check, using T-Bit
S2	Write data	Parity check, using T-Bit
S3	Assigned address during Dynamic address arbitration	Parity check, using PAR Bit
S4	H'7E/R after Sr during Dynamic address arbitration	Detect any value other than H'7E/R after Sr during Dynamic Address Arbitration
S5	Transaction after detecting CCC	Detect illegally formatted CCC
S6 (optional)	Monitoring error	Slave detects (through monitoring) that transmitted Data differs from what it intended to transmit (Does not apply during Dynamic address arbitration)

Before

26.3.2.4 Error Detection

Deleted

(2) SDR Error Detection and Recovery Methods for I3C Master Devices [I3C mode]

The two error types summarized in **Table 26.15** are supported for all I3C master devices. Each error type is further explained below the table.

Table 26.15 SDR Master Error Types

Error Type	Description	Error Detection Method	Error Recovery Method
M0	Transaction after sending CCC	Detect illegally formatted CCC	Stop the transmission, then send STOP and retry the transmission.
M1 (optional)	Monitoring error	Master detects (through monitoring) transmitted data different from what it intended to transmit (Does not apply during Dynamic address arbitration)	Stop the transmission, then send STOP and retry the transmission.
M2	No response to Broadcast address (H'7E)	Master detects NACK after Broadcast address (H'7E) transmission	Upon detection of NACK, master transmits HDR exit pattern followed by STOP

Deleted

After

26.3.2.4 Error Detection

(2) SDR Error Detection for I3C Master Devices [I3C mode]

The two error types summarized in **Table 26.15** are supported for all I3C master devices. Each error type is further explained below the table.

Table 26.15 SDR Master Error Types

Error Type	Description	Error Detection Method
M0	Transaction after sending CCC	Detect illegally formatted CCC
M1 (optional)	Monitoring error	Master detects (through monitoring) transmitted data different from what it intended to transmit (Does not apply during Dynamic address arbitration)
M2	No response to Broadcast address (H'7E)	Master detects NACK after Broadcast address (H'7E) transmission

Before

26.3.2.4 Error Detection

(6) Error Recovery Operation [I3C mode]

When an error occurs, the INST.INEF, NTST.TEF and NTST.TABTF flags are set to 1 according to the cause of the error, or the interrupts associated with each flag are asserted (when detection and interrupts are enabled.)

There is a possibility of communication error or internal module error.

The I3C master must perform an error recovery flow according to the following case:

- When TEF is detected.

After

26.3.2.4 Error Detection

(6) Error Recovery Operation [I3C mode]

Addition

(a) Error Recovery Operation

When an error occurs, the flags of INST.INEF, NTST.TEF, HSTS.TEF and NTST.TABTF are set to 1b according to the cause of the error.

Or the interrupts INT_n3c_ierr_n, INT_n3c_terr_n and INT_ri3c_abort_n associated with each flag are asserted. (When detection and interrupts are enabled.)

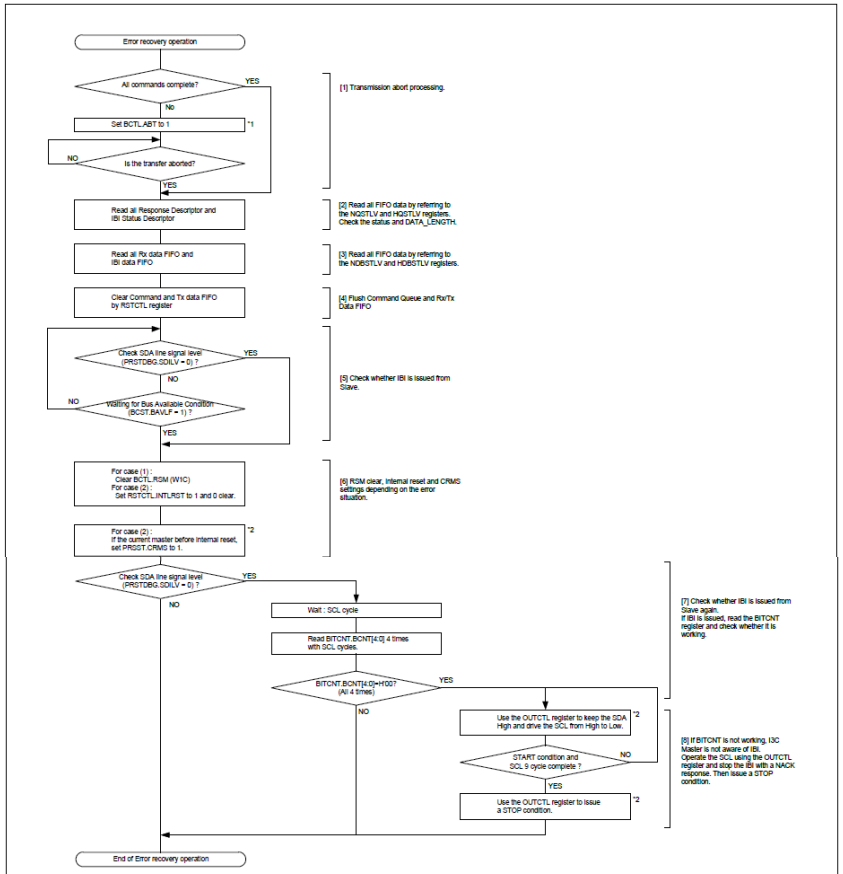
There is a possibility of communication error or I3C internal error.

If an error occurs, I3C will be suspended. (BCTL.RSM becomes 1b.) After I3C is suspended, the application must write the value 1b to the BCTL.RSM bit to resume I3C operation and recover from the suspended state.

Modified

Before

Figure 26.99 and Figure 26.100 show the error recovery flow.



Note 1. If the transfer is not aborted due to an error, set the BCTL.ABT bit to 1 and then abort the transfer.

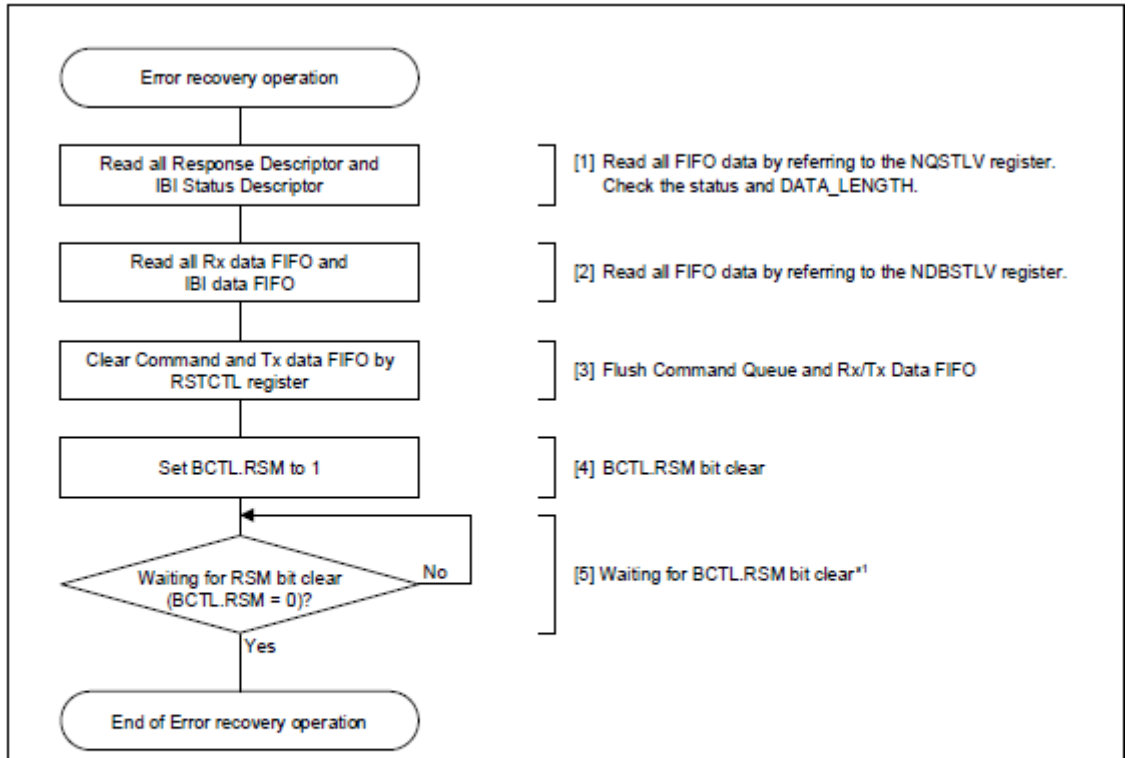
Note 2. When writing to the CRMS bit, set PRSST.PRSSTWP bit to 1 at the same time.

Note 3. When writing to the SDOC and SCOC bit, set OUTCTL.SOCWP bit to 1 at the same time.

Figure 26.99 Example of Error Recovery Operation Flowchart for I3C Master

After

Figure 26.99 and Figure 26.100 show the error recovery flow.



Note 1. The Command Descriptor can be written to the Command Queue via writing to the Command Queue Port (NCMDQP) before the RSM bit is cleared.

Figure 26.99 Example of Error Recovery Operation Flowchart for I3C Master

Modified

Before

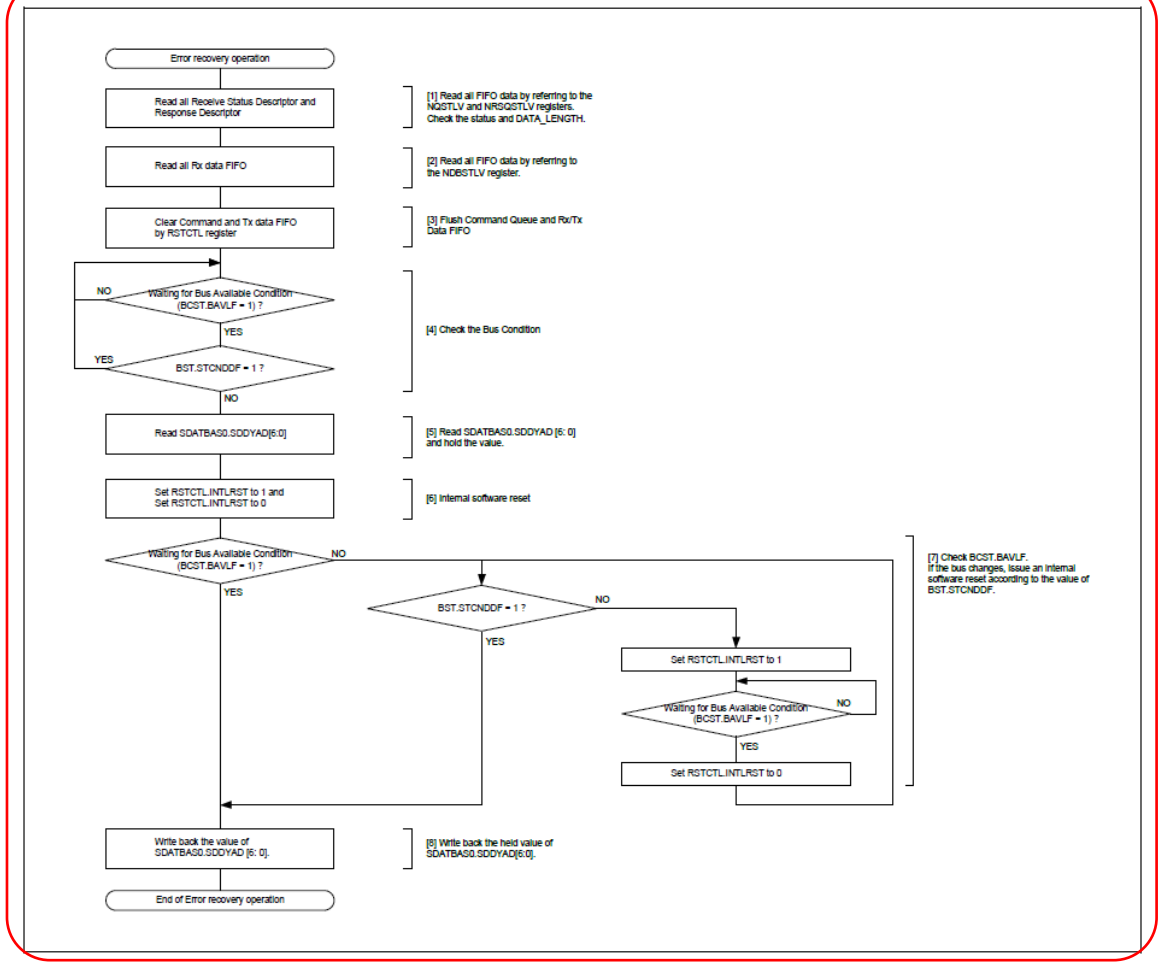


Figure 26.100 Example of Error Recovery Operation Flowchart for I3C Slave

After

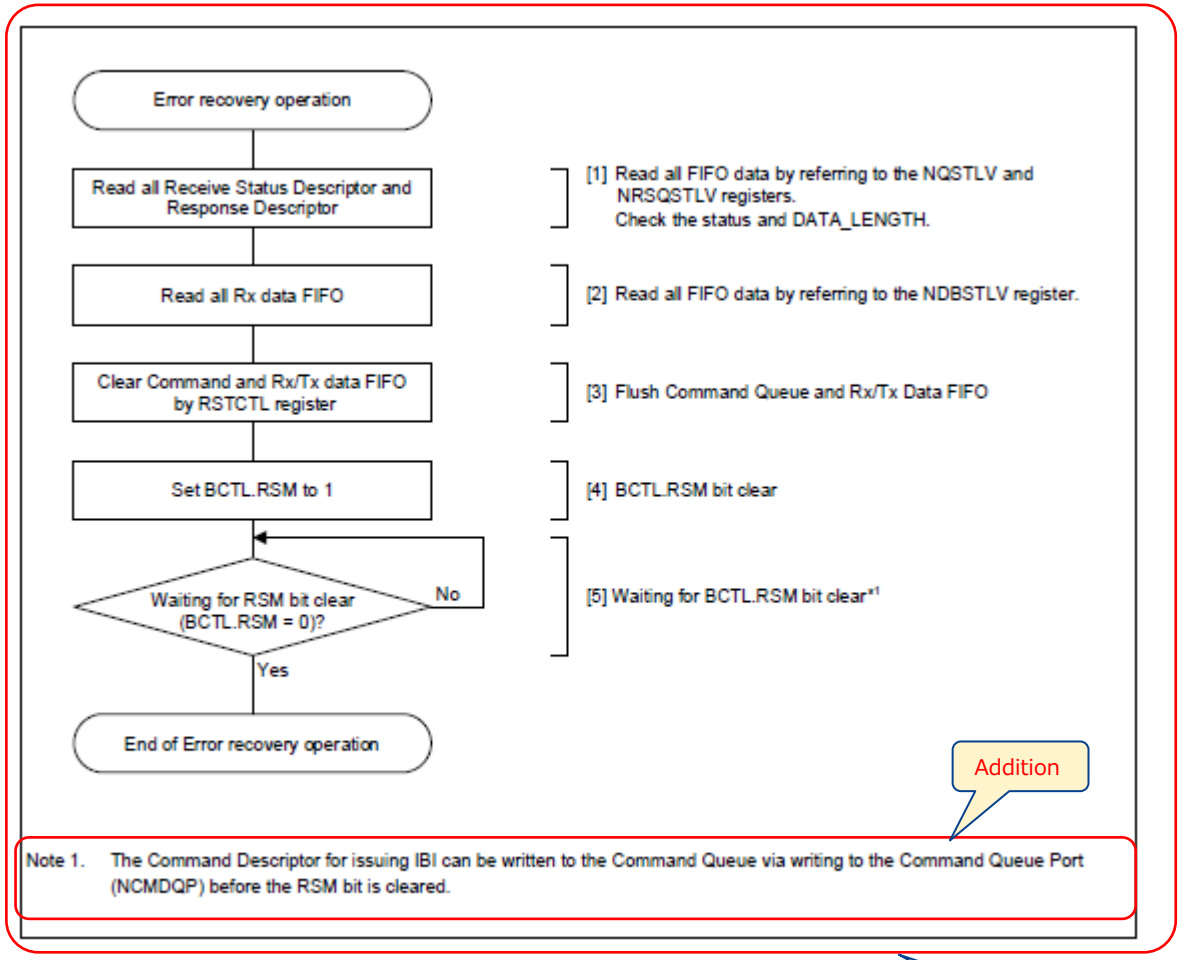


Figure 26.100 Example of Error Recovery Operation Flowchart for I3C Slave

Before

– (none)

After

When I3C Slave recovers from an error according to the error recovery flow, after setting BCTL.RSM to 1b, BCTL.RSM becomes 0b after detecting a state in which Bus Available period communication is not performed on I3C Bus.

If communication occurs on the I3C bus within the Bus Available period, BCTL.RSM will not be set to 0b and error recovery will not be completed, and a NACK response will be transmitted.

(b) Master Error Detection and Escalation Handling

If the Master does not receive an ACK of a transmitted private Message to a Slave and Steps 1 and 2 described in *Chapter 5.1.10.2.4 of MIPI I3C Spec v1.0* fail, the processing flow of Step 3 shown in **Figure 26.101** and **Figure 26.102** is followed.

Addition

Before

– (none)

After

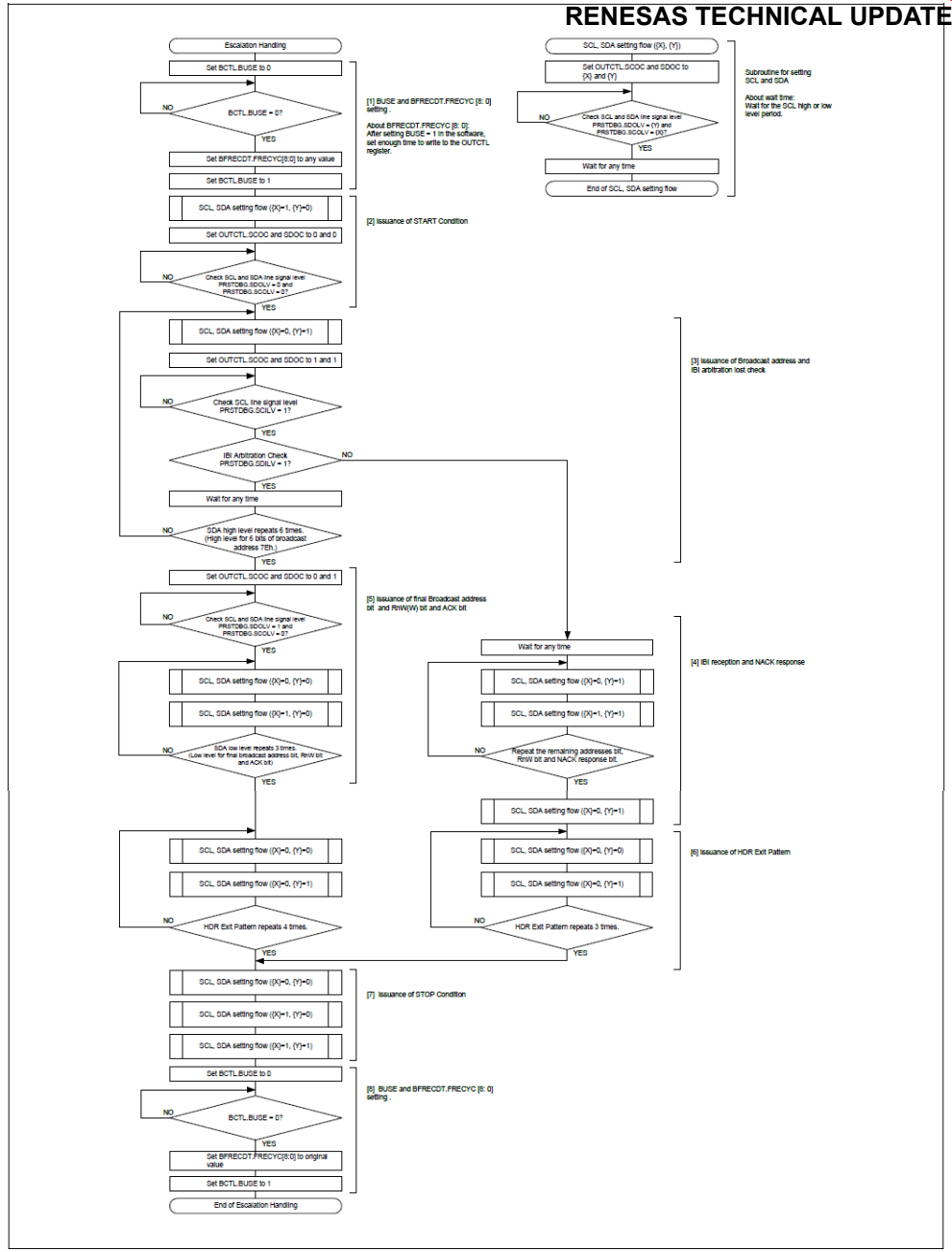


Figure 26.101 Escalation Handling Flowchart for I3C Master

Addition

Before

– (none)

After

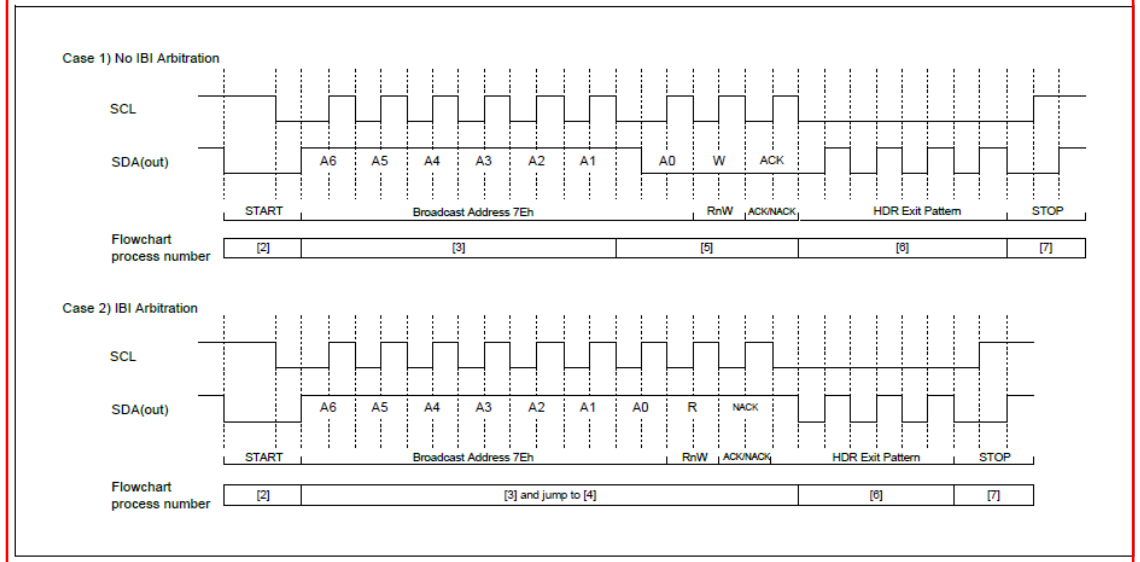


Figure 26.102 Escalation Handling timing chart for I3C Master

Addition

Before

26.3.3 Operation

26.3.3.1 Initial Setting Flow

(2) I3C Initial Setting Flow

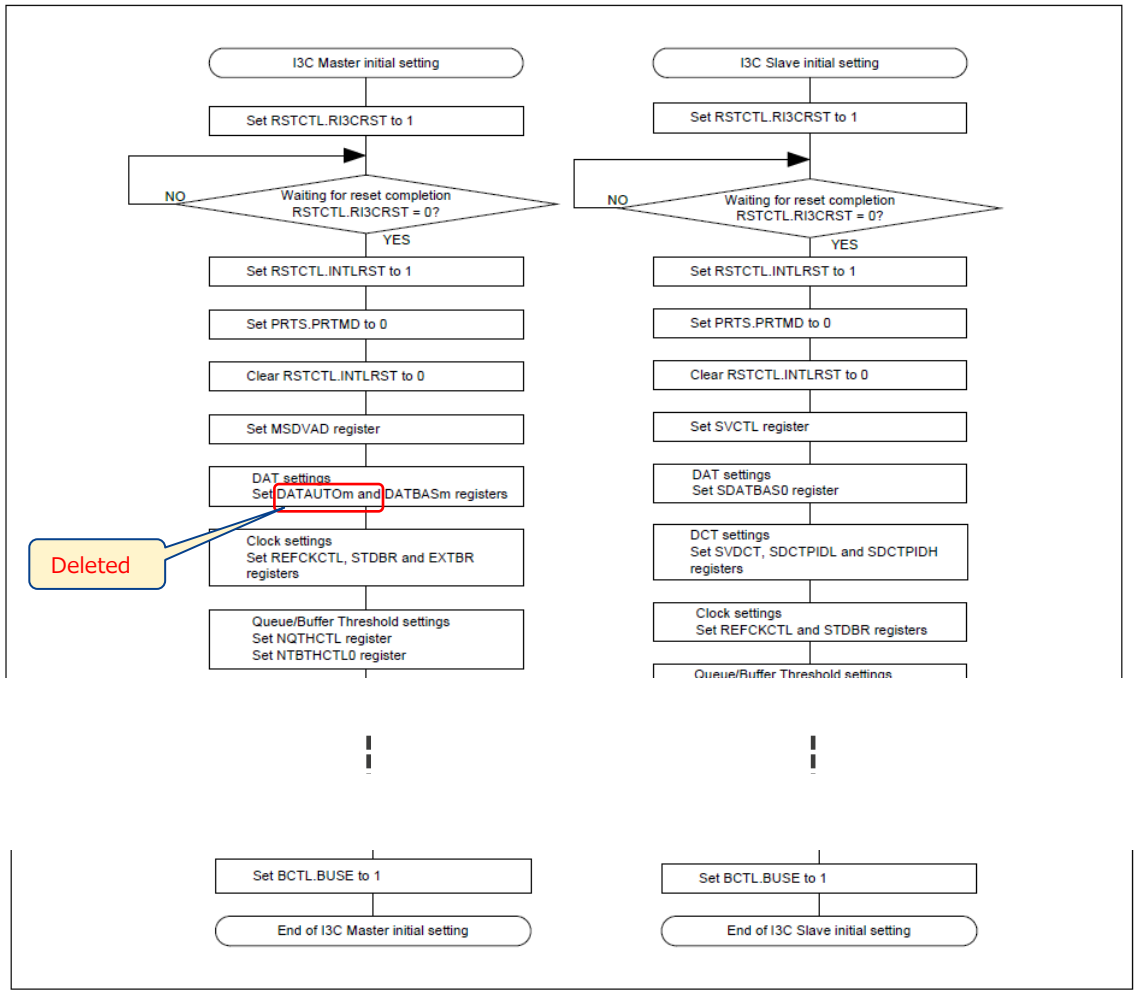


Figure 26.116 Example of I3C Initialization Flowchart

After

26.3.3 Operation

26.3.3.1 Initial Setting Flow

(2) I3C Initial Setting Flow

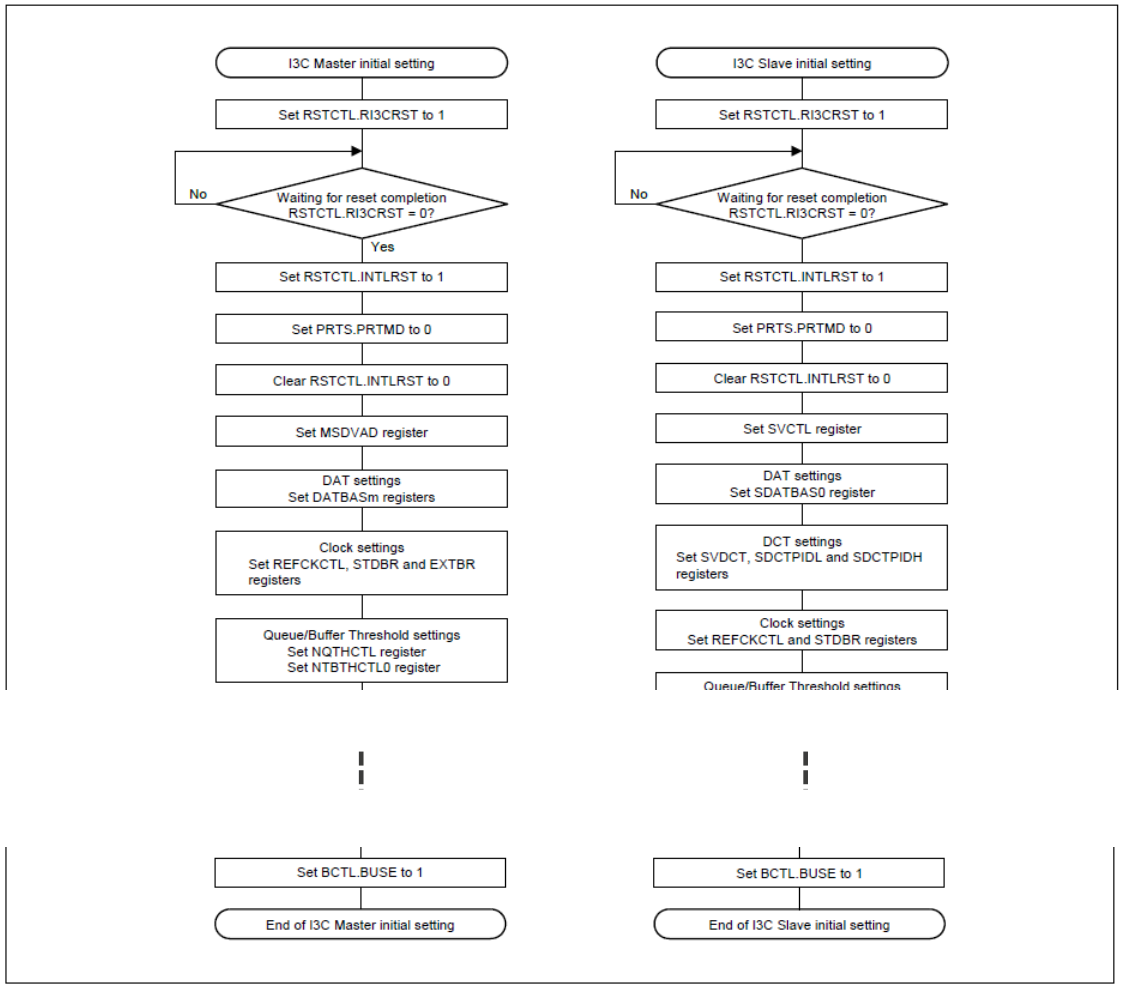


Figure 26.118 Example of I3C Initialization Flowchart

Before

26.3.3 Operation

26.3.3.3 Master Mode Communication Flow

(2) I²C Master Reception Flow (Single Buffer Transfer)

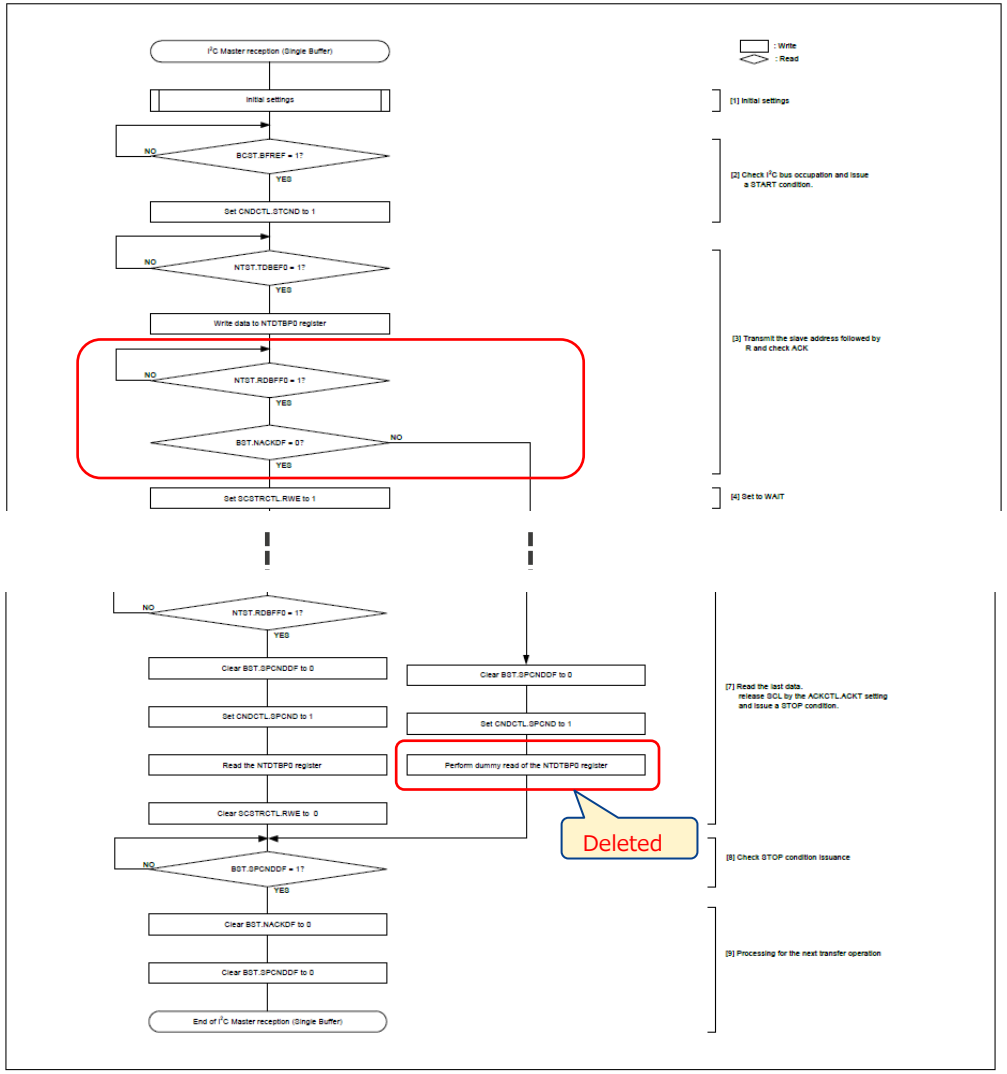


Figure 26.119 Example of I²C Master Reception Flowchart (7-bit Address Format, 1 or 2 bytes)

After

26.3.3 Operation

26.3.3.3 Master Mode Communication Flow

(2) I²C Master Reception Flow (Single Buffer Transfer)

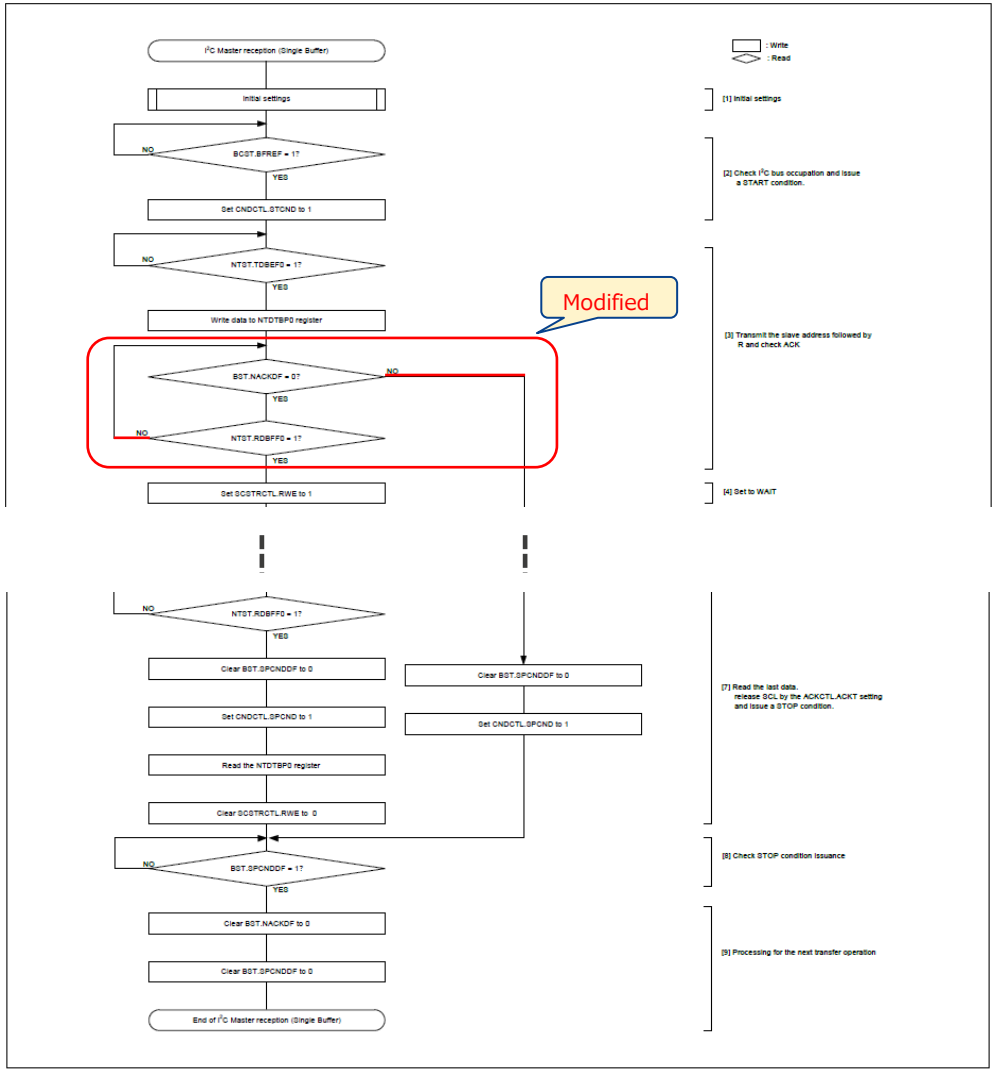


Figure 26.121 Example of I²C Master Reception Flowchart (7-bit Address Format, 1 or 2 bytes)

Before

26.3.3 Operation

26.3.3.3 Master Mode Communication Flow

(2) I²C Master Reception Flow (Single Buffer Transfer)

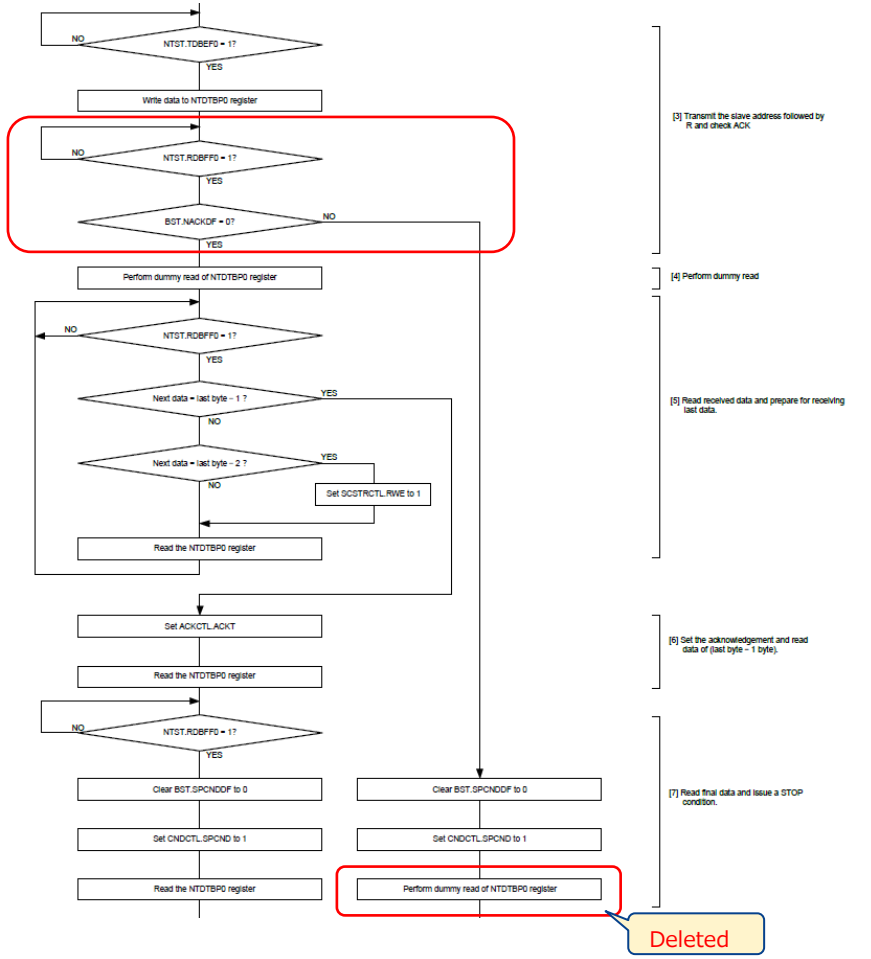


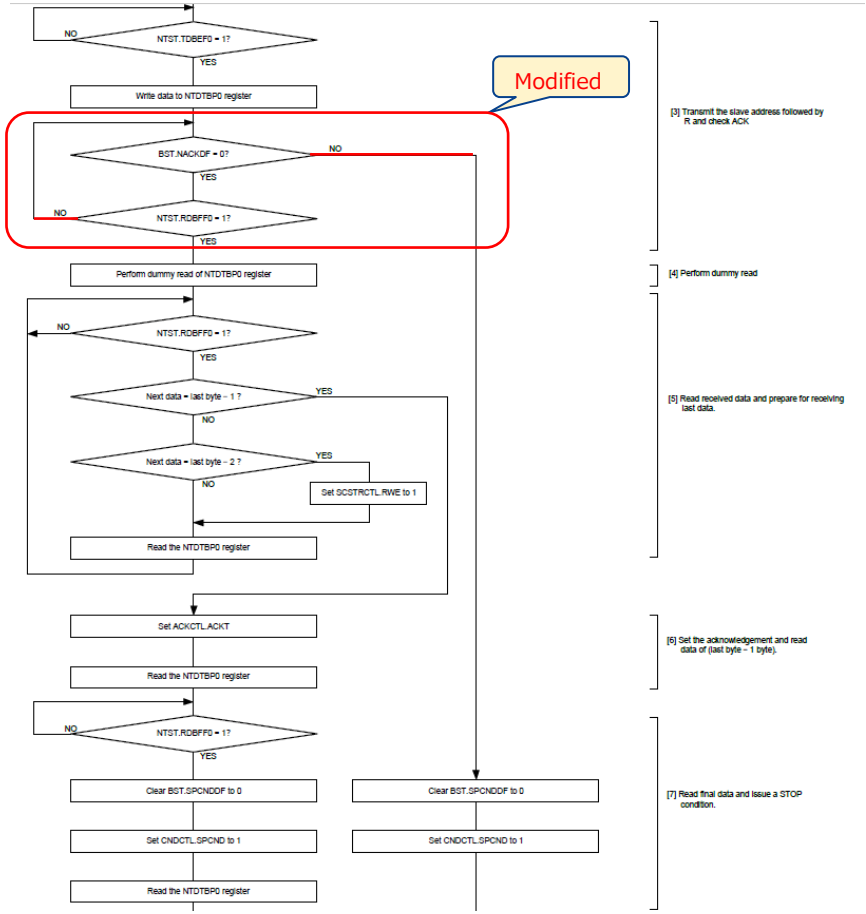
Figure 26.120 Example of I2C Master Reception Flowchart (7-bit Address Format, 3 bytes or more)

After

26.3.3 Operation

26.3.3.3 Master Mode Communication Flow

(2) I²C Master Reception Flow (Single Buffer Transfer)



Before

26.3.3 Operation

26.3.3.3 Master Mode Communication Flow

(6) I3C Master Wake-Up Flow

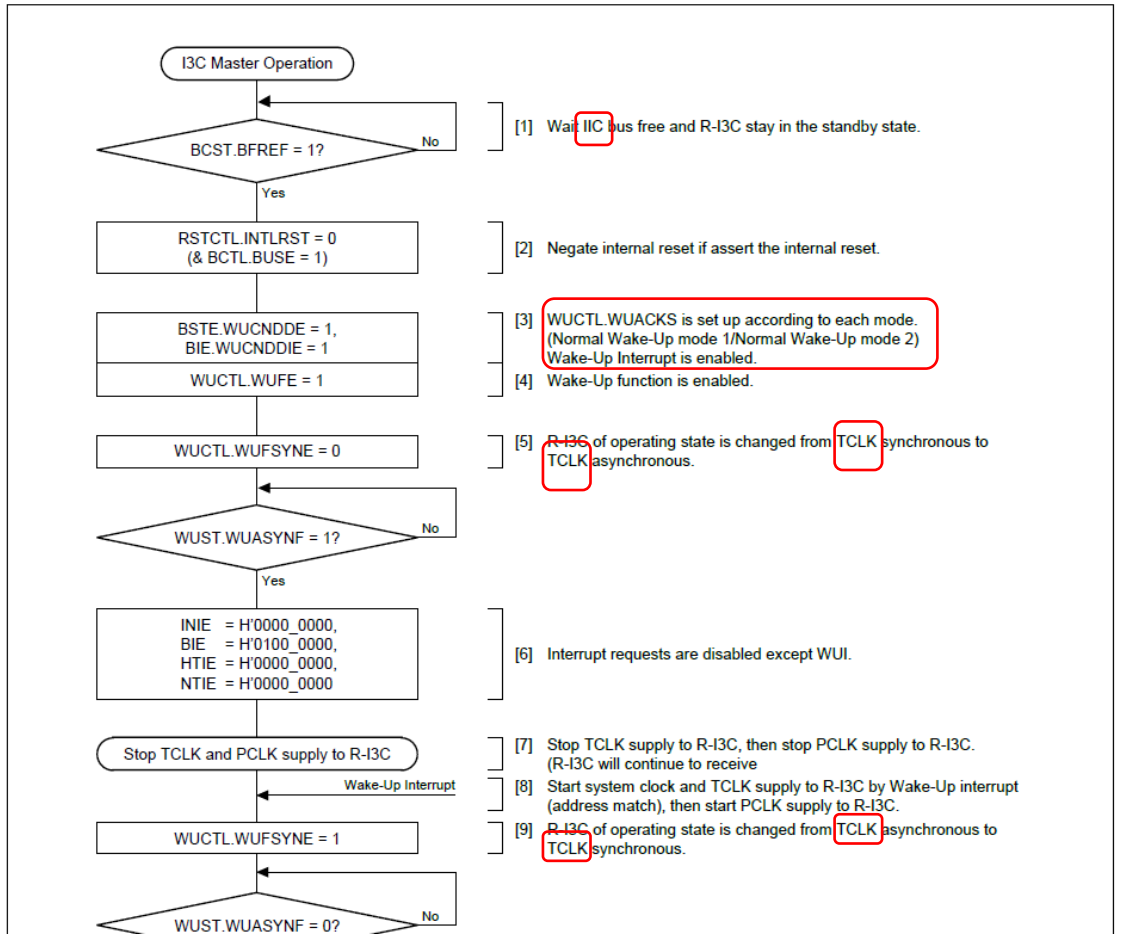


Figure 26.124 Use Case of I3C Master Wake-Up
(Wake-Up Recovery by a Wake-Up Interrupt Triggered by the Match of the Slave Address)

After

26.3.3 Operation

26.3.3.3 Master Mode Communication Flow

(6) I3C Master Wake-Up Flow

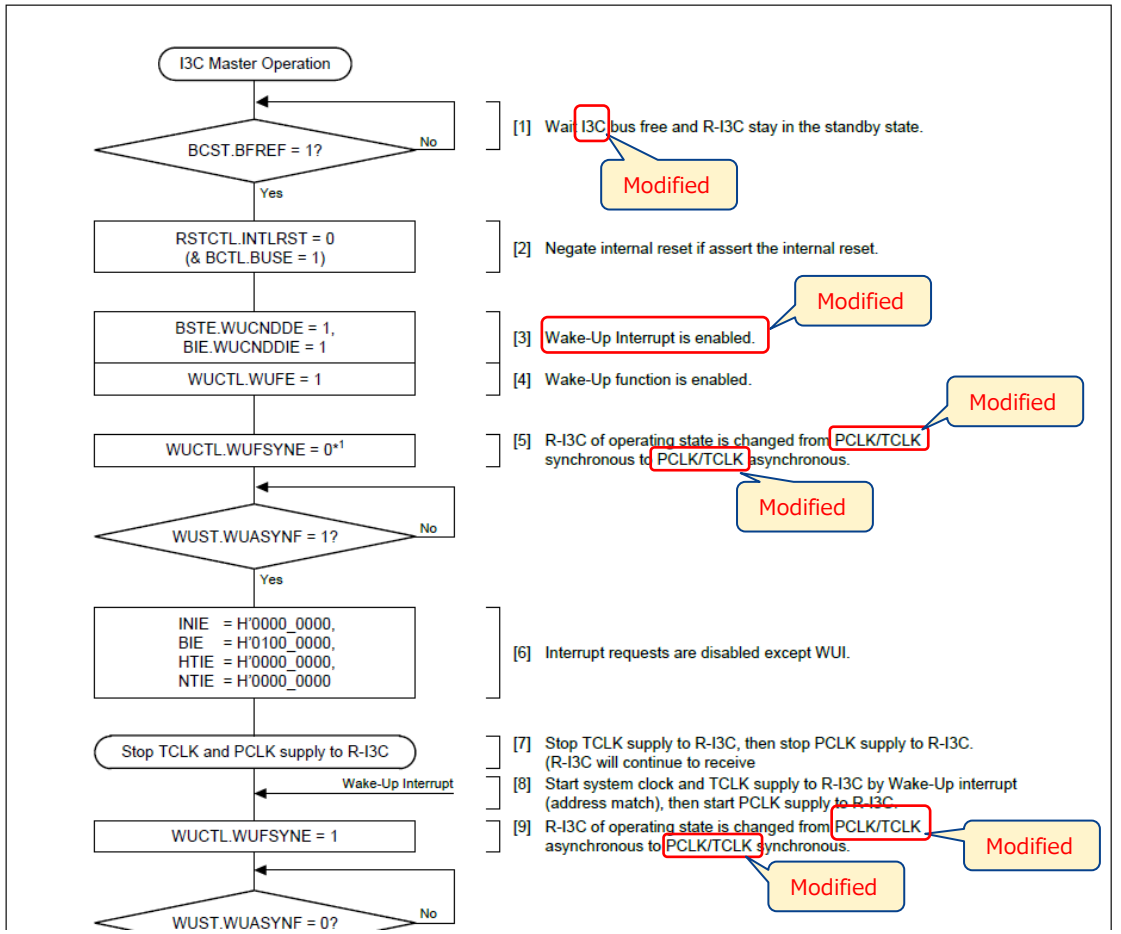


Figure 26.126 Use Case of I3C Master Wake-Up
(Wake-Up Recovery by a Wake-Up Interrupt Triggered by the Match of the Slave Address)

Before

26.3.3 Operation

26.3.3.4 Slave Mode Communication Flow

(1) I²C Slave Transmission Flow (Single Buffer Transfer)

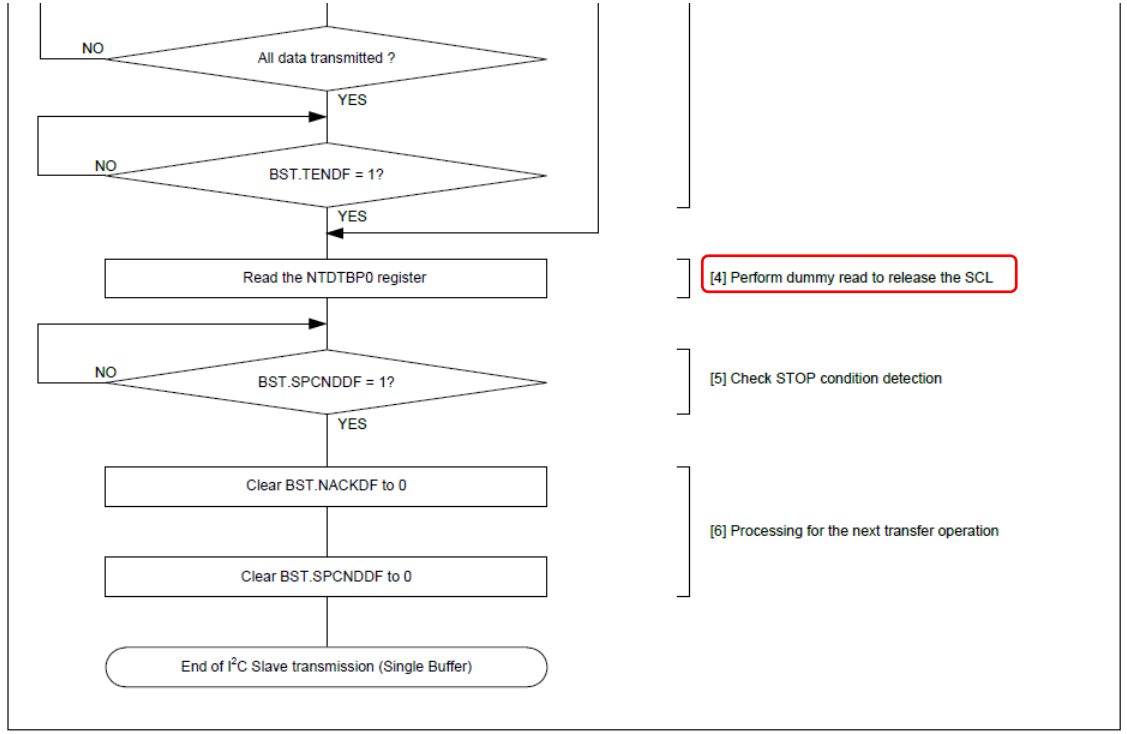


Figure 26.125 Example of I²C Slave Transmission Flowchart (Single Buffer Transfer)

After

26.3.3 Operation

26.3.3.4 Slave Mode Communication Flow

(1) I²C Slave Transmission Flow (Single Buffer Transfer)

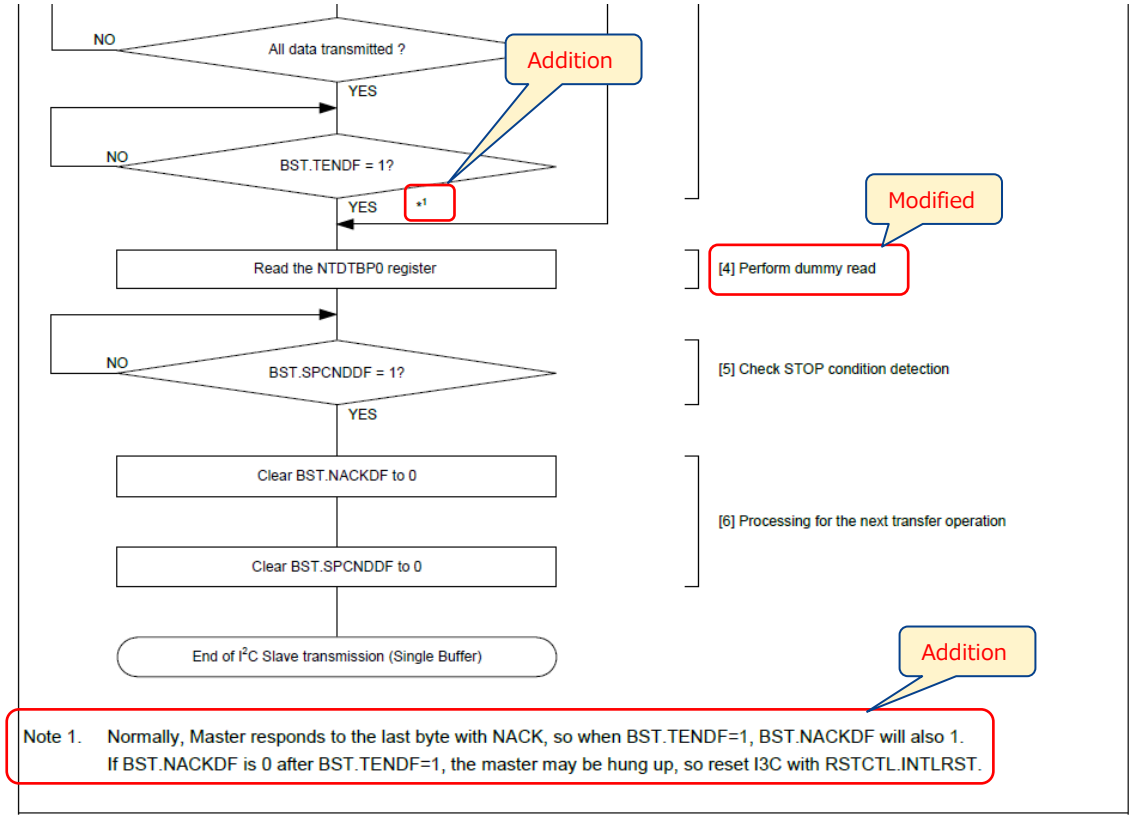


Figure 26.127 Example of I²C Slave Transmission Flowchart (Single Buffer Transfer)

Before

26.3.3 Operation

26.3.3.4 Slave Mode Communication Flow

(6) I3C Slave Wake-Up Flow

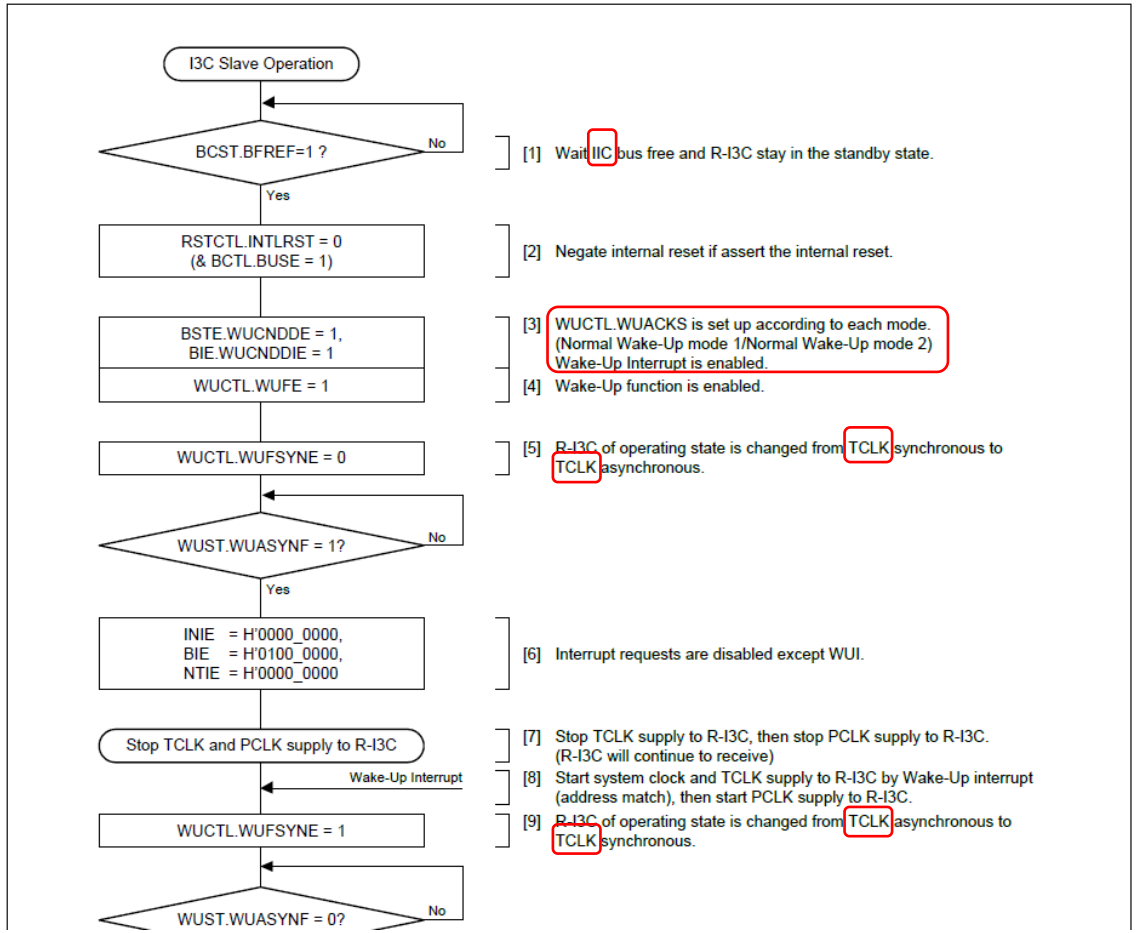


Figure 26.132 Use Case of I3C Slave Wake-Up
(Wake-Up Recovery by a Wake-Up Interrupt Triggered by the Match of the Slave Address)

After

26.3.3 Operation

26.3.3.4 Slave Mode Communication Flow

(6) I3C Slave Wake-Up Flow

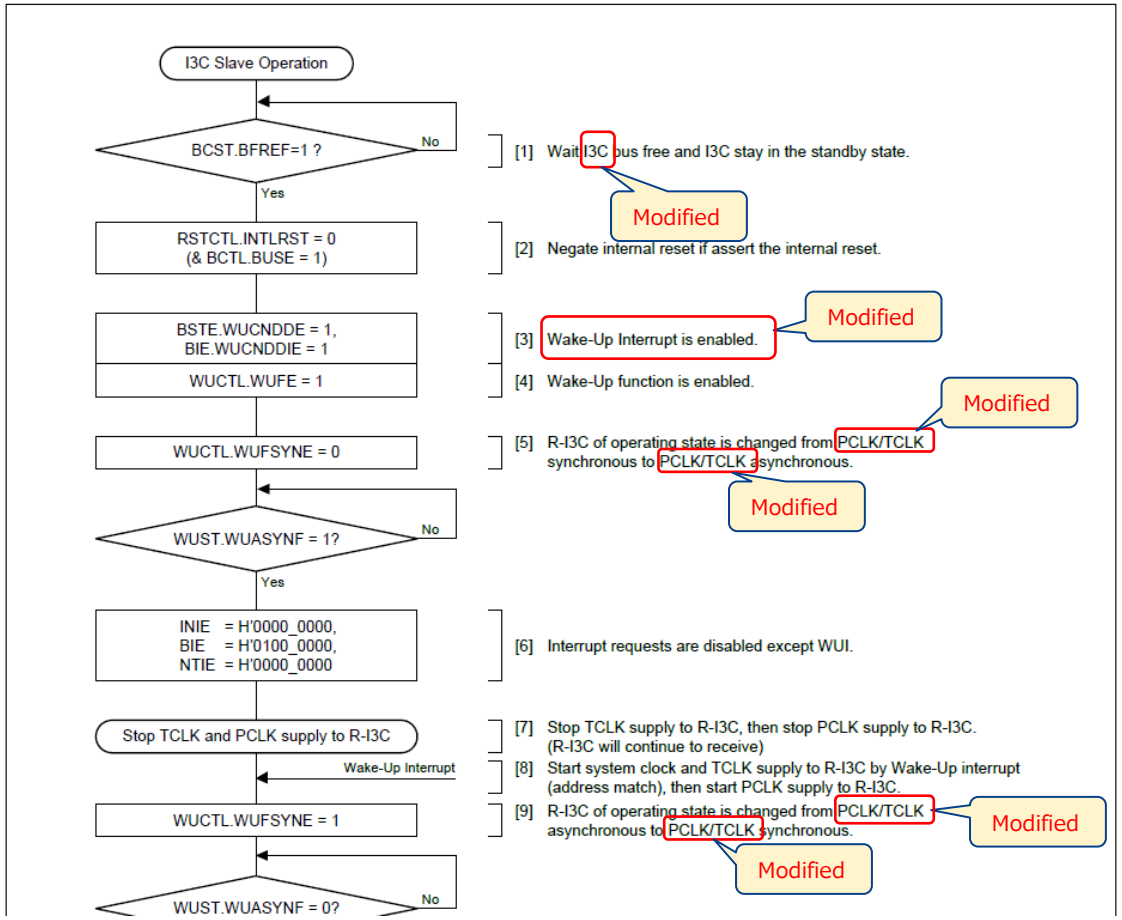


Figure 26.134 Use Case of I3C Slave Wake-Up
(Wake-Up Recovery by a Wake-Up Interrupt Triggered by the Match of the Slave Address)

Before

26.4 Interrupt Sources

26.4.1 Overview

Table 26.17 Interrupt Generation

Symbol	Interrupt Source		Interrupt Flag	Support			
				I²C	I3CM	I3C2M	I3CS
I3C_RESP	Normal response status buffer full		NTST.RSPQFF	—	✓	✓	✓
I3C_CMD	Normal command buffer empty		NTST.CMDQEF	—	✓	✓	✓
I3C_IBI	Normal IBI status buffer empty/full		NTST.IBIQEFF	—	✓	✓	✓
I3C_RX	Normal receive data buffer empty/full		NTST.RDBEF0	✓	✓	✓	✓
I3C_TX	Normal transmit data buffer empty		NTST.TDBEF0	✓	✓	✓	✓
I3C_RCV	Normal receive status buffer full		NTST.RSQFF	—	—	✓	✓
I3C_TEND	Transmit end		BST.TENDF	✓	—	—	—
I3C_EEI	Transfer error or event occurrence	Start condition detection interrupt	BST.STCNDDF	✓	✓	✓	✓
		STOP condition detection interrupt	BST.SPCNDDF	✓	✓	✓	✓
		HDR Exit Pattern detection interrupt	BST.HDREXDF	—	✓	✓	✓
		NACK detection interrupt	BST.NACKDF	✓	—	—	—
		Arbitration lost interrupt	BST.ALF	✓	—	—	—
		Timeout detection interrupt	BST.TODF	✓	✓	✓	✓
		Wake-Up Condition detection interrupt	BST. WUCNDDF	✓	✓	✓	✓
		Non-recoverable internal error interrupt	INST.INEF	—	✓	✓	✓
		Transfer Error interrupt	NTST.TEF	—	✓	✓	✓
		Transfer Abort interrupt	NTST.TABTF	—	✓	✓	✓

Note: ✓: Support
—: Not support

Note: I²C: I²C Master/Slave (Single Buffer)
I3CM: I3C Master
I3C2M: I3C Secondary Master
I3CS: I3C Slave

After

26.4 Interrupt Sources

26.4.1 Overview

Table 26.17 Interrupt Generation

Symbol	Interrupt Source	Interrupt Flag	Support			
			I²C	I3CM	I3C2M	I3CS
INT_ri3c_resp_n	Normal response status buffer full	NTST.RSPQFF	—	✓	✓	✓
INT_ri3c_cmd_n	Normal command buffer empty	NTST.CMDQEF	—	✓	✓	✓
INT_ri3c_ibi_n	Normal IBI status buffer empty/full	NTST.IBIQEFF	—	✓	✓	✓
INT_ri3c_rx_n	Normal receive data buffer full	NTST.RDBFF0	✓	✓	✓	✓
INT_ri3c_tx_n	Normal transmit data buffer empty	NTST.TDBEF0	✓	✓	✓	✓
INT_ri3c_rcv_n	Normal receive status buffer full	NTST.RSQFF	—	—	✓	✓
INT_ri3c_tend_n	Transmit end	BST.TENDF	✓	—	—	—
INT_ri3c_st_n	Start condition detection	BST.STCNDDF	✓	✓	✓	✓
INT_ri3c_sp_n	STOP condition detection	BST.SPCNDDF	✓	✓	✓	✓
INT_ri3c_nack_n	NACK detection	BST.NACKDF	✓	—	—	—
INT_ri3c_al_n	Arbitration lost	BST.ALF	✓	—	—	—
INT_ri3c_tmo_n	Timeout detection	BST.TODF	✓	✓	✓	✓
INT_ri3c_ierr_n	Non-recoverable internal error	INST.INEF	—	✓	✓	✓
INT_ri3c_terr_n	Transfer Error	NTST.TEF	—	✓	✓	✓
INT_ri3c_abort_n	Transfer Abort	NTST.TABTF	—	✓	✓	✓
INT_ri3c_wu_n	Wake-up condition detection	BST.WUCNDDF	✓	✓	✓	✓

Modified

Note: ✓: Support
—: Not support

Note: I²C: I²C Master/Slave (Single Buffer)
I3CM: I3C Master
I3C2M: I3C Secondary Master
I3CS: I3C Slave

Before

26.5 Reset Descriptions

Table 26.18 Register States When Issuing Each Condition (5/11)

Register symbol	Register bit name	System reset	RSTCTL Register											
			RI3CRST	INTLRST	CMDQRST	RSPQRST	TDBRST	RDBRST	IBQRST	RSQRST	HCMDQRST	HRSPQRST	HTDBRST	HRDBRST
BST	WUCNDDF	In reset	In reset	Saved	Saved	Saved	Saved	Saved	Saved	Saved	Saved	Saved	Saved	Saved
	TODF	In reset	In reset	In reset	Saved	Saved	Saved	Saved	Saved	Saved	Saved	Saved	Saved	Saved
	ALF	In reset	In reset	In reset	Saved	Saved	Saved	Saved	Saved	Saved	Saved	Saved	Saved	Saved
	TENDF	In reset	In reset	In reset	Saved	Saved	Saved	Saved	Saved	Saved	Saved	Saved	Saved	Saved
	NACKDF	In reset	In reset	In reset	Saved	Saved	Saved	Saved	Saved	Saved	Saved	Saved	Saved	Saved
	HDREXDF	In reset	In reset	In reset	Saved	Saved	Saved	Saved	Saved	Saved	Saved	Saved	Saved	Saved
	SPCNDDF	In reset	In reset	In reset	Saved	Saved	Saved	Saved	Saved	Saved	Saved	Saved	Saved	Saved
	STCNDDF	In reset	In reset	In reset	Saved	Saved	Saved	Saved	Saved	Saved	Saved	Saved	Saved	Saved

Deleted

After

26.5 Reset Descriptions

Table 26.18 Register States When Issuing Each Condition (5/11)

Register symbol	Register bit name	System reset	RSTCTL Register											
			RI3CRST	INTLRST	CMDQRST	RSPQRST	TDBRST	RDBRST	IBQRST	RSQRST	HCMDQRST	HRSPQRST	HTDBRST	HRDBRST
BST	WUCNDDF	In reset	In reset	Saved	Saved	Saved	Saved	Saved	Saved	Saved	Saved	Saved	Saved	Saved
	TODF	In reset	In reset	In reset	Saved	Saved	Saved	Saved	Saved	Saved	Saved	Saved	Saved	Saved
	ALF	In reset	In reset	In reset	Saved	Saved	Saved	Saved	Saved	Saved	Saved	Saved	Saved	Saved
	TENDF	In reset	In reset	In reset	Saved	Saved	Saved	Saved	Saved	Saved	Saved	Saved	Saved	Saved
	NACKDF	In reset	In reset	In reset	Saved	Saved	Saved	Saved	Saved	Saved	Saved	Saved	Saved	Saved
	SPCNDDF	In reset	In reset	In reset	Saved	Saved	Saved	Saved	Saved	Saved	Saved	Saved	Saved	Saved
	STCNDDF	In reset	In reset	In reset	Saved	Saved	Saved	Saved	Saved	Saved	Saved	Saved	Saved	Saved

Before

26.5 Reset Descriptions

Table 26.18 Register States When Issuing Each Condition (6/11)

Register symbol	Register bit name	System reset	RSTCTL Register											
			RI3CRST	INTLRST	CMDQRST	RSPQRST	TDBRST	RDBRST	IBIQRST	RSQRST	HCMDQRST	HRSPQRST	HTDBRST	HRDBRST
BSTE	WUCNDDE	In reset	In reset	Saved	Saved	Saved	Saved	Saved	Saved	Saved	Saved	Saved	Saved	Saved
	TODE	In reset	In reset	Saved	Saved	Saved	Saved	Saved	Saved	Saved	Saved	Saved	Saved	Saved
	ALE	In reset	In reset	Saved	Saved	Saved	Saved	Saved	Saved	Saved	Saved	Saved	Saved	Saved
	TENDE	In reset	In reset	Saved	Saved	Saved	Saved	Saved	Saved	Saved	Saved	Saved	Saved	Saved
	NACKDE	In reset	In reset	Saved	Saved	Saved	Saved	Saved	Saved	Saved	Saved	Saved	Saved	Saved
	HOREXDE	In reset	In reset	Saved	Saved	Saved	Saved	Saved	Saved	Saved	Saved	Saved	Saved	Saved
	SPCNDDE	In reset	In reset	Saved	Saved	Saved	Saved	Saved	Saved	Saved	Saved	Saved	Saved	Saved
	STCNDDE	In reset	In reset	Saved	Saved	Saved	Saved	Saved	Saved	Saved	Saved	Saved	Saved	Saved

After

26.5 Reset Descriptions

Table 26.18 Register States When Issuing Each Condition (5/11)

Register symbol	Register bit name	System reset	RSTCTL Register											
			RI3CRST	INTLRST	CMDQRST	RSPQRST	TDBRST	RDBRST	IBIQRST	RSQRST	HCMDQRST	HRSPQRST	HTDBRST	HRDBRST
BSTE	WUCNDDE	In reset	In reset	Saved	Saved	Saved	Saved	Saved	Saved	Saved	Saved	Saved	Saved	Saved
	TODE	In reset	In reset	Saved	Saved	Saved	Saved	Saved	Saved	Saved	Saved	Saved	Saved	Saved
	ALE	In reset	In reset	Saved	Saved	Saved	Saved	Saved	Saved	Saved	Saved	Saved	Saved	Saved
	TENDE	In reset	In reset	Saved	Saved	Saved	Saved	Saved	Saved	Saved	Saved	Saved	Saved	Saved
	NACKDE	In reset	In reset	Saved	Saved	Saved	Saved	Saved	Saved	Saved	Saved	Saved	Saved	Saved
	SPCNDDE	In reset	In reset	Saved	Saved	Saved	Saved	Saved	Saved	Saved	Saved	Saved	Saved	Saved
	STCNDDE	In reset	In reset	Saved	Saved	Saved	Saved	Saved	Saved	Saved	Saved	Saved	Saved	Saved

Deleted

Before

26.5 Reset Descriptions

Table 26.18 Register States When Issuing Each Condition (6/11)

Register symbol	Register bit name	System reset	RSTCTL Register											
			RI3CRST	INTLRST	CMDQRST	RSPQRST	TDBRST	RDBRST	IBIQRST	RSQRST	HCMDQRST	HRSPQRST	HTDBRST	HRDBRST
BIE	WUCNDDIE	In reset	In reset	Saved	Saved	Saved	Saved	Saved	Saved	Saved	Saved	Saved	Saved	Saved
	TODIE	In reset	In reset	Saved	Saved	Saved	Saved	Saved	Saved	Saved	Saved	Saved	Saved	Saved
	ALIE	In reset	In reset	Saved	Saved	Saved	Saved	Saved	Saved	Saved	Saved	Saved	Saved	Saved
	TENDIE	In reset	In reset	Saved	Saved	Saved	Saved	Saved	Saved	Saved	Saved	Saved	Saved	Saved
	NACKDIE	In reset	In reset	Saved	Saved	Saved	Saved	Saved	Saved	Saved	Saved	Saved	Saved	Saved
	HDREXDIE	In reset	In reset	Saved	Saved	Saved	Saved	Saved	Saved	Saved	Saved	Saved	Saved	Saved
	SPCNDDIE	In reset	In reset	Saved	Saved	Saved	Saved	Saved	Saved	Saved	Saved	Saved	Saved	Saved
	STCNDDIE	In reset	In reset	Saved	Saved	Saved	Saved	Saved	Saved	Saved	Saved	Saved	Saved	Saved
BSTFC	WUCNDDFC	In reset	In reset	Saved	Saved	Saved	Saved	Saved	Saved	Saved	Saved	Saved	Saved	Saved
	TODFC	In reset	In reset	Saved	Saved	Saved	Saved	Saved	Saved	Saved	Saved	Saved	Saved	Saved
	ALFC	In reset	In reset	Saved	Saved	Saved	Saved	Saved	Saved	Saved	Saved	Saved	Saved	Saved
	TENDFC	In reset	In reset	Saved	Saved	Saved	Saved	Saved	Saved	Saved	Saved	Saved	Saved	Saved
	NACKDFC	In reset	In reset	Saved	Saved	Saved	Saved	Saved	Saved	Saved	Saved	Saved	Saved	Saved
	HDREXDFC	In reset	In reset	Saved	Saved	Saved	Saved	Saved	Saved	Saved	Saved	Saved	Saved	Saved
	SPCNDDFC	In reset	In reset	Saved	Saved	Saved	Saved	Saved	Saved	Saved	Saved	Saved	Saved	Saved
	STCNDDFC	In reset	In reset	Saved	Saved	Saved	Saved	Saved	Saved	Saved	Saved	Saved	Saved	Saved

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After

26.5 Reset Descriptions

Table 26.18 Register States When Issuing Each Condition (6/11)

Register symbol	Register bit name	System reset	RSTCTL Register											
			RI3CRST	INTLRST	CMDQRST	RSPQRST	TDBRST	RDBRST	IBIQRST	RSQRST	HCMDQRST	HRSPQRST	HTDBRST	HRDBRST
BIE	WUCNDDIE	In reset	In reset	Saved	Saved	Saved	Saved	Saved	Saved	Saved	Saved	Saved	Saved	Saved
	TODIE	In reset	In reset	Saved	Saved	Saved	Saved	Saved	Saved	Saved	Saved	Saved	Saved	Saved
	ALIE	In reset	In reset	Saved	Saved	Saved	Saved	Saved	Saved	Saved	Saved	Saved	Saved	Saved
	TENDIE	In reset	In reset	Saved	Saved	Saved	Saved	Saved	Saved	Saved	Saved	Saved	Saved	Saved
	NACKDIE	In reset	In reset	Saved	Saved	Saved	Saved	Saved	Saved	Saved	Saved	Saved	Saved	Saved
	SPCNDDIE	In reset	In reset	Saved	Saved	Saved	Saved	Saved	Saved	Saved	Saved	Saved	Saved	Saved
	STCNDDIE	In reset	In reset	Saved	Saved	Saved	Saved	Saved	Saved	Saved	Saved	Saved	Saved	Saved
BSTFC	WUCNDDFC	In reset	In reset	Saved	Saved	Saved	Saved	Saved	Saved	Saved	Saved	Saved	Saved	Saved
	TODFC	In reset	In reset	Saved	Saved	Saved	Saved	Saved	Saved	Saved	Saved	Saved	Saved	Saved
	ALFC	In reset	In reset	Saved	Saved	Saved	Saved	Saved	Saved	Saved	Saved	Saved	Saved	Saved
	TENDFC	In reset	In reset	Saved	Saved	Saved	Saved	Saved	Saved	Saved	Saved	Saved	Saved	Saved
	NACKDFC	In reset	In reset	Saved	Saved	Saved	Saved	Saved	Saved	Saved	Saved	Saved	Saved	Saved
	SPCNDDFC	In reset	In reset	Saved	Saved	Saved	Saved	Saved	Saved	Saved	Saved	Saved	Saved	Saved
	STCNDDFC	In reset	In reset	Saved	Saved	Saved	Saved	Saved	Saved	Saved	Saved	Saved	Saved	Saved

Before

26.6 Usage Notes

26.6.1 Settings for the Operating Clock

The clock frequency ratio of PCLKD and PCLKB must be 2:1 or 1:1 when using the I3C module. Operation is not guaranteed for other settings.

After

26.6 Usage Notes

Deleted