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RENESAS TECHNICAL UPDATE

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Product Category	MPU/MCU		Document No.	TN-RZ*-A0141A/E	Rev.	1.00
Title	- PCIe REFCLK input architecture restriction. - I3C initialization setting flow correction. - Addition to xSPI AC specifications.		Information Category	Technical Notification		
Applicable Product	RZ/G3S Group	Lot No. All lots	Reference Document	RZ/G3S Group User's Manual: Hardware Rev.1.10		

[Title]
PCIe REFCLK input architecture restriction.

[Phenomenon]
The document does not specify which of the three REFCLK input architecture (Common, SRNS, or SRIS).

[User's manual Update]
PCIe REFCLK input architecture is limited to Common and SRNS Clock.

User's Manual
34 PCI Express 3.0 Interface (PCIe)
34.1 Overview
PCI Express Specification (Compliant with the PCI Express Base Specification 4.0)

[From]

■ **PCI Express Specification (Compliant with the PCI Express Base Specification 4.0)**

- PCI Express Gen1(2.5[GT/s])/Gen2(5.0[GT/s])
- Root Complex Applications, Type1 Configuration Register
- Lane implementation x1
- Support Polarity inversion
- Maximum data payload of 256 bytes, Maximum read request size 512 bytes
- Not support for Virtual channels (support VC0 only)
- Number of outstanding 1-8
- Dynamic control of speed/width up/down configuration
- Not support for Clock Power Management (not support P1.CPM, P2.CPM)
- Power Management (ASPM L1-Substate Support (Support PowerDown Sequence only))
- Error handling/logging (AER Support)
- Replay FIFO with ECC
- Internal Memory without Parity
- Number of Support Functions 1

[To]

■ **PCI Express Specification (Compliant with the PCI Express Base Specification 4.0)**

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- Internal Memory without Parity
- Number of Support Functions 1
- **Supported reference clock architecture**
  - Common and SRNS

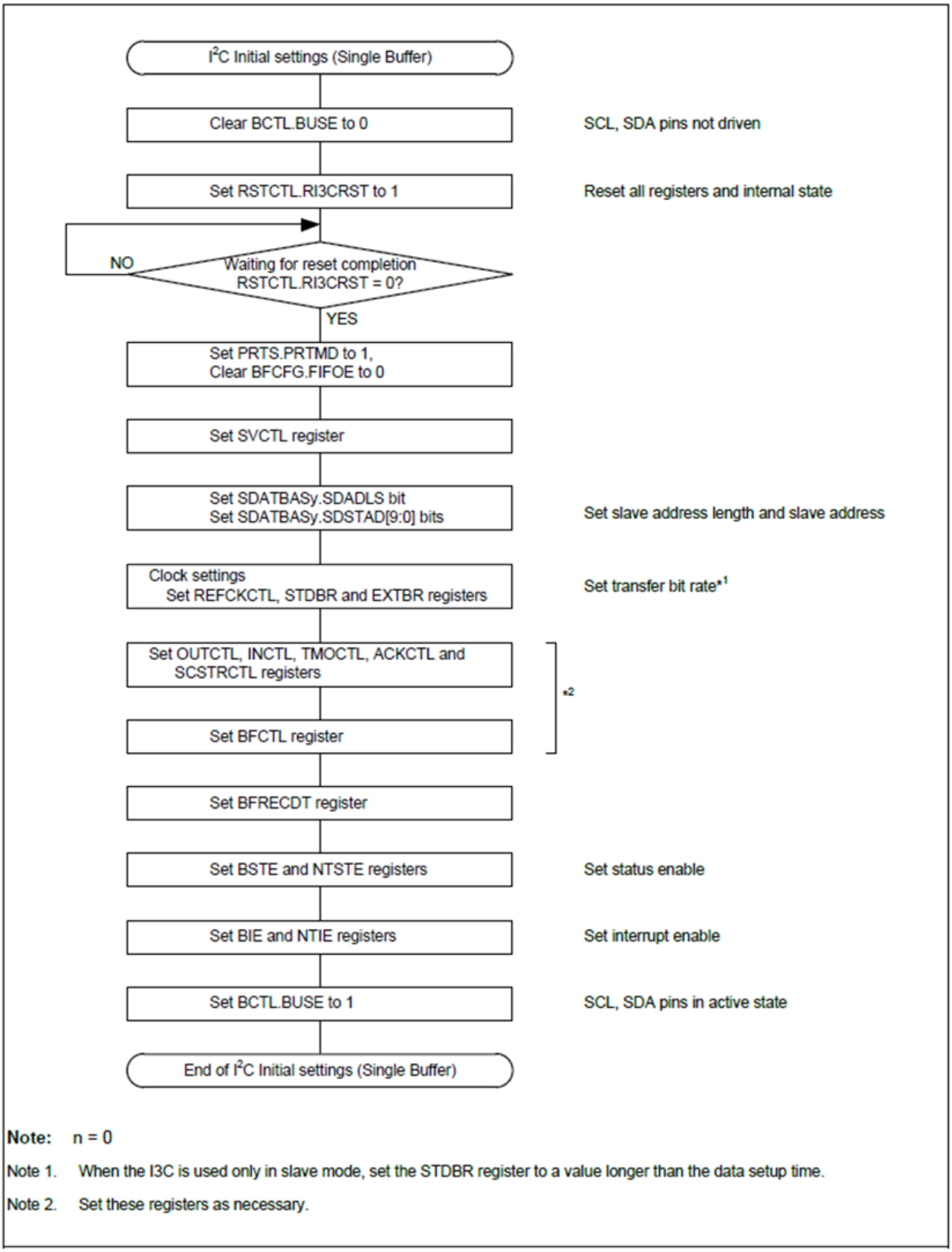
[Title]
I3C initialization setting flow correction.

[Phenomenon]
In the current initialization flow, the initial state of the communication I/F pins may become unstable.

[User’s manual Update]
Add an internal reset assert to the initialization flow to mask the unstable period of the I/F pins.

User’s Manual
26 I3C Bus Interface (I3C)
26.3.3.1 Initial Setting Flow
Figure 26.115 Example of I2C Initialization Flowchart (Single Buffer Transfer)

[From]



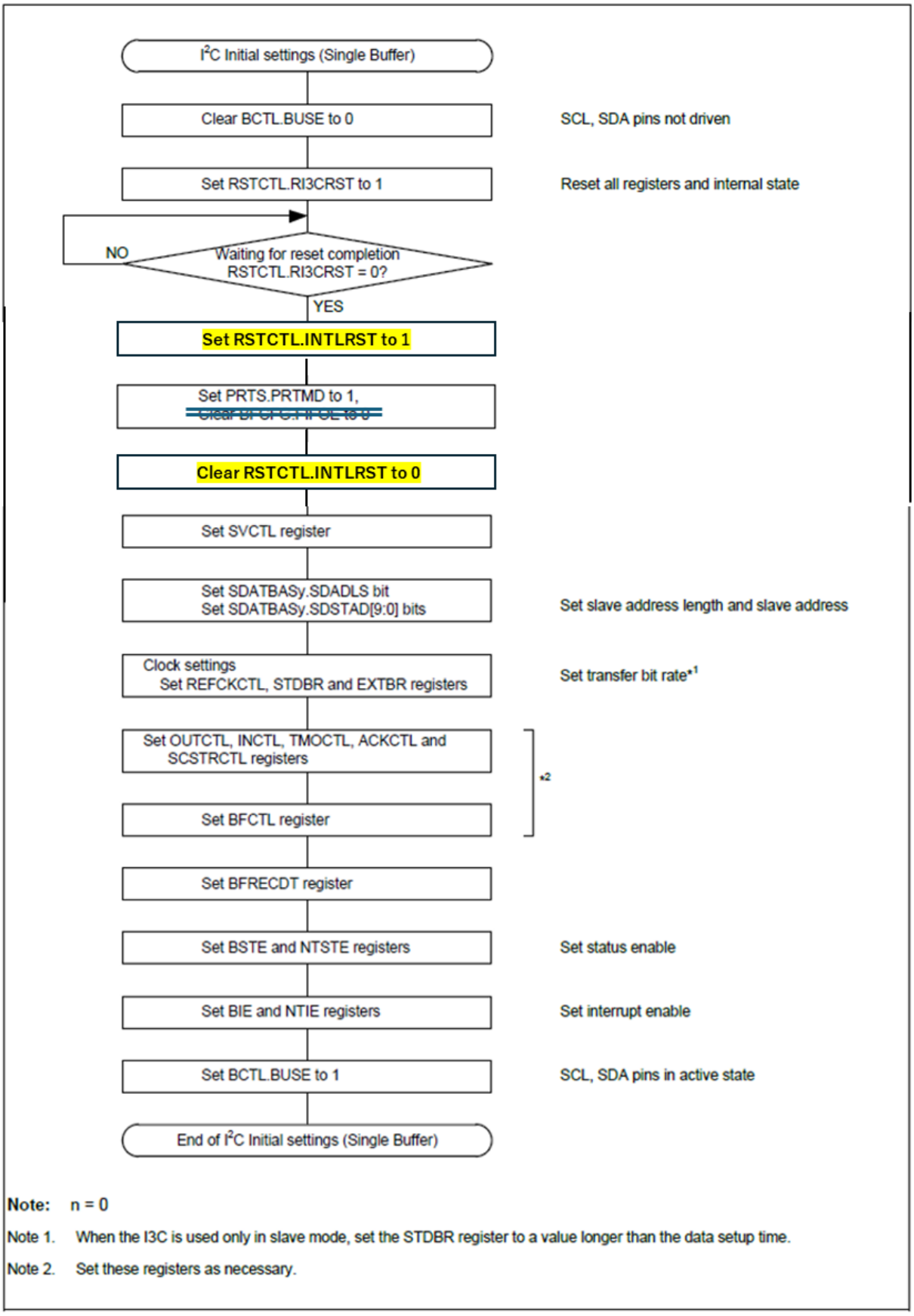
Note: n = 0

Note 1. When the I3C is used only in slave mode, set the STDBR register to a value longer than the data setup time.

Note 2. Set these registers as necessary.

Figure 26.115 Block Diagram of Digital Noise Filter Circuit

[To]



Note: n = 0

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Note 2. Set these registers as necessary.

Figure 26.115 **Example of I2C Initialization Flowchart (Single Buffer Transfer)**

User’s Manual
26 I3C Bus Interface (I3C)
26.3.3.1 Initial Setting Flow
Figure 26-116 Example of I3C Initialization Flowchart

[From]

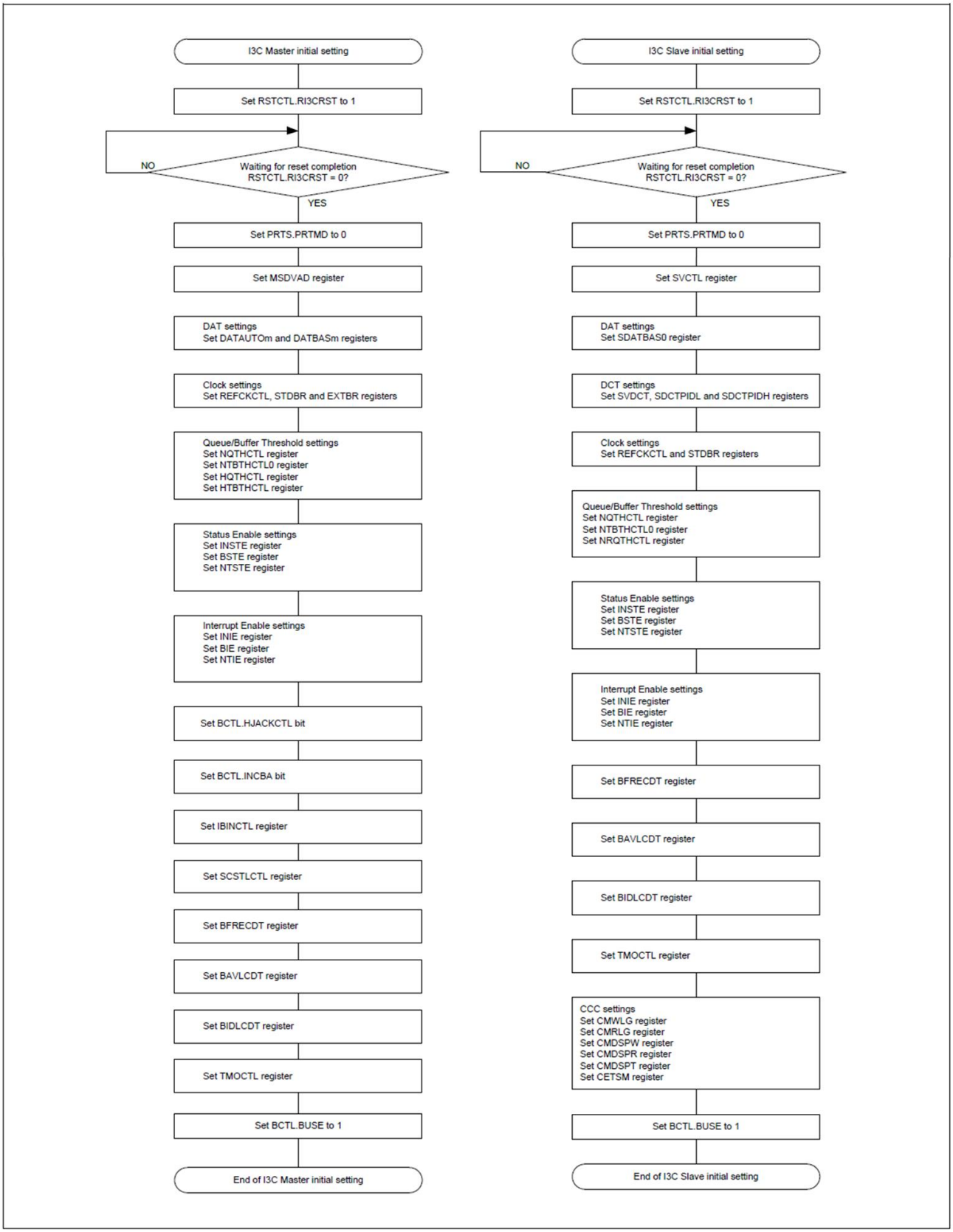

Figure 26.116 Example of I3C Initialization Flowchart

[To]

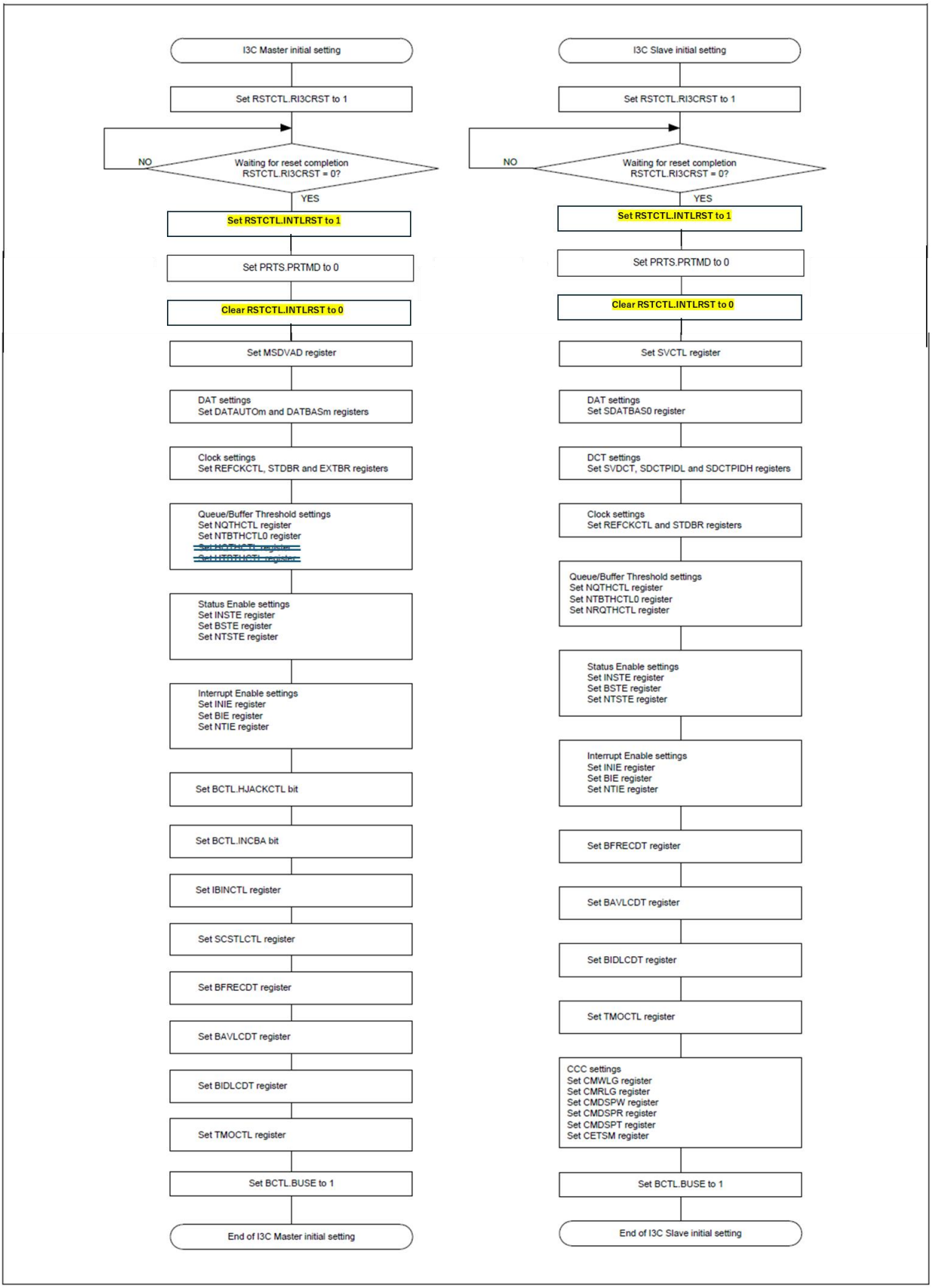

Figure 26.116 Example of I3C Initialization Flowchart

[Title]
Addition to xSPI AC specifications.

[Phenomenon]
There is a possibility of malfunction due to capturing the DS signal (intermediate voltage) immediately after the CS signal falls.

[User's manual Update]
Define the maximum value of t_{CSLDSL} as the corresponding specification. If this AC specification is not met and JESD251 Profile 1.0 memory or Profile 2.0 memory is used, the internal pull-down of the IOBUFF must be enabled before starting the access.

User's Manual
47 Electrical Characteristics
47.5 AC Characteristics
47.5.8 xSPI Timing

[From]

Table 47.27 xSPI Timing

Item		Symbol	1.8 V		3.3 V		Unit	Figures
			Min.	Max.	Min.	Max.		
Clock cycle	SDR	t_{SPBcyc}	15	—	15	—	ns	**Figure 47.28**
	DDR		7.5	—	—	—	ns	
Clock output slew rate		t_{SRck}	0.75/0.56*2	—	1.03*6	—	V/ns	
Clock minimum pulse width		t_{CKMPW}	t_{PERIOD} × 0.45	—	t_{PERIOD} × 0.45	—	ns	
DS duty cycle distortion		t_{DSDCD}	0.0	t_{PERIOD} × 0.04	0.0	t_{PERIOD} × 0.04	ns	
DS minimum pulse width		t_{DSMPW}	t_{PERIOD} × 0.41	—	t_{PERIOD} × 0.41	—	ns	
Data input/output slew rate		t_{SR}	0.75/0.56*2	—	1.03*6	—	V/ns	
Data input setup time (to CK)	SDR	t_{SU}	5.0	—	5.0	—	ns	**Figure 47.29**
Data input hold time (to CK)		t_H	1.0	—	1.0	—	ns	
Data output delay time	SDR	t_{OD}	—	8.32*3	—	8.32*3	ns	
	DDR		—	1	—	—	ns	
Data output hold time	SDR	t_{OH}	4.8	—	4.8	—	ns	
	DDR		−1	—	—	—	ns	
Data output buffer off time	SDR	t_{BOFF}	4.8	—	4.8	—	ns	
	DDR		−1	—	—	—	ns	
Data input setup time (to DS)	DDR*1,*3	t_{SU}	−0.6/−0.8	—	−0.6/−0.8	—	ns	**Figure 47.30**
Data input hold time (to DS)		t_H	t_{PERIOD} × 0.41 − 0.6/0.8	—	t_{PERIOD} × 0.41 − 0.6/0.8	—	ns	
Data output setup time (to CK)		t_{SUO}	0.6*5	—	1.0	—	ns	
Data output hold time (to CK)		t_{HO}	0.6*5	—	1.0	—	ns	
CS low to clock high		t_{CSLCKH}	6.0/8.0*2,*4	—	8.0*4	—	ns	**Figure 47.29, Figure 47.30**
Clock low to CS high		t_{CKLCSH}	6.0/8.0*2	—	8.0	—	ns	
CS high time		t_{CSTD}	1	16	1	16	t_{PERIOD}	
DS low to CS high		t_{DSLCSH}	6.0/8.0*2	—	10.6	—	ns	**Figure 47.31**
CS high to DS Tri-state		t_{CSHDST}	0.0	t_{PERIOD}	0.0	t_{PERIOD}	ns	
CS low to DS low		t_{CSLDSL}	0.0	—	0.0	—	ns	
DS Tri-state to CS low		t_{DSTCSL}	0.0	—	0.0	—	ns	

Remarks: CK: XSPI_SPCLK
DS: XSPI_DS
CS: XSPI_CS0#, XSPI_CS1#

Note 1. The DS shift setting (WRAPCFG.DSSFTCSx[4:0]) is 0_1000b for xSPI200.

Note 2. Specification at 133 MHz / Specification at 100 MHz

Note 3. These are values when the OEN assertion is extended in the Output Enable Asserting extension bit (COMCFG.OEASTEX = 1b).

Note 4. These are the values when the CS assertion is extended in the CS asserting extension bit (LIOCFGCSn.CSASTEX = 1b) and the CS negation is extended in CS negating extension bit.

Note 5. The standard value for xSPI266 is 0.8 ns.

Note 6. When IOLH register is 10b or more.

[To]

Table 47.27 xSPI Timing

Item		Symbol	1.8 V		3.3 V		Unit	Figures
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DS duty cycle distortion		t_{DSDCD}	0.0	t_{PERIOD} × 0.04	0.0	t_{PERIOD} × 0.04	ns	
DS minimum pulse width		t_{DSMPW}	t_{PERIOD} × 0.41	—	t_{PERIOD} × 0.41	—	ns	
Data input/output slew rate		t_{SR}	0.75/0.56*2	—	1.03*6	—	V/ns	
Data input setup time (to CK)	SDR	t_{SU}	5.0	—	5.0	—	ns	**Figure 47.29**
Data input hold time (to CK)		t_{H}	1.0	—	1.0	—	ns	
Data output delay time	SDR	t_{OD}	—	8.32*3	—	8.32*3	ns	
	DDR		—	1	—	—	ns	
Data output hold time	SDR	t_{OH}	4.8	—	4.8	—	ns	
	DDR		−1	—	—	—	ns	
Data output buffer off time	SDR	t_{BOFF}	4.8	—	4.8	—	ns	
	DDR		−1	—	—	—	ns	
Data input setup time (to DS)	DDR*1,*3	t_{SU}	−0.6/−0.8	—	−0.6/−0.8	—	ns	**Figure 47.30**
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Data output setup time (to CK)		t_{SUO}	0.6*5	—	1.0	—	ns	
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CS low to clock high		t_{CSLCKH}	6.0/8.0*2,*4	—	8.0*4	—	ns	**Figure 47.29, Figure 47.30**
Clock low to CS high		t_{CKLCSH}	6.0/8.0*2	—	8.0	—	ns	
CS high time		t_{CSTD}	1	16	1	16	t_{PERIOD}	
DS low to CS high		t_{DSLCSH}	6.0/8.0*2	—	10.6	—	ns	**Figure 47.31**
CS high to DS Tri-state		t_{CSHDST}	0.0	t_{PERIOD}	0.0	t_{PERIOD}	ns	
CS low to DS low *7		t_{CSLDSL}	0.0	12.5*8	0.0	17.4*8	ns	
DS Tri-state to CS low		t_{DSTCSL}	0.0	—	0.0	—	ns	

Remarks: CK: XSPI_SPCLK
DS: XSPI_DS
CS: XSPI_CS0#, XSPI_CS1#

Note 1. The DS shift setting (WRAPCFG.DSSFTCSx[4:0]) is 0_1000b for xSPI200.

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Note 5. The standard value for xSPI266 is 0.8 ns.

Note 6. When IOLH register is 10b or more.

Note 7. If the DS is high during the command & modifier phase when using JESD251 Profile 2.0 memory, the time from CS low to DS high must also meet this specification.

Note 8. When using JESD251 Profile 1.0 memory or JESD251 Profile 2.0 memory with LIOCFGCSn.LATEMD set to 0, this constraint does not apply if the internal pull-down resistor of the DS pin is enabled.