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RENESAS TECHNICAL UPDATE

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Product Category	MPU/MCU		Document No.	TN-RZ*-A0139A/E	Rev.	1.00
Title	User's Manual Hardware correction : Delete Sampling Rate Converter (SRC)		Information Category	Technical Notification		
Applicable Product	RZ/G2L Group, RZ/G2LC Group RZ/V2L Group RZ/G2UL Group RZ/Five Group RZ/G3S Group	Lot No. All lots	Reference Document	R01UH0914EJ0145 R01UH0936EJ0145 R01UH0968EJ0130 R01UH0986EJ0120 R01UH1014EJ0110		

This technical update describes document corrections of the following User's Manual: Hardware.

RZ/G2L Group, RZ/G2LC Group User's Manual: Hardware Rev.1.45 (R01UH0914EJ0145)

RZ/V2L Group User's Manual: Hardware Rev.1.45 (R01UH0936EJ0145)

RZ/G2UL Group User's Manual: Hardware Rev.1.30 (R01UH0968EJ0130)

RZ/Five Group User's Manual: Hardware Rev.1.20 (R01UH0986EJ0120)

RZ/G3S Group User's Manual: Hardware Rev.1.10 (R01UH1014EJ0110)

The following table shows the outline of the corrections.

Chapter No.	Title of chapter	Description
1	Overview	Delete descriptions related to SRC
5	LSI Internal Bus	Delete descriptions related to SRC
6	System Controller (SYSC)	Delete descriptions related to SRC
7	Clock Pulse Generator (CPG)	Delete descriptions related to SRC
8	Interrupt Controller	Delete descriptions related to SRC
14	Direct Memory Controller	Delete descriptions related to SRC
29 (except RZ/G3S) 36 (RZ/G3S)	Sampling Rate Converter (SRC)	Delete chapter
42 (except RZ/G3S) 41 (RZ/G3S)	Low Power Mode	Delete descriptions related to SRC

The detailed corrections information is described from next page.

Section 1. Overview

- **1.2.9 Sound Interface : [RZ/G2L,LC, RZ/V2L]**
- **1.2.8 Sound Interface : [RZ/G2UL]**
- **1.2.5 Sound Interface : [RZ/Five, RZ/G3S]**

The following descriptions are deleted.

[From]

Item	Description
Serial Sound Interface (SSI)	[RZ/G2L] • 4 channels bidirectional serial transfer [RZ/G2LC] • 3 channels bidirectional serial transfer [RZ/G2L RZ/G2LC] • 2 external clock sources available • Full Duplex communication (channel 0, 1, and 3) • Support of I2S / Monaural / TDM audio formats • Support of master and slave functions • Generation of programmable word clock and bit clock • Multi-channel formats • Support of 8, 16, 18, 20, 22, 24, and 32-bit data formats • Support of 32-stage FIFO for transmission and reception • Support of LR-clock continue function in which the LR-clock signal is not stopped
Sampling Rate Converter (SRC)	[RZ/ G2L RZ/G2LC] • 1 channel • Data format: 16-bit (stereo / monaural) • Sampling Rate Input: Selectable from 8 kHz, 11.025 kHz, 12 kHz, 16 kHz, 22.05 kHz, 24 kHz, 32 kHz, 44.1 kHz, 48 kHz Output: Selectable from 8 kHz*, 16 kHz*, 32 kHz, 44.1 kHz, 48 kHz (*: can select in 44.1 kHz input mode) • SNR: More than or equal to 80 db

[To]

Item	Description
Serial Sound Interface (SSI)	[RZ/G2L] • 4 channels bidirectional serial transfer [RZ/G2LC] • 3 channels bidirectional serial transfer [RZ/G2L RZ/G2LC] • 2 external clock sources available • Full Duplex communication (channel 0, 1, and 3) • Support of I2S / Monaural / TDM audio formats • Support of master and slave functions • Generation of programmable word clock and bit clock • Multi-channel formats • Support of 8, 16, 18, 20, 22, 24, and 32-bit data formats • Support of 32-stage FIFO for transmission and reception • Support of LR-clock continue function in which the LR-clock signal is not stopped
Sampling Rate Converter (SRC)	[RZ/ G2L RZ/G2LC] • 1 channel • Data format: 16-bit (stereo / monaural) • Sampling Rate Input: Selectable from 8 kHz, 11.025 kHz, 12 kHz, 16 kHz, 22.05 kHz, 24 kHz, 32 kHz, 44.1 kHz, 48 kHz Output: Selectable from 8 kHz*, 16 kHz*, 32 kHz, 44.1 kHz, 48 kHz (*: can select in 44.1 kHz input mode) • SNR: More than or equal to 80 db

Delete

Section 5. LSI Internal Bus

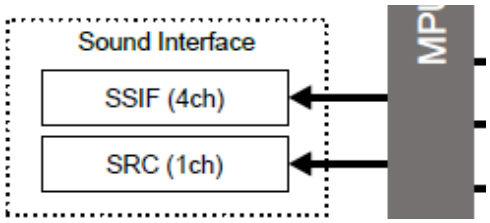
■ 5.1.2 Block Diagram of LSI Internal Bus

The following descriptions are deleted.

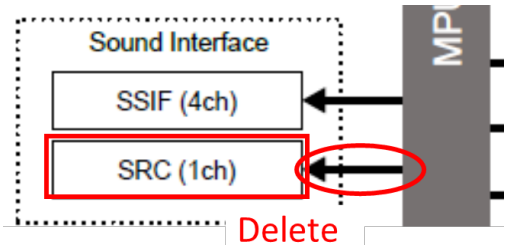
- **[RZ/G2L,LC, RZ/V2L, RZ/G2UL, RZ/Five]**

Figure 5.1 Configuration of LSI Internal Bus

[From]



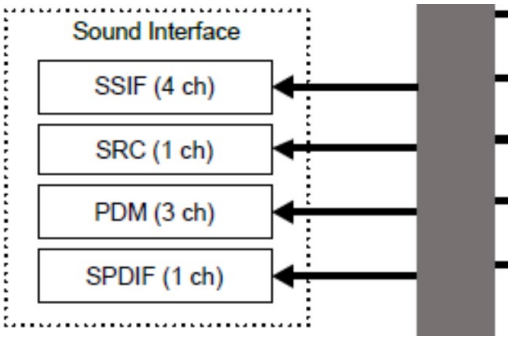
[To]



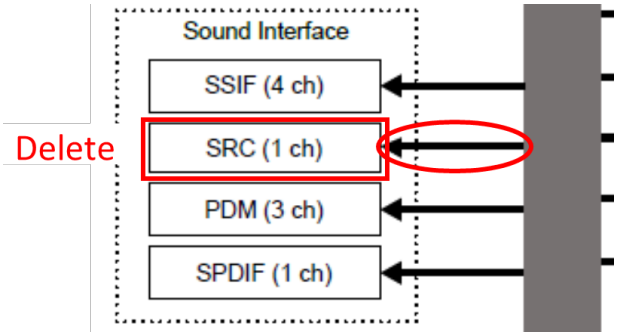
■ **[RZ/G3S]**

Figure 5.1 Configuration of LSI Internal Bus

[From]



[To]



■ 5.2.1 Overall Address Space

The following descriptions are fixed.

- **[RZ/G2L,LC, RZ/V2L, RZ/G2UL, RZ/Five]**

Table 5.1 Detailed Address Space (3/3)

[From]

H'0_1004_7000	H'0_1004_7FFF	4	Kbytes	SRC (Reg)
H'0_1004_0000	H'0_1004_6FFF	28	Kbytes	SRC (Memory)

[To]

H'0_1004_7000	H'0_1004_7FFF	4	Kbytes	Reserved
H'0_1004_0000	H'0_1004_6FFF	28	Kbytes	Reserved

- **[RZ/G3S]**

Table 5.1 Detailed Address Space (3/4)

[From]

H'0_100A_7000	H'0_100A_7FFF	4	Kbytes	SRC (Reg)
H'0_100A_0000	H'0_100A_6FFF	28	Kbytes	SRC (Memory)

[To]

H'0_100A_7000	H'0_100A_7FFF	4	Kbytes	Reserved
H'0_100A_0000	H'0_100A_6FFF	28	Kbytes	Reserved

■ 5.2.2 Cortex-M33 Address Space

The following descriptions are fixed.

- **[RZ/G2L,LC, RZ/V2L, RZ/G2UL]**

[From]

Table 5.2 Detailed Address Space of Cortex-M33 (3/6)

H'5004_7000	H'5004_7FFF	4	Kbytes	SRC (Reg) (Secure)
H'5004_0000	H'5004_6FFF	28	Kbytes	SRC (Memory) (Secure)

Table 5.2 Detailed Address Space of Cortex-M33 (6/6)

H'4004_7000	H'4004_7FFF	4	Kbytes	SRC (Reg) (Non-Secure)
H'4004_0000	H'4004_6FFF	28	Kbytes	SRC (Memory) (Non-Secure)

[To]

Table 5.2 Detailed Address Space of Cortex-M33 (3/6)

H'5004_7000	H'5004_7FFF	4	Kbytes	Reserved
H'5004_0000	H'5004_6FFF	28	Kbytes	Reserved

Table 5.2 Detailed Address Space of Cortex-M33 (6/6)

H'4004_7000	H'4004_7FFF	4	Kbytes	Reserved
H'4004_0000	H'4004_6FFF	28	Kbytes	Reserved

- **[RZ/G3S]**

[From]

Table 5.2 Detailed Address Space of Cortex-M33/Cortex-M33_FPU (3/8)

H'500A_7000	H'500A_7FFF	4	Kbytes	SRC (Reg) (Non-Secure)
H'500A_0000	H'500A_6FFF	28	Kbytes	SRC (Memory) (Non-Secure)

Table 5.2 Detailed Address Space of Cortex-M33/Cortex-M33_FPU (6/8)

H'400A_7000	H'400A_7FFF	4	Kbytes	SRC (Reg) (Secure)
H'400A_0000	H'400A_6FFF	28	Kbytes	SRC (Memory) (Secure)

[To]

Table 5.2 Detailed Address Space of Cortex-M33/Cortex-M33_FPU (3/8)

H'500A_7000	H'500A_7FFF	4	Kbytes	Reserved
H'500A_0000	H'500A_6FFF	28	Kbytes	Reserved

Table 5.2 Detailed Address Space of Cortex-M33/Cortex-M33_FPU (6/8)

H'400A_7000	H'400A_7FFF	4	Kbytes	Reserved
H'400A_0000	H'400A_6FFF	28	Kbytes	Reserved

■ 5.3 Accessible Areas

The following descriptions are deleted.

- **[RZ/G2L,LC, RZ/V2L]**

Table 5.3 Accessible Areas (1/2)

[From]

POEGA	✓	×	✓	✓	✓	✓	×	×	×	×	×	×	×	×
POEGB	✓	×	✓	✓	✓	✓	×	×	×	×	×	×	×	×
POEGC	✓	×	✓	✓	✓	✓	×	×	×	×	×	×	×	×
POEGD	✓	×	✓	✓	✓	✓	×	×	×	×	×	×	×	×
GPT	✓	×	✓	✓	✓	✓	×	×	×	×	×	×	×	×
SRC (Memory/Reg)	✓	×	✓	✓	✓	✓	×	×	×	×	×	×	×	×
POE3	✓	×	✓	✓	✓	✓	×	×	×	×	×	×	×	×
MTU3a	✓	×	✓	✓	✓	✓	×	×	×	×	×	×	×	×

[To]

POEGA	✓	×	✓	✓	✓	✓	×	×	×	×	×	×	×	×
POEGB	✓	×	✓	✓	✓	✓	×	×	×	×	×	×	×	×
POEGC	✓	×	✓	✓	✓	✓	×	×	×	×	×	×	×	×
POEGD	✓	×	✓	✓	✓	✓	×	×	×	×	×	×	×	×
GPT	✓	×	✓	✓	✓	✓	×	×	×	×	×	×	×	×
SRC (Memory/Reg)	✓	×	✓	✓	✓	✓	×	×	×	×	×	×	×	×
POE3	✓	×	✓	✓	✓	✓	×	×	×	×	×	×	×	×
MTU3a	✓	×	✓	✓	✓	✓	×	×	×	×	×	×	×	×

Delete

- **[RZ/G2UL, RZ/Five]**

Table 5.3 Accessible Areas (1/2)

[From]

CANFD	✓	✓	✓	✓	✓	×	×	×	×	×	×	×
ADC	✓	✓	✓	✓	✓	×	×	×	×	×	×	×
TSU	✓	✓	✓	✓	✓	×	×	×	×	×	×	×
SRC (Memory/Reg)	✓	✓	✓	✓	✓	×	×	×	×	×	×	×
POE3	✓	✓	✓	✓	✓	×	×	×	×	×	×	×
MTU3a	✓	✓	✓	✓	✓	×	×	×	×	×	×	×

[To]

CANFD	✓	✓	✓	✓	✓	×	×	×	×	×	×	×
ADC	✓	✓	✓	✓	✓	×	×	×	×	×	×	×
TSU	✓	✓	✓	✓	✓	×	×	×	×	×	×	×
SRC (Memory/Reg)	✓	✓	✓	✓	✓	×	×	×	×	×	×	×
POE3	✓	✓	✓	✓	✓	×	×	×	×	×	×	×
MTU3a	✓	✓	✓	✓	✓	×	×	×	×	×	×	×

Delete

- **[RZ/G3S]**

Table 5.3 Accessible Areas (1/2)

[From]

POEGA	✓	✓	✓	✓	✓	✓	×	×	×	×	×
POEGB	✓	✓	✓	✓	✓	✓	×	×	×	×	×
POEGC	✓	✓	✓	✓	✓	✓	×	×	×	×	×
POEGE	✓	✓	✓	✓	✓	✓	×	×	×	×	×
GPT	✓	✓	✓	✓	✓	✓	×	×	×	×	×
GPT_ELC	✓	✓	✓	✓	✓	✓	×	×	×	×	×
SRC (Memory/Reg)	✓	✓	✓	✓	✓	✓	×	×	×	×	×
SPDIF	✓	✓	✓	✓	✓	✓	×	×	×	×	×
PDM	✓	✓	✓	✓	✓	✓	×	×	×	×	×

[To]

POEGA	✓	✓	✓	✓	✓	✓	×	×	×	×	×
POEGB	✓	✓	✓	✓	✓	✓	×	×	×	×	×
POEGC	✓	✓	✓	✓	✓	✓	×	×	×	×	×
POEGE	✓	✓	✓	✓	✓	✓	×	×	×	×	×
GPT	✓	✓	✓	✓	✓	✓	×	×	×	×	×
GPT_ELC	✓	✓	✓	✓	✓	✓	×	×	×	×	×
SRC (Memory/Reg)	✓	✓	✓	✓	✓	✓	×	×	×	×	×
SPDIF	✓	✓	✓	✓	✓	✓	×	×	×	×	×
PDM	✓	✓	✓	✓	✓	✓	×	×	×	×	×

Delete

■ 5.4.1.2 Determining the Security Levels of Bus Slaves]

The following descriptions are deleted.

- **[RZ/G2L,LC, RZ/V2L, RZ/G2UL]**

Table 5.7 Bus Slaves for which the Security Levels are Determined by Using the Slave Control Registers (2/2)

- **[RZ/Five]**

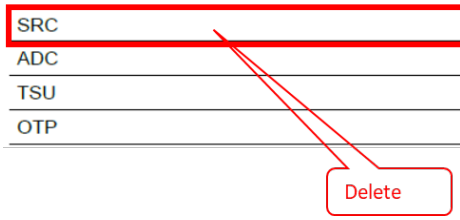
Table 5.6 Bus Slaves for which the Security Levels are Determined by Using the Slave Control Registers (2/2)

[From]

SCI (channel 0)	SYS_SLVACCCTL4	Bits [27:26]
SCI (channel 1)	SYS_SLVACCCTL4	Bits [29:28]
SCI (channel 0) (IrDA)	SYS_SLVACCCTL4	Bits [31:30]
SSIF	SYS_SLVACCCTL5	Bits [1:0]
SRC	SYS_SLVACCCTL5	Bits [5:4]
ADC	SYS_SLVACCCTL6	Bits [1:0]
TSU	SYS_SLVACCCTL6	Bits [3:2]
OTP	SYS_SLVACCCTL7	Bits [3:2]

[To]

SCI (channel 0)	SYS_SLVACCCTL4	Bits [27:26]
SCI (channel 1)	SYS_SLVACCCTL4	Bits [29:28]
SCI (channel 0) (IrDA)	SYS_SLVACCCTL4	Bits [31:30]
SSIF	SYS_SLVACCCTL5	Bits [1:0]
SRC	SYS_SLVACCCTL5	Bits [5:4]
ADC	SYS_SLVACCCTL6	Bits [1:0]
TSU	SYS_SLVACCCTL6	Bits [3:2]
OTP	SYS_SLVACCCTL7	Bits [3:2]



- **[RZ/G3S]**

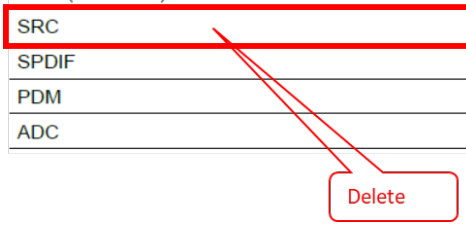
Table 5.7 Bus Slaves for which the Security Levels are Determined by Using the Slave Control Registers (3/3)

[From]

SSIF (channel 0)	SYS_SLVACCCTL9	Bits [1:0]
SSIF (channel 1)	SYS_SLVACCCTL9	Bits [3:2]
SSIF (channel 2)	SYS_SLVACCCTL9	Bits [5:4]
SSIF (channel 3)	SYS_SLVACCCTL9	Bits [7:6]
SRC	SYS_SLVACCCTL9	Bits [9:8]
SPDIF	SYS_SLVACCCTL9	Bits [11:10]
PDM	SYS_SLVACCCTL9	Bits [13:12]
ADC	SYS_SLVACCCTL10	Bits [1:0]

[To]

SSIF (channel 0)	SYS_SLVACCCTL9	Bits [1:0]
SSIF (channel 1)	SYS_SLVACCCTL9	Bits [3:2]
SSIF (channel 2)	SYS_SLVACCCTL9	Bits [5:4]
SSIF (channel 3)	SYS_SLVACCCTL9	Bits [7:6]
SRC	SYS_SLVACCCTL9	Bits [9:8]
SPDIF	SYS_SLVACCCTL9	Bits [11:10]
PDM	SYS_SLVACCCTL9	Bits [13:12]
ADC	SYS_SLVACCCTL10	Bits [1:0]



Section 6. System Controller (SYS)

■ 6.3.11 Slave Access Control Register 5 (SYS_SLVACCCTL5)

The following descriptions are fixed.

- **[RZ/G2L,LC, RZ/V2L, RZ/G2UL, RZ/Five]**

[From]

6.3.11 Slave Access Control Register 5 (SYS_SLVACCCTL5)

This register sets the security levels for determining whether to enable or disable access to each set of registers in the SSIF and SRC.

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—
Initial Value	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
R/W	R	R	R	R	R	R	R	R	R	R	R	R	R	R	R	R

Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
	—	—	—	—	—	—	—	—	—	—	SRC_SL		—	—	SSIF_SL	
Initial Value	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
R/W	R	R	R	R	R	R	R	R	R	R	R/W	R/W	R	R	R/W	R/W

Bit	Bit Name	Initial Value	R/W	Description
31 to 6	—	All 0	R	Reserved Whenever it is read, 0 is read. The written value will be ignored.
5, 4	SRC_SL	00b	R/W	SRC slave access permission control Set the security level SL [1:0] for the slave SRC.
3, 2	—	00b	R	Reserved Whenever it is read, 0 is read. The written value will be ignored.
1, 0	SSIF_SL	00b	R/W	SSIF slave access permission control Set the security level SL [1:0] for the slave SSIF. SSIF has a common security level for channel 0 to channel 3.

[To]

6.3.11 Slave Access Control Register 5 (SYS_SLVACCCTL5)

This register sets the security levels for determining whether to enable or disable access to each set of registers in the SSIF and SRC. Delete

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—
Initial Value	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
R/W	R	R	R	R	R	R	R	R	R	R	R	R	R	R	R	R

Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
	—	—	—	—	—	—	—	—	—	—	—	—	—	—	SSIF_SL	
Initial Value	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
R/W	R	R	R	R	R	R	R	R	R	R	R	R	R	R	R/W	R/W

Bit	Bit Name	Initial Value	R/W	Description
31 to 6	—	All 0	R	Reserved Whenever it is read, 0 is read. The written value will be ignored.
5, 4	—	00b	R	Reserved When read, the initial value is read. When writing, be sure to write the initial value. Operation is not guaranteed if a value other than the initial value is written.
3, 2	—	00b	R	Reserved Whenever it is read, 0 is read. The written value will be ignored.
1, 0	SSIF_SL	00b	R/W	SSIF slave access permission control Set the security level SL [1:0] for the slave SSIF. SSIF has a common security level for channel 0 to channel 3.

■ 6.3.13 Slave Access Control Register 9 (SYS_SLVACCCTL9)

The following descriptions are fixed.

- **[RZ/G3S]**

[From]

6.3.13 Slave Access Control Register 9 (SYS_SLVACCCTL9)

This register sets the security levels for determining whether to enable or disable access to each set of registers in the SSIF, SRC, SPDIF and PDM.

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—
Initial Value	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
R/W	R	R	R	R	R	R	R	R	R	R	R	R	R	R	R	R

Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
	—	—	PDM_SL		SPDIF_SL		SRC_SL		SSIF3_SL		SSIF2_SL		SSIF1_SL		SSIF0_SL	
Initial Value	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
R/W	R	R	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W

Bit	Bit Name	Initial Value	R/W	Description
31 to 14	—	All 0	R	Reserved Whenever it is read, 0 is read. The written value will be ignored.
13, 12	PDM_SL[1:0]	00b	R/W	PDM slave access permission control Set the security level SL [1:0] for the slave PDM. PDM has a common security level for channel 0 to channel 2.
11, 10	SPDIF_SL [1:0]	00b	R/W	SPDIF slave access permission control Set the security level SL [1:0] for the slave SPDIF.
9, 8	SRC_SL[1:0]	00b	R/W	SRC slave access permission control Set the security level SL [1:0] for the slave SRC.
7, 6	SSIF3_SL [1:0]	00b	R/W	SSIF channel 3 slave access permission control Set the security level SL [1:0] for the slave SSIF channel 3.
5, 4	SSIF2_SL [1:0]	00b	R/W	SSIF channel 2 slave access permission control Set the security level SL [1:0] for the slave SSIF channel 2.
3, 2	SSIF1_SL [1:0]	00b	R/W	SSIF channel 1 slave access permission control Set the security level SL [1:0] for the slave SSIF channel 1.
1, 0	SSIF0_SL [1:0]	00b	R/W	SSIF channel 0 slave access permission control Set the security level SL [1:0] for the slave SSIF channel 0.

[To]

6.3.13 Slave Access Control Register 9 (SYS_SLVACCCTL9)

This register sets the security levels for determining whether to enable or disable access to each set of registers in the SSIF, SRC, SPDIF and PDM.

Delete

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—
Initial Value	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
R/W	R	R	R	R	R	R	R	R	R	R	R	R	R	R	R	R

Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
	—	—	PDM_SL		SPDIF_SL		—	—	SSIF3_SL		SSIF2_SL		SSIF1_SL		SSIF0_SL	
Initial Value	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
R/W	R	R	R/W	R/W	R/W	R/W	R	R	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W

Bit	Bit Name	Initial Value	R/W	Description
31 to 14	—	All 0	R	Reserved Whenever it is read, 0 is read. The written value will be ignored.
13, 12	PDM_SL[1:0]	00b	R/W	PDM slave access permission control Set the security level SL [1:0] for the slave PDM. PDM has a common security level for channel 0 to channel 2.
11, 10	SPDIF_SL [1:0]	00b	R/W	SPDIF slave access permission control Set the security level SL [1:0] for the slave SPDIF.
9, 8	—	00b	R	Reserved When read, the initial value is read. When writing, be sure to write the initial value. Operation is not guaranteed if a value other than the initial value is written.
7, 6	SSIF3_SL [1:0]	00b	R/W	SSIF channel 3 slave access permission control Set the security level SL [1:0] for the slave SSIF channel 3.
5, 4	SSIF2_SL [1:0]	00b	R/W	SSIF channel 2 slave access permission control Set the security level SL [1:0] for the slave SSIF channel 2.
3, 2	SSIF1_SL [1:0]	00b	R/W	SSIF channel 1 slave access permission control Set the security level SL [1:0] for the slave SSIF channel 1.
1, 0	SSIF0_SL [1:0]	00b	R/W	SSIF channel 0 slave access permission control Set the security level SL [1:0] for the slave SSIF channel 0.

Section 7. Clock Pulse Generator (CPG)

■ 7.2.3 Register configuration

The following descriptions are deleted.

- **[RZ/G2L,LC, RZ/V2L, RZ/G2UL, RZ/Five, RZ/G3S]**

Table 7.5 Register list

[From]

Clock Control Register SSI	CPG_CLKON_SSI	RW	H'0000 0000	H'570	32
Clock Control Register SRC	CPG_CLKON_SRC	RW	H'0000 0000	H'574	32
Clock Control Register USB	CPG_CLKON_USB	RW	H'0000 0000	H'578	32
Clock Control Register ETH	CPG_CLKON_ETH	RW	H'0000 0000	H'57C	32
Clock Control Register I2C	CPG_CLKON_I2C	RW	H'0000 0000	H'580	32
Clock Control Register SCIF	CPG_CLKON_SCIF	RW	H'0000 0000	H'584	32

[To]

Clock Control Register SSI	CPG_CLKON_SSI	RW	H'0000 0000	H'570	32
Clock Control Register SRC	CPG_CLKON_SRC	RW	H'0000 0000	H'574	32
Clock Control Register USB	CPG_CLKON_USB	RW	H'0000 0000	H'578	32
Clock Control Register ETH	CPG_CLKON_ETH	RW	H'0000 0000	H'57C	32
Clock Control Register I2C	CPG_CLKON_I2C	RW	H'0000 0000	H'580	32
Clock Control Register SCIF	CPG_CLKON_SCIF	RW	H'0000 0000	H'584	32

Delete

[From]

Clock Monitor Register SSI	CPG_CLKMON_SSI	R	H'0000 0000	H'6F0	32
Clock Monitor Register SRC	CPG_CLKMON_SRC	R	H'0000 0000	H'6F4	32
Clock Monitor Register USB	CPG_CLKMON_USB	R	H'0000 0000	H'6F8	32
Clock Monitor Register ETH	CPG_CLKMON_ETH	R	H'0000 0000	H'6FC	32
Clock Monitor Register I2C	CPG_CLKMON_I2C	R	H'0000 0000	H'700	32
Clock Monitor Register SCIF	CPG_CLKMON_SCIF	R	H'0000 0000	H'704	32

[To]

Clock Monitor Register SSI	CPG_CLKMON_SSI	R	H'0000 0000	H'6F0	32
Clock Monitor Register SRC	CPG_CLKMON_SRC	R	H'0000 0000	H'6F4	32
Clock Monitor Register USB	CPG_CLKMON_USB	R	H'0000 0000	H'6F8	32
Clock Monitor Register ETH	CPG_CLKMON_ETH	R	H'0000 0000	H'6FC	32
Clock Monitor Register I2C	CPG_CLKMON_I2C	R	H'0000 0000	H'700	32
Clock Monitor Register SCIF	CPG_CLKMON_SCIF	R	H'0000 0000	H'704	32

Delete

[From]

Reset Control Register SSIF	CPG_RST_SSIF	RW	H'0000 0000	H'870	32
Reset Control Register SRC	CPG_RST_SRC	RW	H'0000 0000	H'874	32
Reset Control Register USB	CPG_RST_USB	RW	H'0000 0000	H'878	32
Reset Control Register ETH	CPG_RST_ETH	RW	H'0000 0000	H'87C	32

[To]

Reset Control Register SSIF	CPG_RST_SSIF	RW	H'0000 0000	H'870	32
Reset Control Register SRC	CPG_RST_SRC	RW	H'0000 0000	H'874	32
Reset Control Register USB	CPG_RST_USB	RW	H'0000 0000	H'878	32
Reset Control Register ETH	CPG_RST_ETH	RW	H'0000 0000	H'87C	32

Delete

[From]

Reset Monitor Register SSIF	CPG_RSTMON_SSIF	R	H'0000 000F	H'9F0	32
Reset Monitor Register SRC	CPG_RSTMON_SRC	R	H'0000 0001	H'9F4	32
Reset Monitor Register USB	CPG_RSTMON_USB	R	H'0000 000F	H'9F8	32
Reset Monitor Register ETH	CPG_RSTMON_ETH	R	H'0000 0003	H'9FC	32
Reset Monitor Register I2C	CPG_RSTMON_I2C	R	H'0000 000F	H'A00	32
Reset Monitor Register SCIF	CPG_RSTMON_SCIF	R	H'0000 001F	H'A04	32
Reset Monitor Register SCI	CPG_RSTMON_SCI	R	H'0000 0003	H'A08	32
Reset Monitor Register IRDA	CPG_RSTMON_IRDA	R	H'0000 0001	H'A0C	32
Reset Monitor Register RSPI	CPG_RSTMON_RSPI	R	H'0000 0007	H'A10	32

[To]

Reset Monitor Register SSIF	CPG_RSTMON_SSIF	R	H'0000 000F	H'9F0	32
Reset Monitor Register SRC	CPG_RSTMON_SRC	R	H'0000 0001	H'9F4	32
Reset Monitor Register USB	CPG_RSTMON_USB	R	H'0000 000F	H'9F8	32
Reset Monitor Register ETH	CPG_RSTMON_ETH	R	H'0000 0003	H'9FC	32
Reset Monitor Register I2C	CPG_RSTMON_I2C	R	H'0000 000F	H'A00	32
Reset Monitor Register SCIF	CPG_RSTMON_SCIF	R	H'0000 001F	H'A04	32
Reset Monitor Register SCI	CPG_RSTMON_SCI	R	H'0000 0003	H'A08	32
Reset Monitor Register IRDA	CPG_RSTMON_IRDA	R	H'0000 0001	H'A0C	32
Reset Monitor Register RSPI	CPG_RSTMON_RSPI	R	H'0000 0007	H'A10	32

Delete

■ 7.2.4 Register Descriptions

The following descriptions are deleted.

- **[RZ/G2L,LC, RZ/V2L]**

  7.2.4.55 Clock Control Register SRC (CPG_CLKON_SRC)

- **[RZ/G2UL]**

  7.2.4.48 Clock Control Register SRC (CPG_CLKON_SRC)

- **[RZ/Five]**

  7.2.4.31 Clock Control Register SRC (CPG_CLKON_SRC)

- **[RZ/G3S]**

  7.2.4.43 Clock Control Register SRC (CPG_CLKON_SRC)

[From]

7.2.4.55 Clock Control Register SRC (CPG_CLKON_SRC)

This register is used to supply or stop clocks for individual modules.

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	CLK0_ONWEN
Initial Value	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
R/W	R	R	R	R	R	R	R	R	R	R	R	R	R	R	R	R0W1

Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	CLK0_ON
Initial Value	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
R/W	R	R	R	R	R	R	R	R	R	R	R	R	R	R	R	RW

Bit	Bit Name	Initial Value	R/W	Description
31 to 17	—	All 0	R	Reserved Whenever it is read, 0 is read. The written value will be ignored.
16	CLK0_ONWEN	0b	R0W1	Flag for enabling the writing to the CLK0_ON bit (bit 0) This bit is always read as 0. 0: Writing is disabled. 1: Writing is enabled.
15 to 1	—	All 0	R	Reserved Whenever it is read, 0 is read. The written value will be ignored.
0	CLK0_ON	0b	RW	The SRC_CLKP clock is supplied or stopped. 0: Clock is stopped. 1: Clock is supplied.

[To]

Delete

- **[RZ/G2L,LC, RZ/V2L]**

  7.2.4.95 Clock Monitor Register SRC (CPG_CLKMON_SRC)

- **[RZ/G2UL]**

  7.2.4.83 Clock Monitor Register SRC (CPG_CLKMON_SRC)

- **[RZ/Five]**

  7.2.4.61 Clock Monitor Register SRC (CPG_CLKMON_SRC)

- **[RZ/G3S]**

  7.2.4.93 Clock Monitor Register SRC (CPG_CLKMON_SRC)

[From]

7.2.4.95 Clock Monitor Register SRC (CPG_CLKMON_SRC)

This register is used to monitor the state of the clocks supplied to individual modules.

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—
Initial Value	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
R/W	R	R	R	R	R	R	R	R	R	R	R	R	R	R	R	R

Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	CLK0_MON
Initial Value	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
R/W	R	R	R	R	R	R	R	R	R	R	R	R	R	R	R	R

Bit	Bit Name	Initial Value	R/W	Description
31 to 1	—	All 0	R	Reserved Whenever it is read, 0 is read. The written value will be ignored.
0	CLK0_MON	0b	R	The state of the SRC_CLKP clock is monitored. 0: Clock is not supplied. 1: Clock is supplied.

[To]

Delete

- **[RZ/G2L,LC, RZ/V2L]**

  7.2.4.134 Reset Control Register SRC (CPG_RST_SRC)

- **[RZ/G2UL]**

  7.2.4.117 Reset Control Register SRC (CPG_RST_SRC)

- **[RZ/Five]**

  7.2.4.91 Reset Control Register SRC (CPG_RST_SRC)

- **[RZ/G3S]**

  7.2.4.142 Reset Control Register SRC (CPG_RST_SRC)

[From]

7.2.4.134 Reset Control Register SRC (CPG_RST_SRC)

This register is used to control the reset signals for individual modules.

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	UNIT0_RST WEN
Initial Value	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
R/W	R	R	R	R	R	R	R	R	R	R	R	R	R	R	R	R0W1

Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	UNIT0_RSTB
Initial Value	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
R/W	R	R	R	R	R	R	R	R	R	R	R	R	R	R	R	RW

Bit	Bit Name	Initial Value	R/W	Description
31 to 17	—	All 0	R	Reserved Whenever it is read, 0 is read. The written value will be ignored.
16	UNIT0_RST WEN	0b	R0W1	Flag for enabling the writing to the UNIT0_RSTB bit (bit 0) This bit is always read as 0. 0: Writing is disabled. 1: Writing is enabled.
15 to 1	—	All 0	R	Reserved Whenever it is read, 0 is read. The written value will be ignored.
0	UNIT0_RSTB	0b	RW	The SRC_RST reset terminal is controlled. 0: Reset signal is applied (reset state). 1: Reset signal is stopped (released from the reset state).

[To]

Delete

- **[RZ/G2L,LC, RZ/V2L]**

  7.2.4.173 Reset Monitor Register SRC (CPG_RSTMON_SRC)

- **[RZ/G2UL]**

  7.2.4.151 Reset Monitor Register SRC (CPG_RSTMON_SRC)

- **[RZ/Five]**

  7.2.4.121 Reset Monitor Register SRC (CPG_RSTMON_SRC)

- **[RZ/G3S]**

  7.2.4.191 Reset Monitor Register SRC (CPG_RSTMON_SRC)

[From]

7.2.4.173 Reset Monitor Register SRC (CPG_RSTMON_SRC)

This register is used to monitor the reset signals of individual modules.

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—
Initial Value	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
R/W	R	R	R	R	R	R	R	R	R	R	R	R	R	R	R	R

Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	RST0_MON
Initial Value	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	1
R/W	R	R	R	R	R	R	R	R	R	R	R	R	R	R	R	R

Bit	Bit Name	Initial Value	R/W	Description
31 to 1	—	All 0	R	Reserved Whenever it is read, 0 is read. The written value will be ignored.
0	RST0_MON	1b	R	The state of the SRC_RST reset signal is monitored. 0: Reset signal is not applied (released from the reset state). 1: Reset signal is applied (reset state).

[To]

Delete

- **[RZ/G2L,LC, RZ/V2L]**

  7.2.4.195 MSTOP Register MCPU1 (CPG_BUS_MCPU1_MSTOP)

- **[RZ/G2UL]**

  7.2.4.171 MSTOP Register MCPU1 (CPG_BUS_MCPU1_MSTOP)

- **[RZ/Five]**

  7.2.4.141 MSTOP Register MCPU1 (CPG_BUS_MCPU1_MSTOP)

- **[RZ/G3S]**

  7.2.4.227 MSTOP Register MCPU1 (CPG_BUS_MCPU1_MSTOP)

[From]

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
	MSTOP15_ON_WEN	MSTOP14_ON_WEN	MSTOP13_ON_WEN	MSTOP12_ON_WEN	MSTOP11_ON_WEN	MSTOP10_ON_WEN	MSTOP9_ON_WEN	MSTOP8_ON_WEN	MSTOP7_ON_WEN	MSTOP6_ON_WEN	MSTOP5_ON_WEN	MSTOP4_ON_WEN	MSTOP3_ON_WEN	MSTOP2_ON_WEN	MSTOP1_ON_WEN	MSTOP0_ON_WEN
Initial Value	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
R/W	R0W1	R0W1	R0W1	R0W1	R0W1	R0W1	R0W1	R0W1	R0W1	R0W1	R0W1	R0W1	R0W1	R0W1	R0W1	R0W1

Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
	MSTOP15_ON	MSTOP14_ON	MSTOP13_ON	MSTOP12_ON	MSTOP11_ON	MSTOP10_ON	MSTOP9_ON	MSTOP8_ON	MSTOP7_ON	MSTOP6_ON	MSTOP5_ON	MSTOP4_ON	MSTOP3_ON	MSTOP2_ON	MSTOP1_ON	MSTOP0_ON
Initial Value	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
R/W	RW	RW	RW	RW	RW	RW	RW	RW	RW	RW	RW	RW	RW	RW	RW	RW

[To]

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
	MSTOP15_ON_WEN	MSTOP14_ON_WEN	MSTOP13_ON_WEN	MSTOP12_ON_WEN	MSTOP11_ON_WEN	MSTOP10_ON_WEN	MSTOP9_ON_WEN	MSTOP8_ON_WEN	MSTOP7_ON_WEN	MSTOP6_ON_WEN	MSTOP5_ON_WEN	MSTOP4_ON_WEN	MSTOP3_ON_WEN	MSTOP2_ON_WEN	MSTOP1_ON_WEN	MSTOP0_ON_WEN
Initial Value	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
R/W	R0W1	R0W1	R0W1	R0W1	R0W1	R0W1	R0W1	R0W1	R0W1	R0W1	R0W1	R0W1	R0W1	R0W1	R0W1	R0W1

Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
	MSTOP15_ON	MSTOP14_ON	MSTOP13_ON	MSTOP12_ON	MSTOP11_ON	MSTOP10_ON	MSTOP9_ON	MSTOP8_ON	MSTOP7_ON	MSTOP6_ON	MSTOP5_ON	MSTOP4_ON	—	MSTOP2_ON	MSTOP1_ON	MSTOP0_ON
Initial Value	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
R/W	RW	RW	RW	RW	RW	RW	RW	RW	RW	RW	RW	RW	R	RW	RW	RW

[From]

Bit	Bit Name	Initial Value	R/W	Description
7	MSTOP7_ON	0b	RW	The state of BUS_MCPU_MSTOP5_MHPOEGC operation is indicated. 0: Normal operation 1: Module stop state (MSTP)
6	MSTOP6_ON	0b	RW	The state of BUS_MCPU_MSTOP4_MHPOEGB operation is indicated. 0: Normal operation 1: Module stop state (MSTP)
5	MSTOP5_ON	0b	RW	The state of BUS_MCPU_MSTOP3_MHPOEGA operation is indicated. 0: Normal operation 1: Module stop state (MSTP)
4	MSTOP4_ON	0b	RW	The state of BUS_MCPU_MSTOP2_MHGPT operation is indicated. 0: Normal operation 1: Module stop state (MSTP)
3	MSTOP3_ON	0b	RW	The state of BUS_MCPU_MSTOP1_MHSRC operation is indicated. 0: Normal operation 1: Module stop state (MSTP)
2	MSTOP2_ON	0b	RW	The state of BUS_MCPU_MSTOP0_MHMTU3A operation is indicated. 0: Normal operation 1: Module stop state (MSTP)
1	MSTOP1_ON	0b	RW	The state of BUS_MCPU_MSTOP_MHSPI operation is indicated. 0: Normal operation 1: Module stop state (MSTP)
0	MSTOP0_ON	0b	RW	The state of BUS_MCPU_MSTOP_MXSRAM_M operation is indicated. 0: Normal operation 1: Module stop state (MSTP)

[To]

Bit	Bit Name	Initial Value	R/W	Description
7	MSTOP7_ON	0b	RW	The state of BUS_MCPU_MSTOP5_MHPOEGC operation is indicated. 0: Normal operation 1: Module stop state (MSTP)
6	MSTOP6_ON	0b	RW	The state of BUS_MCPU_MSTOP4_MHPOEGB operation is indicated. 0: Normal operation 1: Module stop state (MSTP)
5	MSTOP5_ON	0b	RW	The state of BUS_MCPU_MSTOP3_MHPOEGA operation is indicated. 0: Normal operation 1: Module stop state (MSTP)
4	MSTOP4_ON	0b	RW	The state of BUS_MCPU_MSTOP2_MHGPT operation is indicated. 0: Normal operation 1: Module stop state (MSTP)
3	—	0b	R	Reserved When read, the initial value is read. When writing, be sure to write the initial value. Operation is not guaranteed if a value other than the initial value is written.
2	MSTOP2_ON	0b	RW	The state of BUS_MCPU_MSTOP0_MHMTU3A operation is indicated. 0: Normal operation 1: Module stop state (MSTP)
1	MSTOP1_ON	0b	RW	The state of BUS_MCPU_MSTOP_MHSPI operation is indicated. 0: Normal operation 1: Module stop state (MSTP)
0	MSTOP0_ON	0b	RW	The state of BUS_MCPU_MSTOP_MXSRAM_M operation is indicated. 0: Normal operation 1: Module stop state (MSTP)

- **[RZ/G2L,LC]**

  RZG2L_clock_list_r1.2.xlsx

- **[RZ/V2L]**

  RZV2L_clock_list_r1.2.xlsx

- **[RZ/G2UL]**

  RZG2UL_clock_list_r1.1.xlsx

- **[RZ/Five]**

  RZFIVE_clock_list_100_20220623_r01.xlsx

- **[RZ/G3S]**

  RZG3S_clock_list_r1.00_20230602.xlsx

[From]

SSI	SSI0_PCLK2	P0φ	SEL_PLL2_1	100/50/25/12.5/3.125	100	not supplied
	SSI0_PCLK_SFR	P0φ	SEL_PLL2_1	100/50/25/12.5/3.125	100	not supplied
	SSI1_PCLK2	P0φ	SEL_PLL2_1	100/50/25/12.5/3.125	100	not supplied
	SSI1_PCLK_SFR	P0φ	SEL_PLL2_1	100/50/25/12.5/3.125	100	not supplied
	SSI2_PCLK2	P0φ	SEL_PLL2_1	100/50/25/12.5/3.125	100	not supplied
	SSI2_PCLK_SFR	P0φ	SEL_PLL2_1	100/50/25/12.5/3.125	100	not supplied
	SSI3_PCLK2	P0φ	SEL_PLL2_1	100/50/25/12.5/3.125	100	not supplied
	SSI3_PCLK_SFR	P0φ	SEL_PLL2_1	100/50/25/12.5/3.125	100	not supplied
SRC	SRC_CLKP	P0φ	SEL_PLL2_1	100/50/25/12.5/3.125	100	not supplied
USB2.0	USB_U2H0_HCLK	P1φ	PLL3	200/100/50/25/6.25	200	not supplied
	USB_U2H1_HCLK	P1φ	PLL3	200/100/50/25/6.25	200	not supplied
	USB_U2P_EXR_CPUCLK	P1φ	PLL3	200/100/50/25/6.25	200	not supplied

[To]

SSI	SSI0_PCLK2	P0φ	SEL_PLL2_1	100/50/25/12.5/3.125	100	not supplied
	SSI0_PCLK_SFR	P0φ	SEL_PLL2_1	100/50/25/12.5/3.125	100	not supplied
	SSI1_PCLK2	P0φ	SEL_PLL2_1	100/50/25/12.5/3.125	100	not supplied
	SSI1_PCLK_SFR	P0φ	SEL_PLL2_1	100/50/25/12.5/3.125	100	not supplied
	SSI2_PCLK2	P0φ	SEL_PLL2_1	100/50/25/12.5/3.125	100	not supplied
	SSI2_PCLK_SFR	P0φ	SEL_PLL2_1	100/50/25/12.5/3.125	100	not supplied
	SSI3_PCLK2	P0φ	SEL_PLL2_1	100/50/25/12.5/3.125	100	not supplied
	SSI3_PCLK_SFR	P0φ	SEL_PLL2_1	100/50/25/12.5/3.125	100	not supplied
SRC	SRC_CLKP	P0φ	SEL_PLL2_1	100/50/25/12.5/3.125	100	not supplied
USB2.0	USB_U2H0_HCLK	P1φ	PLL3	200/100/50/25/6.25	200	not supplied
	USB_U2H1_HCLK	P1φ	PLL3	200/100/50/25/6.25	200	not supplied
	USB_U2P_EXR_CPUCLK	P1φ	PLL3	200/100/50/25/6.25	200	not supplied

Delete

Section 8. Interrupt Controller

■ 8.2 Interrupt Mapping

Table 8.2 Interrupt mapping

The following descriptions are fixed.

- **[RZ/G2L,LC, RZ/V2L, RZ/G2UL]**

[From]

Reserved	—	373	SPI 341	IRQ 341	—	
SRC	SRC_IDEI	374	SPI 342	IRQ 342	Edge	
	SRC_ODFI	375	SPI 343	IRQ 343	Edge	
	SRC_CEF	376	SPI 344	IRQ 344	Level	
	SRC_UDF	377	SPI 345	IRQ 345	Level	
	SRC_OVF	378	SPI 346	IRQ 346	Level	
ADC	INTAD	379	SPI 347	IRQ 347	Edge	

[To]

Reserved	—	373	SPI 341	IRQ 341	—	
Reserved	—	374	SPI 342	IRQ 342	—	
	—	375	SPI 343	IRQ 343	—	
	—	376	SPI 344	IRQ 344	—	
	—	377	SPI 345	IRQ 345	—	
	—	378	SPI 346	IRQ 346	—	
ADC	INTAD	379	SPI 347	IRQ 347	Edge	

- **[RZ/Five]**

[From]

Reserved	—	373	—	
SRC	SRC_IDEI	374	Edge	
	SRC_ODFI	375	Edge	
	SRC_CEF	376	Level	
	SRC_UDF	377	Level	
	SRC_OVF	378	Level	
ADC	INTAD	379	Edge	

[To]

Reserved	—	373	—	
Reserved	—	374	—	
	—	375	—	
	—	376	—	
	—	377	—	
	—	378	—	
ADC	INTAD	379		

■ [RZ/G3S]

[From]

	INT_ssif_dma_tx_2	280	SPI 248	IRQ 248	IRQ 248	Edge	
SSIF (ch3)	INT_ssif_int_req_3	281	SPI 249	IRQ 249	IRQ 249	Level	
	INT_ssif_dma_rx_3	282	SPI 250	IRQ 250	IRQ 250	Edge	
	INT_ssif_dma_tx_3	283	SPI 251	IRQ 251	IRQ 251	Edge	
SRC	SRC_IDEI	284	SPI 252	IRQ 252	IRQ 252	Edge	
	SRC_ODFI	285	SPI 253	IRQ 253	IRQ 253	Edge	
	SRC_CEF	286	SPI 254	IRQ 254	IRQ 254	Level	
	SRC_UDF	287	SPI 255	IRQ 255	IRQ 255	Level	
	SRC_OVF	288	SPI 256	IRQ 256	IRQ 256	Level	
I2C (ch0)	INTRIICTEI0	289	SPI 257	IRQ 257	IRQ 257	Level	
	INTRIICNAKI0	290	SPI 258	IRQ 258	IRQ 258	Level	

[To]

	INT_ssif_dma_tx_2	280	SPI 248	IRQ 248	IRQ 248	Edge	
SSIF (ch3)	INT_ssif_int_req_3	281	SPI 249	IRQ 249	IRQ 249	Level	
	INT_ssif_dma_rx_3	282	SPI 250	IRQ 250	IRQ 250	Edge	
	INT_ssif_dma_tx_3	283	SPI 251	IRQ 251	IRQ 251	Edge	
Reserved	—	284	SPI 252	IRQ 252	IRQ 252	—	
	—	285	SPI 253	IRQ 253	IRQ 253	—	
	—	286	SPI 254	IRQ 254	IRQ 254	—	
	—	287	SPI 255	IRQ 255	IRQ 255	—	
	—	288	SPI 256	IRQ 256	IRQ 256	—	
I2C (ch0)	INTRIICTEI0	289	SPI 257	IRQ 257	IRQ 257	Level	
	INTRIICNAKI0	290	SPI 258	IRQ 258	IRQ 258	Level	

Section 14. Direct Memory Access Controller

■ 14.5.2 DMA Transfer Requests

The following descriptions are deleted.

- **[RZ/G2L,LC, RZ/V2L, RZ/G2UL, RZ/Five, RZ/G3S]**

Table 14.3 On-Chip Module Requests

[From]

SSIF ch3	INT_ssif_dma_rx_3 (receive data full)	SSIF RDR_3	Arbitrary	10011000	10	0	010	0	1	0	0
	INT_ssif_dma_tx_3 (transmit data empty)	Arbitrary	SSIF TDR_3	10011000	01	0	010	0	1	0	1
SRC	SRC_IDEI (input data FIFO empty)	Arbitrary	SRCID	10011001	10	0	010	0	1	0	1
	SRC_ODFI (output data FIFO full)	SRCOD	Arbitrary	10011001	01	0	010	0	1	0	0
I2C ch0	INTRIIC_RI0 (receive data full)	RIIC0DRR	Arbitrary	10011010	10	0	010	0	1	0	0
	INTRIIC_TI0	Arbitrary	RIIC0DRT	10011010	01	0	010	0	1	0	1

[To]

SSIF ch3	INT_ssif_dma_rx_3 (receive data full)	SSIF RDR_3	Arbitrary	10011000	10	0	010	0	1	0	0
	INT_ssif_dma_tx_3 (transmit data empty)	Arbitrary	SSIF TDR_3	10011000	01	0	010	0	1	0	1
SRC	SRC_IDEI (input data FIFO empty)	Arbitrary	SRCID	10011001	10	0	010	0	1	0	1
	SRC_ODFI (output data FIFO full)	SRCOD	Arbitrary	10011001	01	0	010	0	1	0	0
I2C ch0	INTRIIC_RI0 (receive data full)	RIIC0DRR	Arbitrary	10011010	10	0	010	0	1	0	0
	INTRIIC_TI0	Arbitrary	RIIC0DRT	10011010	01	0	010	0	1	0	1

Delete

Section N. Sampling Rate Converter (SRC)

N=29 :[RZ/G2L,LC, RZ/V2L, RZ/G2UL, RZ/Five, RZ/G3S]

N=36 :[RZ/G3S]

[From]

All contents are included.

[To]

All contents are deleted

Section N. Low Power Mode

N=42 :[RZ/G2L,LC, RZ/V2L, RZ/G2UL, RZ/Five, RZ/G3S]

N=41 :[RZ/G3S]

■ **[RZ/G2L,LC, RZ/V2L, RZ/G2UL, RZ/Five]**

● **42.2.2.1 Setting of Clock control and MSTOP register**

Table 42.3 Registers for Module Standby Mode

■ **[RZ/G3S]**

● **41.2.2.1 Setting of Clock control and MSTOP register**

Table 41.4 Registers for Module Standby Mode

[From]

SSI ch0	SSI	[1:0]	MCPU1	[10]
SSI ch1		[3:2]		[11]
SSI ch2		[5:4]		[12]
SSI ch3		[7:6]		[13]
SRC	SRC	[0]	MCPU1	[3]
USB2.0 ch0	USB	[0], [2]	PERI_COM	[6:5]

[To]

SSI ch0	SSI	[1:0]	MCPU1	[10]
SSI ch1		[3:2]		[11]
SSI ch2		[5:4]		[12]
SSI ch3		[7:6]		[13]
SRC	SRC	[0]	MCPU1	[3]
USB2.0 ch0	USB	[0], [2]	PERI_COM	[6:5]

Delete