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- Document Name VR4181A Preliminary User's Manual (Draft) Rev. 0.13
- Document Number SUD-T-5239-1
- Document Date August 3rd, 2001
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NEC

User's Manual (Preliminary)

Revision 0.13

VR4181A™

64-/32-bit Microprocessor

μPD30181A

This document was created at the product planning stage of silicon and is subject to change without notice

NEC S. E. D. Microcomputer Engineering Dept.
Document No. SUD-T-5239-1, CP(K)
Date Published 8/3/01

CHAPTER 1 Introduction

This chapter describes the outline of the VR4181A (μPD30181A), which is a 64-bit microprocessor.

1.1 Features

The VR4181A, which is a high-performance 64-bit microprocessor employing the RISC (reduced instruction set computer) architecture developed by MIPS™, is one of the VR-Series microprocessor products manufactured by NEC.

The VR4181A contains the VR4120™ CPU core of ultra-low-power consumption with cache memory, high-speed product-sum operation unit, and memory management unit. It also has interface units for peripheral circuits such as LCD controller, Compact-Flash controller, USB (Host / Client) controller, DMA controller, SDRAM controller, Pulse Width Modulation controller, AC97/I2S Audio Codec interface, RS232C serial interface, IrDA interface, I2C Serial interface, Keyboard interface, Touch-panel interface, Real-time clock, A/D converter and D/A converter required for the battery-driven portable information equipment, Stattionary compact information equipment, Car navigation system, and Compact embedded equipment. The features of the VR4181A are described below.

- Employ 64-bit RISC VR4120 CPU core
  - Pipeline clock: 131.1 MHz
  - 64 bit data handling internally
  - operation in 64/32-bit mode is available
- Optimized pipeline
- On-chip instruction and data caches with 8 KB each in size
- Write-back cache for reducing store operation that use the system bus
- 32-bit physical address space and 40-bit virtual address space
- Virtual address management structure by 32 double-entry TLB
- Instruction set: MIPS III (with the FPU, LL and SC instructions left out) and MIPS16
- Supports MACC and DMACC instructions for executing a multiply-and-accumulate operation of 32-bit data x 32-bit data + 64-bit data within one clock cycle

- Effective power management features, which include four operating modes, Full-speed, Standby, Suspend and Hibernate mode
- Low power comsumption design by dynamic clock control

- Employ high performance internal system bus (T-bus)
- System Bus interface supporting Ordinary ROM / Page ROM / flash memory / SRAM / ISA device, IDE(ATA) device, SyncFlash ™
- DRAM controller supporting 64, 128, 256M bit SDRAM
- DMA controller (4ch) supporting chain mode
- UMA based LCD (STN / TFT) controller
- Compact-Flash interface (2slot) compatible with ExCA
- USB(HOST) comformed to Universal Serial Bus Specification Rev 1.1 and OHCI Rev1.0 (1ch)
- USB(Client) comformed to Universal Serial Bus Specification Rev 1.1 (1ch)
- AC97/I2S Stereo Audio interface (1ch, respectively)
- Clocked Serial interface (CSI) (1ch)
- Asynchronous Serial interfaces (3ch) compatible with NS16550 (UART)
- IrDA(SIR) interface (1ch)
- I2C interface (2ch)
- Pulse Width Modulation (3ch)
- Keyboard Scan interface (8 x 12 key matrix)
- X-Y auto-scan touch panel interface
- A/D and D/A converters
- Watchdog Timer unit
- RTC unit including 3-channel timers and counters

- On-chip PLL and clock generator
- Supply voltage: 2.5 V for CPU core, 3.3 V for I/O
- Employs 0.25 μm process
- Package: 240-pin FPBGA

1.2 Ordering Information

Part number	Package	Maximum frequency
μPD30181AYF1-131-GA3	240-pin Plastic BGA (Fine-pitch) (16mm X 16mm)	131.1 MHz

1.3 64-Bit Architecture

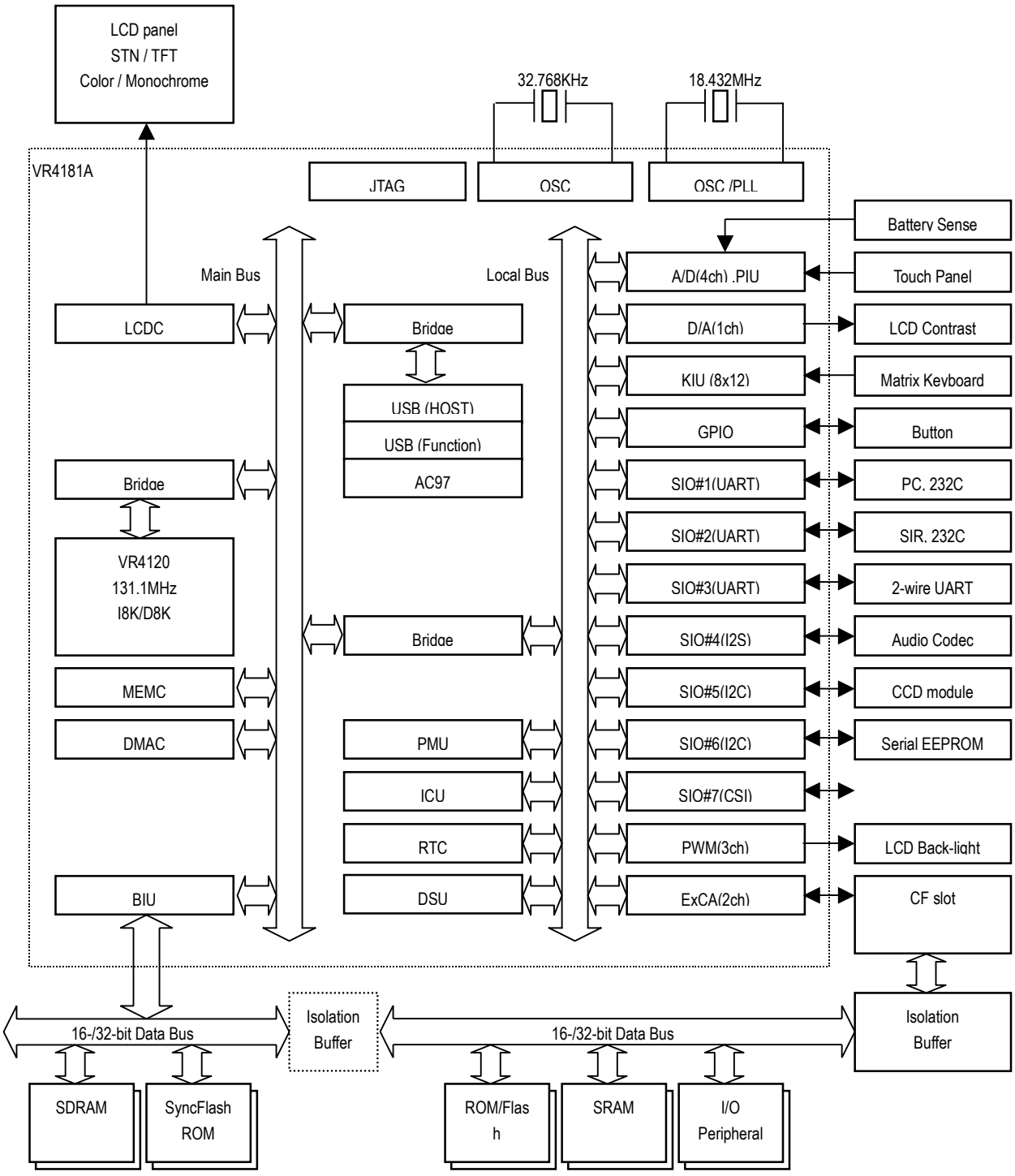
The VR4181A is a high-performance 64-bit microprocessor. There're 64 bit register set and internal data bus, and therefore VR4181A can handle data in 64 bit.

Then, it can run 32-bit applications even if it operates as a 64-bit microprocessor.

1.4 VR4181A Key Features

The VR4181A consists of the VR4120 CPU core and 24 peripheral units, and has enough interface to connect to controllers directly. Figure 1-1 describes an internal block diagram of the VR4181A processor and example of connection to external blocks.

Figure 1-1 Internal Block Diagram



1.4.1 CPU core

The VR4181A integrates an NEC VR4120 CPU core supporting both the MIPS III and MIPS16 instruction sets, and supports the following pipeline clock (AClock) and internal system bus clock (TClock) frequencies. The AClock is set by attaching pull-up or pull-down resistors to the CLKSEL(2:0) pins, then Tclock is set by attaching pull-up or pull-down resistors to the DIVMODE(1:0) pins. TClock can be changed by software after boot-up.

Table 1-1 Supported AClock and TClock Frequencies

AClock frequency	TClock frequency
131.1 MHz	65.5 / 43.7 MHz
118.0 MHz	59.0 / 39.0 MHz
98.3 MHz	49.1 / 32.8 MHz
90.7 MHz	45.3 / 30.3 MHz
84.1 MHz	42.0 / 28.0 MHz
78.5 MHz	39.2 / 26.2 MHz
73.7 MHz	36.8 / 24.6 MHz

The VR4120 core of the VR4181A includes 8 KB of instruction cache and 8 KB of data cache. The VR4120 core also supports four power management modes: Fullspeed mode, Standby mode, Suspend mode, and Hibernate mode.

1.4.2 Bus interface

The VR4181A incorporates single bus architecture. All external memory and I/O devices are connected to the same 25-bit address bus and either 16-bit or 32-bit data bus. These external address and data bus are together called the system bus. When the external bus connected to SDRAM or SyncFlash ™ operates at a very high speed, the external data bus must be isolated from other low speed devices. The VR4181A can controls the isolation buffer using SYSEN# and SYSDIR pin.

Both internal and external bus cycle will be generated based on four clocks as follows.

Table 1-2 Relationship between bus cycle and clocks

Bus Cycle	Clock	Maximum frequency
SDRAM Access Cycle	TClock	65.5 MHz
External System Bus Cycle	LClock	65.5 MHz
Internal System Bus Cycle	TClock	65.5 MHz
Internal ISA Bus Cycle	PClock	65.5 MHz
Internal PCI Bus Cycle	PCIClock	32.8 MHz

TClock is utilized at the internal system bus, and generated based on Pipeline Clock (AClock) according to the value set by attaching pull-up or pull-down resistors to the DIVMODE(1:0) pins at the rising edge of RTCRST# pin.

LClock is utilized at the external system bus, and generated based on TClock according to the internal divider (1/1, 1/2, 1/3 ,1/4) set by internal register. PClock is utilized at the internal ISA bus, and generated based on TClock according to the internal divider (1/1, 1/2, 1/4, 1/8) set by internal register. PCIClock is utilized at the internal PCI bus, and generated based on AClock according to the internal divider (1/3, 1/4) set by internal register.

VR4181A supports the following types of devices connected to the system bus.

Table 1-3 Devices Supported by System Bus

Device	Data Width
ROM, Flash Memory, SRAM	8 / 16 / 32 bits
External I/O device	8 / 16 / 32 bits
SDRAM	16 bits
Sync Flash ™	16 bits
Compact Flash Card	8 / 16 bits
ISA device	8 / 16 bits

1.4.3 ROM Chip Select / Programmable Chip Select

VR4181A provides one ROM chip select ROMCS# pin and five programmable chip select PCS(4:0)# pin. Each chip select has dedicated timing parameter based on LClock. The programmable chip select PCS(4:0)# pin can be used to connect to ROM.

1.4.4 Memory interface

VR4181A provides control for ROM / Flash memory, SRAM, Sync Flash ™, and SDRAM. VR4181A supports 64M / 128M / 256M bit of ROM / Flash memory and SRAM with both single mode and page mode. Up to six banks of them can be supported by using both ROMCS# pin and PCD(4:0)# pin at 8 / 16 / 32 bit width, though 256M bit ROM / Flash memory is not supported at 32 bit width. ROMCS# pin and PCS(4:0)# pin not connected to ROM / Flash memory and SRAM can be used to connect to external I/O device as programmable chip select.

VR4181A supports 64M / 128M / 256M bit (4M X 16 bit / 8M X 16 bit / 16M X 16 bit) of SDRAM with two banks at 66MHz, and connects to them by SDCS(1:0)# pin.

VR4181A supports 64M / 128M / 256M bit (4M X 16 bit / 8M X 16 bit / 16M X 16 bit) of Sync Flash ™ with two banks at 66MHz, and connects to them by SDCS(3:2)# pin.

1.4.5 DMA controller (DCU)

The VR4181A provides 4ch DMA controller. The main features are described below.

- Support four channel for DMA transaction
- Support DRAM (SDRAM) space, Boot ROM space (ROM, Sync Flash™), External I/O space, and Internal ISA space as the source address
- Support DRAM (SDRAM) space, External I/O space, and Internal ISA space as the destination address
- Support 1, 2, 4, 32bytes (8 word) as DMA transaction unit for each channel, individually
- Support Chain mode, which enables automatic DMA transaction from 2nd transaction
- Support DMA transaction to external I/O device by Hardware handshake using DRQ(1:0)# pin and DAK(1:0)# pin
- Support DMA transaction to SIU (16550 UART ch0,1,2), I2SU, AIU integrated into VR4181A by Hardware handshake
- Support DMA transaction termination report to external I/O device by using TC(1:0)# pin
- Support DMA transaction termination report to CPU by interrupt

1.4.6 Interrupt controller (ICU)

VR4181A provides an interrupt controller which combines all interrupt request sources into one of the VR4120 core interrupt inputs - NMI and Int(4:0). The interrupt controller supports enable of Interrupt request to CPU, assignment of interrupt request, and indication of interrupt request status.

1.4.7 LCD controller (LCU)

VR4181A provides an LCD controller using Unified Memory Architecture (UMA) based in which the frame buffer is part of system DRAM. The LCD controller supports monochrome STN LCD panels having 1-bit, 2-bit, and 4-bit data bus interfaces and color STN LCD panels having 8-bit data bus interface, then, in addition, color TFT LCD panels having 12-bit and 16-bit bus interfaces.

In monochrome mode with STN panel , the LCD controller supports 1-bpp mode (mono), 2-bpp mode (4 gray levels) and 4-bpp mode (16 gray levels). In color mode with STN panel, it supports 4-bpp mode (16 colors) and 8-bpp mode (256 colors), then in color mode with TFT panel, it supports 12-bpp mode (4,096 colors) and 16-bpp mode (65,536 colors).

The LCD controller includes a 256-entry x 18-bit color pallet. In 4-bpp and 8-bpp modes with STN panel, the pallet can be used, then, in 8-bpp modes, the pallet is used to select one of 256 colors out of possible 262,144.

The LCD controller can be configured to support the following LCD panel horizontal / vertical resolutions typically.

Table 1-4 TFT interface

16-bit TFT		12-bit TFT	
FPD(15:11)	R	FPD(11:8)	R
FPD(10:5)	G	FPD(7:4)	G
FPD(4:0)	B	FPD(3:0)	B

The LCD controller will have the capability of up to logical 1,024 pixel x 1,024 pixel resolutions with a pixel order, but the resolution will have to be decided to consider not only the specification (panel size, color depth, refressh rate) of LCD panel, but also the bus traffic based on the Unified Memory Architecture (UMA) to get the necessary system performance.

The LCD controller also provides power on and power down sequence control for the LCD panel via the VPLCD and VPBIAS pins. Power sequencing is provided to prevent latch-up damage to the panel.

1.4.8 Compact-Flash interface (ECU)

VR4181A provides an ExCA-compatible bus controller supporting two CompactFlash slots. The main features are described below.

- Support two Compact Flash slots
- Support the register sets [Note] being compatiblle with ExCA™ (Exchangeable Card Architecture) as defact standard.
- Map the address space of Compact Flash Card to the external ISA I/O space and memory space using window.
- Support Hot insertion (HOT plug-in) of Compact Flash card, and the control function of connection / dis-connection to the internal I/O interface and external isolation buffer.
- Suport to report the interrupt of Compact Flash card to VR4181A Interrupt controller (ICU).
- Support to occur the interrupt to detect the insertion of Compact Flash card.
- Support IDE(ATA) interface using the control signals of slot 0.

1.4.9 USB (HOST / Client) controller (USBHU / USBFU)

VR4181A provides USB(HOST) controller (1ch) complying Universal Serial Bus Specification Rev 1.1 and OHCI Rev1.0, and USB(Client) controller (1ch) complying Universal Serial Bus Specification Rev 1.1.

1.4.10 AC97 / I2S Stereo Audio Codec interface (AC97U / I2SU)

VR4181A provides both AC97 CODEC interface which can support the CODEC having SRC/ Filter inside, and I2S interface supporting both master and slave mode.

AC97 interface can be connected to the Codec complying AC97 Rev2.0. AC97 interface (AC97U) supports Variable Sampling Rate (VSR) feature, and therefore can converts the sampling frequency without sample rate convertor (SRC).

AC97 interface controller (AC97U) integrates Bus master function, and therefore can executes DMA transaction to DRAM not using integrated general DMA controller.

I2S Codec interface (I2SU) can be connected to Codec device complying not only I2S format but also other serial stereo data format provided by several company. I2SU can be executed DMA transaction to DRAM by using general DMA controller.

1.4.11 Clocked Serial interface (CSI)

VR4181A provides a clocked serial interface (CSI) multiplexed with Keyboard interface. This interface supports both master and slave mode operation. The clocked serial interface supports three wires transfer using SI, SO, and SCK signals, and supports to multislave function using FRM pin. The interface is multiplexed with a part of Keyboard iinterface.

1.4.12 16550 Serial interface (SIU)

VR4181A provides three 16550 UART for implementing RS-232-C type serial interface. This interface can be configured in one of the following modes:

- Simple 2-wire serial interface using TxD and RxD
- 4-wire serial interface using TxD, RxD, RTS# and CTS#
- Full RS-232-C compatible interface using TxD, RxD, RTS#, CTS#, DTR#, DCD# and DSR#
- SIR-type IrDA interface using IRDIN and IRDOUT

When I2C is used, ch1 can not be utilized. When either AC97 or I2S is used, ch2 with Full RS-232-C compatible interface can not be utilized. When ch0,1 is not used, this interface can be utilized as GPIO interface.

1.4.13 I2C Serial interface (I2CU)

VR4181A provides I2C Serial interface (I2CU) having two channel. I2CU supports both normal mode (max: 100kbit / s) and high speed mode (max: 400kbit / s).

Ch0 interface is multiplexed with a part of Keyboard interface. When 16550 Serial interface (ch1) is used, ch1 interface can not be utilized. When this interface is not used, this interface can be utilized as GPIO interface.

1.4.14 Baud-rate and Configuration for Serial interface

VR4181A provides the Baud-rate and the Configuration for Serial interface as follows.

Table 1-5 Baud-rate for Serial interface

Serial interface	Baud-rate
USB(HOST)	1.5Mbps, 12Mbps
USB(Peripheral)	12Mbps
16550 UART	1Mbps (MAX)
IrDA	115.2Kbps (MAX)
CSI	4.6Mbps (MAX)
I2C	400Kbps (MAX)
I2S	4Mbps (MAX)

Table 1-6 Configuration for Serial interface

1) 7-wire; two channels [ch0, ch2]), I2C (two channels)
2) 7-wire; two channels [ch0, ch2]), 2-wire [ch1], I2C (one channel)
3) 7-wire; one channel [ch0], 2-wire / IrDA (SIR) [ch2], AC97 / I2S, I2C (two channels)
4) 7-wire; one channel [ch0], 2-wire [ch1], 2-wire / IrDA (SIR) [ch2], AC97 / I2S, I2C (one channel)
5) 4-wire; two channels [ch0, ch1]), 2-wire / IrDA (SIR) [ch2], AC97 / I2S, I2C (one channel)

1.4.15 Pulse Width Modulation (PWMU)

VR4181A provides three Pulse Width Modulation Wave Generator. Ch0 is compatible with LEU on VR4181, and generates pulse according to the register value based on Real time clock (32.768KHz), and can be utilized for LED turn-on/-off operation. Ch1 generates pulse according to the register value based on either Real time clock (32.768KHz) or system clock (18.432MHz). Ch2 generates pulse according to the register value based on either Real time clock (32.768KHz) or MasterOut which is 1/4 * TClock. When 8x12 full Keyboard interface is used, this interface can not be utilized. When this interface is not used, this interface can be utilized as GPIO interface.

1.4.16 Keyboard interface (KIU)

VR4181A provides support for an 8 x 12 key matrix as maximum. 4 x 4 key matrix has dedicated interface, but other interface is multiplexed with Compact Flash Card interface, CSI interface, I2C interface, and Pulse Modulation interface. When some of those interface is used, keyboard interface can be utilized by using the remainder of them. When this interface is not used, this interface can be utilized as GPIO interface.

1.4.17 Analog input / output (AIU, A/D, D/A converter)

VR4181A provides an 8ch 10-bit A/D converter for analog input and a 1ch 10-bit D/A converter for analog output.

1.4.18 Touch panel interface and analog input (A/D converter)

VR4181A provides touch panel interface which can be possible to connect to touch panel directly. The touch panel interface uses the integrated A/D converter to detect pen-touch and its location.

1.4.19 Real-time clock (RTC)

VR4181A provides a real-time clock (RTC), which allows time keeping based on the 32.768 kHz clock as a source. RTC provides two kind of timers, and three timers totally as follows. The ElapsedTime Timer below operates at any of power management mode as long as 3.3V power at VR4181A is supplied.

- RTCLong timer

  This is a 24-bit programmable counter that counts down using 32.768 kHz frequency. Cycle interrupts occur for up to 512 seconds. VR4181A RTC unit includes two RTCLong timers.

- ElapsedTime timer

  This is a 48-bit up counter that counts up using 32.768 kHz frequency. It counts up to 272 years before returning to zero. It includes 48-bit comparator (ECMPHREG, ECMPLREG, and ECMPMREG) and 48-bit alarm time register (ETIMELREG, ETIMEMREG, and ETIMEHREG) to enable interrupts to occur at specified times.

1.4.20 Watch Dog Timer (WDT)

VR4181A provides a watch dog timer which can be set from one second to fifteen seconds every second. Any un-control operation caused by software can be detected by this watch dog timer, and the destroy of data into memory can be minimized to reset it by this watch dog timer.

1.4.21 Debug interface (DEBUGU)

VR4181A provides a debug interface complying with NEC N-wire without the trace function.

1.4.22 General-purpose I/O (GPU)

VR4181A provides total 64 bits of general purpose I/O (GPIO; GPO(63:62) pin and GPIO(61:0) pin). GPO(63:54) pins are allocated to A(24:15) by default, when 01 is set to BMODE(1:0) pin at the rising edge of RTCRST#. Other GPIO pins are allocated to general purpose inputs by default. GPO(63:62) and GPIO(61:0) pin can be configured as one of the following:

- General-purpose input
- General-purpose output
- Interrupt request / Wake-up input

Table 1-7 GPIO(63:0) Pin Functions

Pin designation	Alternate function	Pin designation	Alternate function
GPIO0	KSCAN0	GPIO32	CF0_CE2#
GPIO1	KSCAN1	GPIO33	CF_WAIT#
GPIO2	KSCAN2	GPIO34	CF0_IOIS16#
GPIO3	KSCAN3	GPIO35	CF0_CD1#
GPIO4	KPORT0	GPIO36	CF0_CD2#
GPIO5	KPORT1	GPIO37	CF1_VCCEN#, KSCAN4
GPIO6	KPORT2	GPIO38	CF1_EN#, KPORT5
GPIO7	KPORT3	GPIO39	CF1_DIR#, KPORT4
GPIO8	PWM0, KSCAN7	GPIO40	FPD4
GPIO9	PWM1, KSCAN6	GPIO41	FPD5
GPIO10	PWM2, KSCAN5	GPIO42	FPD6
GPIO11	SDA0, KPORT6	GPIO43	FPD7
GPIO12	SCL0, KPORT7	GPIO44	FPD8
GPIO13	TXD1, SDA1	GPIO45	FPD9
GPIO14	RXD1, SCL1	GPIO46	FPD10, CF1_CD1#
GPIO15	DSR0# / CTS1#	GPIO47	FPD11, CF1_CD2#
GPIO16	DCD0#	GPIO48	FPD12, CF1_CE1#
GPIO17	DTR0# / RTS1# / CLKSEL0	GPIO49	FPD13, CF1_CE2#
GPIO18	CTS0#	GPIO50	FPD14, CF1_STSCHG#
GPIO19	RTS0# / CLKSEL1	GPIO51	FPD15, CF1_READY
GPIO20	FRM, KSCAN8	GPIO52	TC0#
GPIO21	SO, KSCAN9	GPIO53	TC1#
GPIO22	SI, KSCAN10	GPIO54	A15
GPIO23	SCK, KSCAN11	GPIO55	A16
GPIO24	CF0_VCCEN#	GPIO56	A17
GPIO25	CF_REG#	GPIO57	A18
GPIO26	CF0_EN#	GPIO58	A19
GPIO27	CF0_DIR#	GPIO59	A20
GPIO28	CF0_RESET	GPIO60	A21
GPIO29	CF0_READY	GPIO61	A22
GPIO30	CF0_STSCHG#	GPO62 Note	VPLCD
GPIO31	CF0_CE1#	GPO63 Note	VPBIAS

Note This signal supports output only.

1.4.23 Power management modes / Wake-up events

VR4181A provides four power management modes: Fullspeed, Standby, Suspend, and Hibernate. Of these modes, Hibernate is the lowest power mode and results in the powering off of all system components including the 2.5 V logic in VR4181A. VR4181A 3.3 V logic, which includes RTC, PMU, PWMU (ch0,1) and non-volatile registers, remain powered during the Hibernate mode. When the data into SDRAM must be preserved during Hibernate mode, 3.3V power can be supplied to SDRAM. Here is the Wake-up events between Hibernate / Suspend / Standby mode and Fullspeed mode.

- Full Speed -> Standby : Standby instruction
- Standby -> Full Speed : Whole interrupts
- Full Speed -> Suspend : Suspend instruction
- Suspend -> Full Speed : RSTSW# inactive,
  POWER active, GPIO(61:0), CF0_READY,
  SIU0,1,2 16550 Serial (Modem Status), NMI#,
  RTC ElapsedTimer (Alarm), RTCLong1, RTCLong2,
  PIU PENCHGINTR (Panel Touch), KIU KEYDOWN (Key Touch),
  PWMU(CH0) Auto Stop
- Full Speed -> Hibernate : Hibernate instruction
- Hibernate -> Full Speed : RTCRST# inactive, POWER active, GPIO(61:0), RTC ElapsedTimer (Alarm)

Here is the relationship between power management modes and each clock.

Table 1-8 Relationship between power management modes and each clock

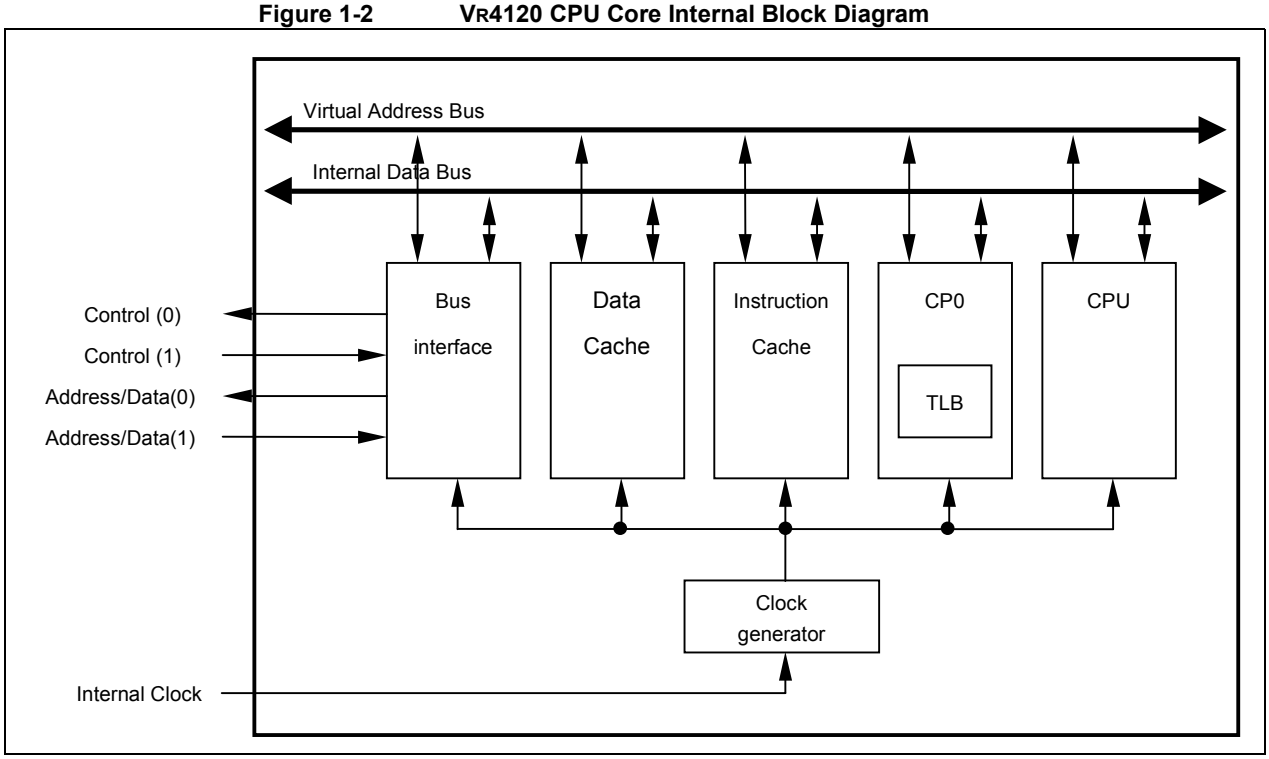
Function	Power management modes			
	Full Speed	Standby	Suspend	Hibernate
CPU Pipeline Clock (AClock)	Active	In-active	In-active	In-active
Internal System Bus Clock (TClock)	Active	Active	In-active	In-active
Internal PCI Bus Clock (PCIClock)	Active	Active	In-active	In-active
Internal ISA Bus Clock (PClock)	Active	Active	In-active	In-active
External Bus Clock (LClock)	Active	Active	In-active	In-active
Interrupt Control Clock (MasterOut)	Active	Active	Active	In-active
PLL	Active	Active	Active	In-active
18.432MHz Xtal	Active	Active	Active	In-active
32.768KHz Xtal	Active	Active	Active	Active

1.5 VR4120 CPU Core

Figure 1-2 shows the internal block diagram of the VR4120 CPU core.

In addition to the conventional high-performance integer operation units, this CPU core has the full-associative format translation lookaside buffer (TLB), which has 32 entries that provide mapping to 2-page pairs (odd and even) for one entry. Moreover, it also includes instruction cache, data cache, and bus interface.

Figure 1-2 VR4120 CPU Core Internal Block Diagram



1.5.1 Internal block configuration

(1) CPU

CPU is a block that performs integer calculations. This block includes a 64-bit integer data path, and product-sum operator.

(2) Coprocessor 0 (CP0)

CP0 incorporates a memory management unit (MMU) and exception handling function. The MMU checks whether there is an access between different memory segments (user, supervisor, and kernel) by executing address conversion. The translation lookaside buffer (TLB) converts virtual addresses to physical addresses.

(3) Instruction cache

The instruction cache employs direct mapping, virtual index, and physical tag formats. Its capacity is 8KB.

(4) Data cache

The data cache employs direct mapping, virtual index, physical tag, and writeback. Its capacity is 8KB.

(5) Bus interface

The bus interface controls data transmission/reception between the VR4120 CPU core and the BCU, which is one of the peripheral units. The bus interface consists of two 32-bit multiplexed address/data buses (one for input, and the other for output), clock signals, interrupt request signals, and various other control signals.

(6) Clock generator

The following clock inputs are oscillated and supplied to internal units.

- 32.768 kHz clock for RTC unit. Oscillating a 32.768 kHz crystal resonator input via an internal oscillator to supply to the RTC unit.
- 18.432 MHz clock for serial interface and the VR4181A's reference operating clock. Oscillating an 18.432 MHz crystal resonator input via an internal oscillator, and then multiplying it by a phase-locked loop (PLL) to generate a pipeline clock (AClock). The internal bus clock (TClock) is generated from AClock and supplied to peripheral units.

1.5.2 CPU registers

The VR4120 CPU core has the following registers:

- General-purpose registers (GPR): 64 bits × 32

In addition, the processor provides the following special registers:

- PC: Program counter (64 bit)
- HI register: Contains the integer multiply and divide higher doubleword result (64 bits)
- LO register: Contains the integer multiply and divide lower doubleword result (64 bits)

Two of the general-purpose registers are assigned the following functions:

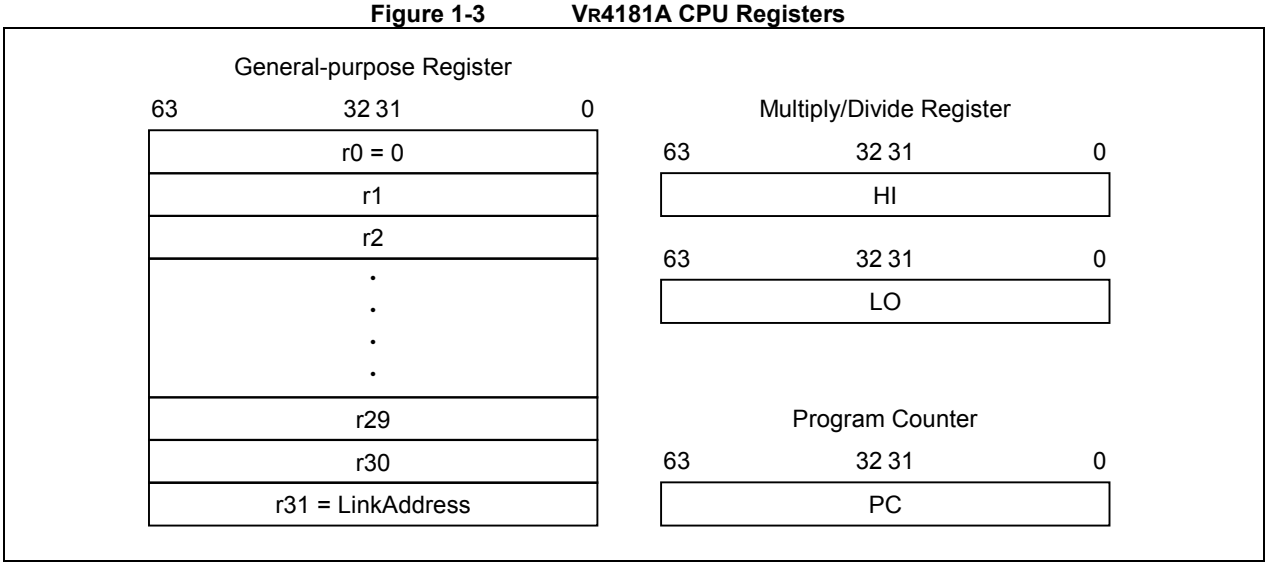
- r0 is fixed to 0, and can be used as the target register for any instruction whose result is to be discarded. r0 can also be used as a source register when a zero value is needed.
- r31 is the link register used by link instructions such as JAL (jump and link) instructions. This register can be used for other instructions. However, be careful that use of the register by a link instruction will not coincide with use of the register for other operations.

The register group is provided within the CP0 (system control coprocessor), to process exceptions and to manage addresses. CPU registers can operate as either 32-bit or 64-bit registers, depending on the VR4181A processor operation mode.

The operation of the CPU register differs depending on what instructions are executed: 32-bit instructions or MIPS16 instructions. For details, refer to **CHAPTER 4 MIPS16 INSTRUCTION SET**.

Figure 1-3 shows the CPU registers.

Figure 1-3 VR4181A CPU Registers



The VR4181A has no program status word (PSW) register as such; this is covered by the status and cause registers incorporated within the system control coprocessor (CP0). For details of CP0 registers, refer to **1.5.5 System control coprocessor (CP0).**

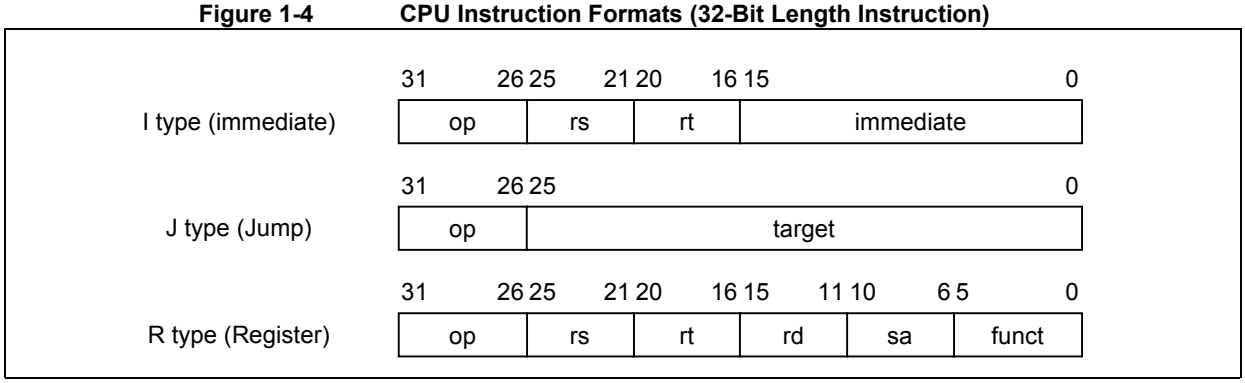
1.5.3 CPU instruction set overview

There are two types of CPU instructions: 32-bit length instructions (MIPS III) and 16-bit length instructions (MIPS16).

(1) MIPS III instructions

All the CPU instructions are 32-bit length when executing MIPS III instructions, and they are classified into three instruction formats as shown in Figure 1-4: immediate (I type), jump (J type), and register (R type). The field of each instruction format is described in **CHAPTER 3 MIPS III INSTRUCTION SET SUMMARY**.

Figure 1-4 CPU Instruction Formats (32-Bit Length Instruction)



The instruction set can be further divided into the following five groupings:

(a) Load and store instructions move data between the memory and the general-purpose registers. They are all immediate (I-type) instructions, since the only addressing mode supported is base register plus 16-bit, signed immediate offset.

(b) Computational instructions perform arithmetic, logical, shift, and multiply and divide operations on values in registers. They include R-type (in which both the operands and the result are stored in registers) and I-type (in which one operand is a 16-bit signed immediate value) formats.

(c) Jump and branch instructions change the control flow of a program. Jumps are made either to an absolute address formed by combining a 26-bit target address with the higher bits of the program counter (J-type format) or register-specified address (R-type format). The format of the branch instructions is I type. Branches have 16-bit offsets relative to the program counter. JAL instructions save their return address in register 31.

(d) System control coprocessor (CP0) instructions perform operations on CP0 registers to control the memory-management and exception-handling facilities of the processor.

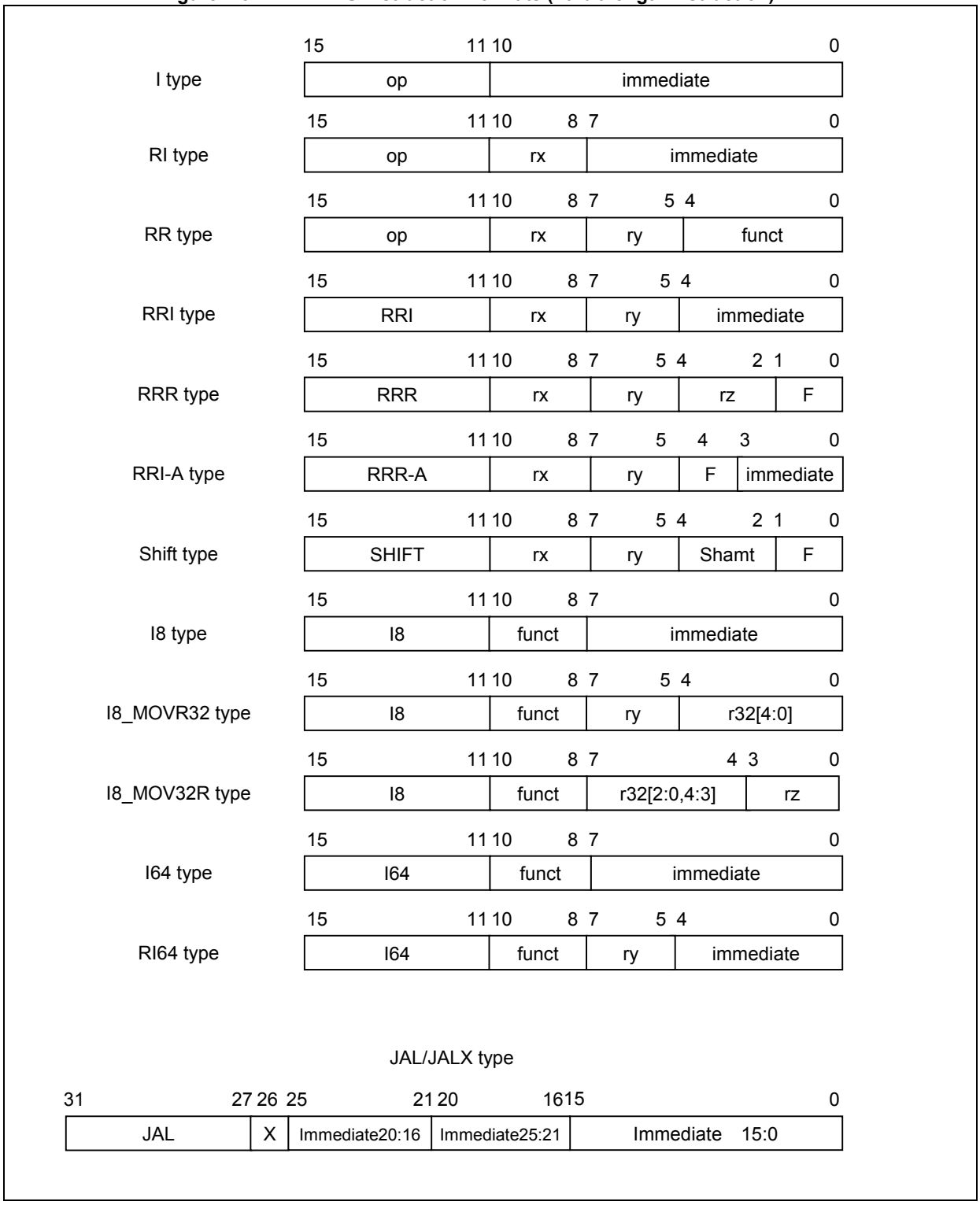
(e) Special instructions perform system calls and breakpoint exceptions, or cause a branch to the general exception-handling vector based upon the result of a comparison. These instructions occur in both R-type and I-type formats.

For the operation of each instruction, refer to **CHAPTER 3 MIPS III INSTRUCTION SET SUMMARY** and **CHAPTER 27 MIPS III INSTRUCTION SET DETAILS.**

(2) MIPS16 instructions

All the CPU instructions except for JAL and JALX are 16-bit length when executing MIPS16 instructions, and they are classified into thirteen instruction formats as shown in Figure 1-5. The field of each instruction format is described in **CHAPTER 4 MIPS 16 INSTRUCTION SET.**

Figure 1-5 CPU Instruction Formats (16-bit length instruction)



The instruction set can be further divided into the following four groupings:

(a) Load and store instructions move data between memory and general-purpose registers. They include RRI, RI, I8, and RI64 types.

(b) Computational instructions perform arithmetic, logical, shift, and multiply and divide operations on values in registers. They include RI-, RRIA, I8, RI64, I64, RR, RRR, I8_MOVR32, and I8_MOV32R types.

(c) Jump and branch instructions change the control flow of a program. They include JAL/JALX, RR, RI, I8, and I types.

(d) Special instructions are Break and Extend instructions. The Break instruction transfers control to an exception handler. The Extend instruction extends the immediate field of the next instruction. They are RR and I types. When extending the immediate field of the next instruction by using the Extend instruction, one cycle is needed for executing the Extend instruction, and another cycle is needed for executing the next instruction.

For more details of each instruction's operation, refer to **CHAPTER 4 MIPS16 INSTRUCTION SET** and **CHAPTER 34 MIPS16 INSTRUCTION SET FORMAT**.

1.5.4 Data formats and addressing

The VR4181A uses following four data formats:

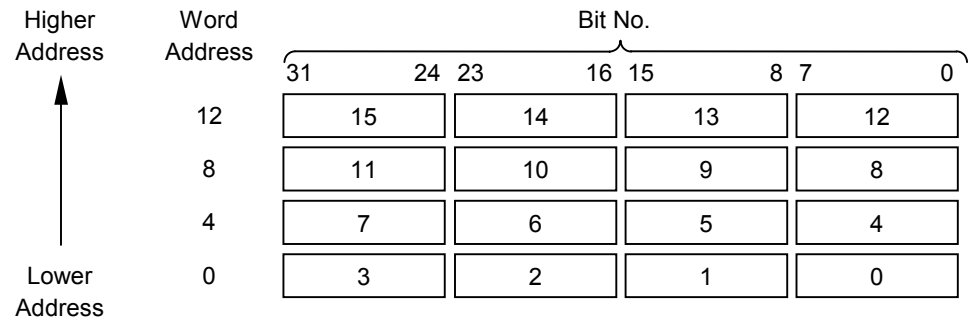
- Doubleword (64 bits)
- Word (32 bits)
- Halfword (16 bits)
- Byte (8 bits)

In the CPU core, if the data format is any one of halfword, word, or doubleword, the byte ordering can be set as either big endian or little endian. **However, the VR4181A only supports the little-endian order.**

Endianness refers to the location of byte 0 within the multi-byte data structure. When configured as a little-endian system, byte 0 is always the least-significant (rightmost) byte, which is compatible with iAPX ™ and DEC VAX ™ conventions. Figures 1-6 and 1-7 show this configuration.

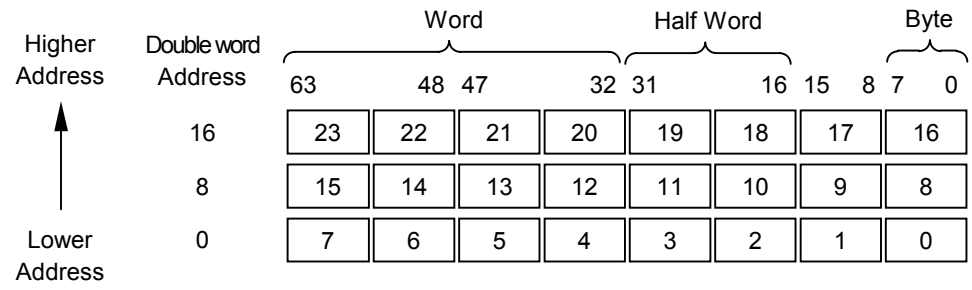
In this manual, bit designations are always little endian.

Figure 1-6 Little-Endian Byte Ordering in Word Data



Remarks 1. The lowest byte is the lowest address.
2. The address of word data is specified by the lowest byte's address.

Figure 1-7 Little-Endian Byte Ordering in Double word Data



Remarks 1. The lowest byte is the lowest address.
2. The address of word data is specified by the lowest byte's address.

The CPU core uses the following byte boundaries for halfword, word, and doubleword accesses:

- Halfword: An even byte boundary (0, 2, 4...)
- Word: A byte boundary divisible by four (0, 4, 8...)
- Doubleword: A byte boundary divisible by eight (0, 8, 16...)

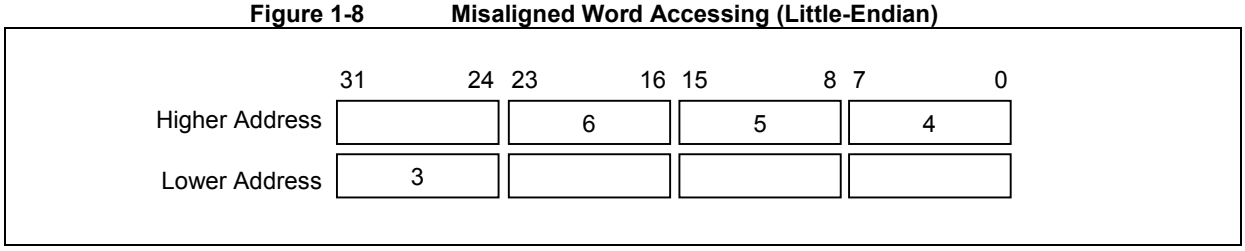
The following special instructions are used to load and store data that are not aligned on 4-byte (word) or 8-byte (doubleword) boundaries:

LWL	LWR	SWL	SWR
LDL	LDR	SDL	SDR

These instructions are used in pairs to provide access to misaligned data. Accessing misaligned data requires one additional instruction cycle (I Pcycle) over that required for accessing aligned data.

Figure 1-8 shows the access of a misaligned word that has byte address 3.

Figure 1-8 Misaligned Word Accessing (Little-Endian)



1.5.5 System control coprocessor (CP0)

MIPS ISA defines 4 types of coprocessors (CP0 to CP3).

- CP0 translates virtual addresses to physical addresses, switches the operating mode (kernel, supervisor, or user mode), and manages exceptions. It also controls the cache subsystem to analyze a cause and to return from the error state.
- CP1 is reserved for floating-point instructions.
- CP2 is reserved for future definition by MIPS.
- CP3 is no longer defined. CP3 instructions are reserved for future extensions.

Figure 1-9 shows the definitions of the CP0 register, and Table 1-18 shows simple descriptions of each register. For detailed descriptions of the registers related to the virtual memory system, refer to **CHAPTER 6 MEMORY MANAGEMENT SYSTEM**. For detailed descriptions of the registers related to exception handling, refer to **CHAPTER 7 EXCEPTION PROCESSING**.

Figure 1-9 CP0 Registers

Register No.	Register name	Register No.	Register name
0	Index[Note1]	16	Config[Note1]
1	Random[Note1]	17	LLAddr[Note1]
2	EntryLo0[Note1]	18	WatchLo[Note2]
3	EntryLo1[Note1]	19	WatchHi[Note2]
4	Context[Note2]	20	Xcontext[Note2]
5	PageMask[Note1]	21	RFU
6	Wired[Note1]	22	RFU
7	RFU	23	RFU
8	BadVAddr[Note1]	24	RFU
9	Count[Note2]	25	RFU
10	EntryHi[Note1]	26	Parity error[Note2]
11	Compare[Note2]	27	Cache error[Note2]
12	Status[Note2]	28	TagLo[Note1]
13	Cause[Note2]	29	TagHi[Note1]
14	EPC[Note2]	30	ErrorEPC[Note2]
15	PRId[Note1]	31	RFU

Notes **1.** For memory management
2. For exception handling

Remark RFU: Reserved for future use

Table 1-9 System Control Coprocessor (CP0) Register Definitions

Register Number	Register Name	Description
0	Index	Programmable pointer to TLB array
1	Random	Pseudo-random pointer to TLB array (read only)
2	EntryLo0	Lower half of TLB entry for even VPN
3	EntryLo1	Lower half of TLB entry for odd VPN
4	Context	Pointer to kernel virtual PTE in 32-bit mode
5	PageMask	Page size specification
6	Wired	Number of wired TLB entries
7	RFU	
8	BadVAddr	Virtual address where the most recent error occurred
9	Count	Timer count
10	EntryHi	Upper half of TLB entry (including ASID)
11	Compare	Timer compare
12	Status	Status register
13	Cause	Cause of last exception
14	EPC	Exception program counter
15	PRId	Processor revision identifier
16	Config	Memory mode system specification
17	LLAddr	Reserved for future use
18	WatchLo	Memory reference trap address lower bits
19	WatchHi	Memory reference trap address higher bits
20	XContext	Pointer to kernel virtual PTE in 64-bit mode
21-25	RFU	
26	Parity error Note	Cache parity bits
27	Cache error Note	Index and status of cache error
28	TagLo	Cache tag register (low)
29	TagHi	Cache tag register (high)
30	ErrorEPC	Error exception program counter
31	RFU	

Note This register is defined to maintain compatibility with the VR4100™. This register is not used in the VR4181A hardware.

1.5.6 Floating-point unit (FPU)

The VR4181A does not support the floating-point unit (FPU). A coprocessor unusable exception will occur if any FPU instructions are executed. If necessary, FPU instructions should be emulated by software in an exception handler.

1.6 CPU Core Memory Management System

The VR4181A has a 32-bit physical addressing range of 4 GB. However, since it is rare for systems to implement a physical memory space as large as that memory space, the CPU provides a logical expansion of memory space by translating addresses composed in the large virtual address space into available physical memory addresses.

The VR4181A supports the following two addressing modes:

- 32-bit mode, in which the virtual address space is divided into 2 GB for user processing and 2 GB for the kernel.
- 64-bit mode, in which the virtual address space is expanded to 1 TB (2^{40}bytes) of user virtual address space.

A detailed description of these address spaces is given in **CHAPTER 6 MEMORY MANAGEMENT SYSTEM.**

1.6.1 Translation lookaside buffer (TLB)

Virtual memory mapping is performed using the translation lookaside buffer (TLB). The TLB converts virtual addresses to physical addresses. It runs by a full-associative method and has 32 entries, each mapping a pair of two consecutive pages. The page size is variable between 1 KB and 256 KB, in powers of 4.

(1) Joint TLB (JTLB)

The JTLB holds both instruction and data addresses.

For fast virtual-to-physical address decoding, the vR4122 uses a large, fully associative TLB (joint TLB) that translates 64 virtual pages to their corresponding physical addresses. The TLB is organized as 32 pairs of even-odd entries, and maps a virtual address and address space identifier (ASID) into the 4 GB physical address space.

The page size can be configured, on a per-entry basis, to map a page size of 1 KB to 256 KB. A CP0 register stores the size of the page to be mapped, and that size is entered into the TLB when a new entry is written. Thus, operating systems can provide special purpose maps; for example, a typical frame buffer can be memory-mapped using only one TLB entry.

Translating a virtual address to a physical address begins by comparing the virtual address from the processor with the physical addresses in the TLB; there is a match when the virtual page number (VPN) of the address is the same as the VPN field of the entry, and either the global (G) bit of the TLB entry is set, or the ASID field of the virtual address is the same as the ASID field of the TLB entry.

This match is referred to as a TLB hit. If there is no match, a TLB miss exception is taken by the processor and software is allowed to refill the TLB from a page table of virtual/physical addresses in memory.

1.6.2 Operating modes

The VR4181A has the following three operating modes:

- User mode
- Supervisor mode
- Kernel mode

The manner in which memory addresses are translated or mapped depends on these operating modes. Refer to **CHAPTER 6 MEMORY MANAGEMENT SYSTEM** for details.

1.6.3 Cache

The VR4181A chip incorporates instruction and data caches, which are independent of each other. This configuration enables high-performance pipeline operations. Both caches have a 64-bit data bus, enabling a one-clock access. These buses can be accessed in parallel. The instruction cache of the VR4181A has a storage capacity of 8 KB, while the data cache has a capacity of 8 KB.

A detailed description of caches is given in **CHAPETER 9 CACHE MEMORY**.

1.7 Instruction Pipeline

The VR4181A has a 6-stage instruction pipeline. Under normal circumstances, one instruction is issued each cycle. A detailed description of the pipeline is provided in **CHAPTER 5 VR4181A PIPELINE**.

1.8 Clock Interface

The VR4181A has the following 13 clocks.

- **CLKX1, CLKX2 (input)**

  These are 18.432 MHz resonator inputs, and are used to generate operation clocks (AClock) for the CPU core. They are also used for the PIU, AIU, SIU, CSI, I2S

- **RTCX1, RTCX2 (input)**

  These are 32.768 kHz resonator inputs, which are used by the PMU, RTC, DSU, PWM, touch panel interface, and keyboard interface. They are also used as the main operation clock for some of the GPIO pins. Only this clock continues to operate when the system is in Hibernate mode.

- **AClock (internal)**

This clock is used to control the pipeline used in the VR4120 CPU core, and for units relating to the pipeline. This clock is generated from the clock input of CLKX1 and CLKX2 pins. Its frequency is determined by CLKSEL(2:0) pins.

- **TClock (internal)**

This is the reference clock for on-chip peripheral operations. This clock is generated from the pipeline clock (Aclock). Its frequency is determined by DIVMODE(1:0) pins.

- **PCIClock (internal)**

This is the reference clock of the internal PCI bus. This clock is generated from AClock, and can be selected one of 1/3, 1/4 of AClock.

- **PClock (internal)**

This is the reference clock of the internal ISA bus. This clock is generated from TClock, and can be selected one of 1/1, 1/2, 1/4 of TClock.

- **LClock (internal)**

This is the reference clock of the external ISA / ROM interface. This clock is generated from TClock, and can be selected one of 1/1, 1/2, 1/3, 1/4 of TClock.

- **Ecu_SysClock (internal)**

This is the reference clock of the CompactFlash interface. This clock is generated from TClock, and can be selected one of 1/2, 1/4, 1/8 of TClock.

- **MasterOut (internal)**

This is the clock output from the VR4120 CPU Core and is used for interrupt control. The contents of the CP0 counter register are incremented in synchronization with this clock. The frequency is 1/4 of AClock.

- **CLK48 (input)**

This is a 48 MHz clock input, and used for USB(HOST/Client).

- **SDCLK (output)**

SDCLK supplies the CLK pins of SDRAM with the clock. It has the same frequency as TClock and operates only when accessing SDRAM.

- **SCLK (I/O)**

This is a 4 MHz (max) clock input at slave mode, and used for I2S Stereo Audio Codec interface. At master mode, this clock is generated based on CLK18 internally.

• **SCK (I/O)**

This is a 4.6 MHz (max) clock input at slave mode, and used for Clocked Serial interface (CSI). At master mode, this clock is generated based on CLK18 internally.

• **BITCLK (input)**

This is a 12.288 MHz clock input, and used for AC97 Stereo Audio Codec interface.

• **SCL0, SCL1 (I/O)**

This is a 400 KHz (max) clock input at slave mode, and used for I2C Serial interface. At master mode, this clock is generated based on CLK18 internally.

• **GCLK (internal)**

This is used for LCD controller. This clock is generated from TClock, and can be selected one of 1/1, 1/2, 1/4 of TClock. This clock is used as the pre-clock for HPCK below.

•**HPCK (internal)**

This is the reference clock of the LCD controller. The timing to send the pixel data is decided by this clock. This clock is generated from GCLK above.

•**DCLK / SHCLK (output)**

The timing to send the pixel data is decided by this clock. This clock has the same frequency as HPCK.

•**HSYNC / LOCLK (output)**

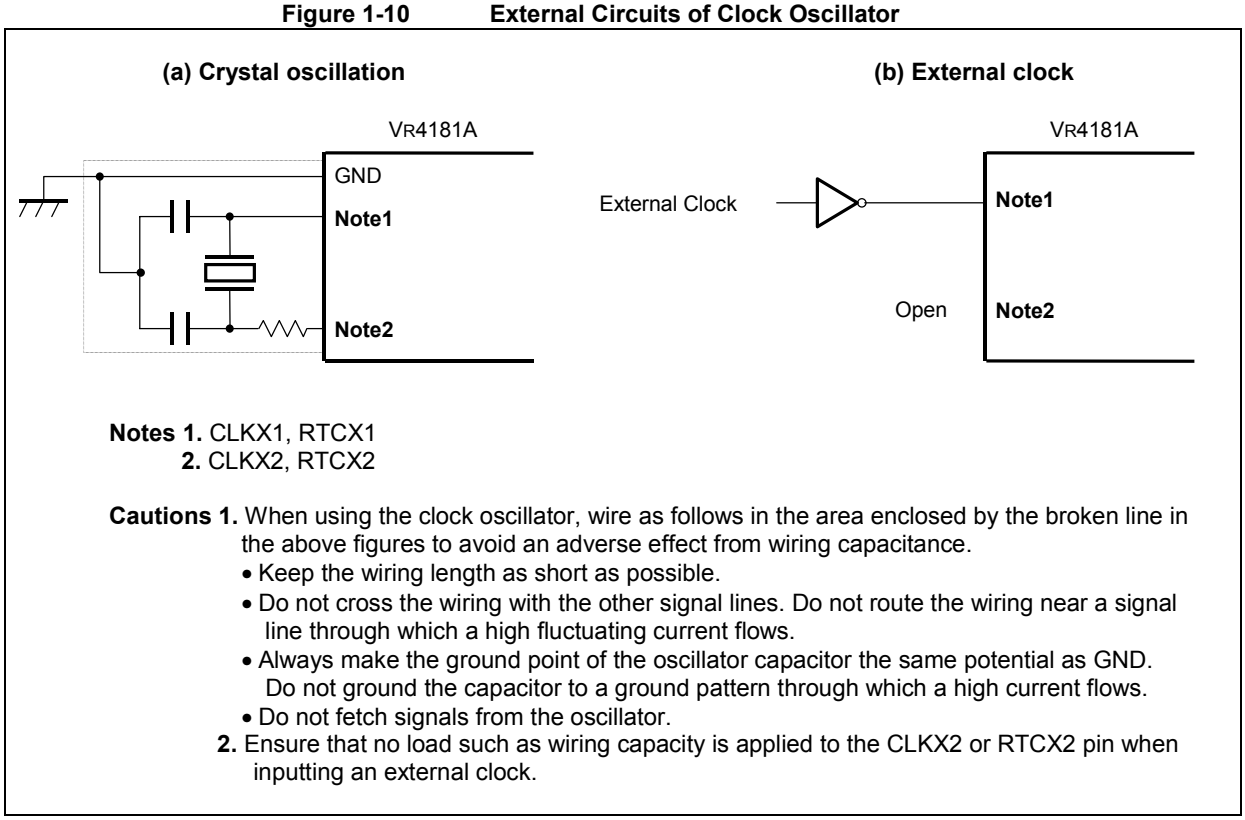
The timing to send the pixel line is decided by this clock.

•**VSYNC / FLM (output)**

The timing to send the pixel frame is decided by this clock.

Figure 1-10 shows the external circuits of the clock oscillator.

Figure 1-10 External Circuits of Clock Oscillator



Notes 1. CLKX1, RTCX1
2. CLKX2, RTCX2

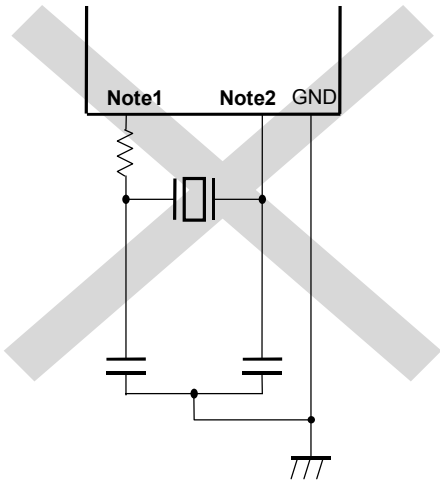
Cautions 1. When using the clock oscillator, wire as follows in the area enclosed by the broken line in the above figures to avoid an adverse effect from wiring capacitance.
- Keep the wiring length as short as possible.
- Do not cross the wiring with the other signal lines. Do not route the wiring near a signal line through which a high fluctuating current flows.
- Always make the ground point of the oscillator capacitor the same potential as GND. Do not ground the capacitor to a ground pattern through which a high current flows.
- Do not fetch signals from the oscillator.

2. Ensure that no load such as wiring capacity is applied to the CLKX2 or RTCX2 pin when inputting an external clock.

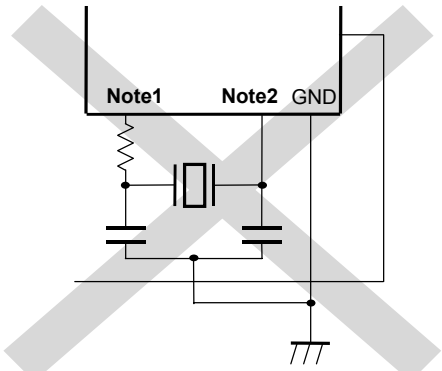
Figure 1-11 shows examples of the incorrect connection circuit of the resonator.

Figure 1-11 Incorrect Connection Circuits of Resonator

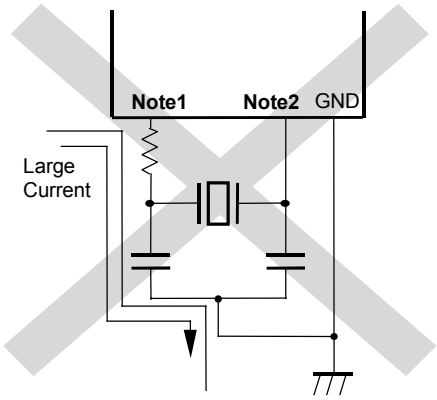
(a) Connection circuit wiring is too long.



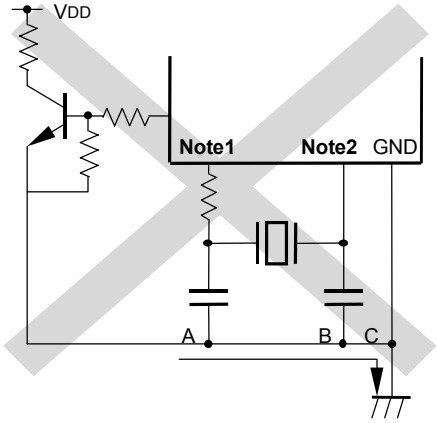
(b) There is another signal line crossing.



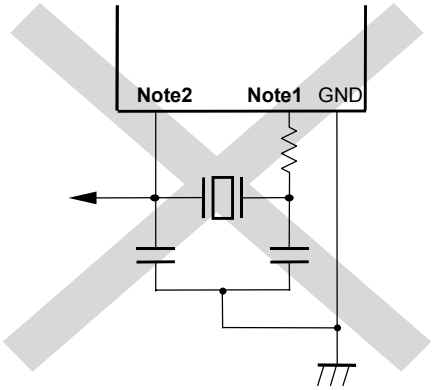
(c) A high fluctuating current flows near a signal line.



(d) A current flows over the ground line of the oscillator (The potentials of points A, B, and C change).



(e) A signal is fetched.



Notes 1. CLKX2, RTCX2
2. CLKX1, RTCX1