To our customers,

Old Company Name in Catalogs and Other Documents

On April 1st, 2010, NEC Electronics Corporation merged with Renesas Technology Corporation, and Renesas Electronics Corporation took over all the business of both companies. Therefore, although the old company name remains in this document, it is a valid Renesas Electronics document. We appreciate your understanding.

Renesas Electronics website: http://www.renesas.com

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Renesas Electronics Corporation

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RENESAS TECHNICAL UPDATE

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Product Category	MPU/MCU		Document No.	TN-SH7-A730A/E	Rev.	1.00
Title	Usage restrictions of SH7764		Information Category	Technical Notification		
Applicable Product	SH7764 Group: R5S77640N300BG, R5S77640D300BG, R5S77640P300BG, R5S77641N300BG, R5S77641D300BG, R5S77641P300BG	Lot No. All	Reference Document	SH7764 Group Hardware Manual (REJ09B0360-0100)		

Dear value customer,

Please be informed that there are specific restrictions for Serial Sound Interface (SSI) and Direct Memory Access Controller (DMAC) of SH7764.

- Descriptions -

1. Specific restrictions for SSI

Please do not write 1 to RDSAM bit in DMA Mode Registers 0 to 5 (SSIDMMR0 to SSIDMMR5) of SSI. (Please do not select decremental mode on RDSAM bit.) If RDSAM bit is set to 1, RDMA may be unable to read memory normally.

Please do not write 1 to WDDAM bit in DMA Mode Registers 0 to 5 (SSIDMMR0 to SSIDMMR5) of SSI. (Please do not select decremental mode on WDDAM bit.) If WDDAM bit is set to 1, WDMA may be unable to write memory normally.

2. Specific restrictions for DMAC

If transfer request source (*1) is each one of following, neither transition to sleep mode, cancelling sleep mode, clearing the DE bit (*2) of the relevant DMAC channel nor clearing the DME bit (*3) must be performed. The controversial transfer request sources are USB (transmit), USB (receive), FLCTL (transmit and receive the data section), FLCTL (transmit and receive the control code section), SRC (transfer data from SRCOD), SDHI (transmit), SDHI (receive) and DREQ pins. If this restriction is violated, DMAC may make two transmits on one transmit request.
As a countermeasure, transition to Sleep Mode, canceling Sleep Mode, clearing DE bit(*2) of corresponding channel or clearing DME bit(*3) should be performed after DMAC transfer (i.e. after Transfer End interrupt).

Under the same operating condition, if address error exception (event which makes AE bit (*4) be set to 1) or NMI exception occurs, DMAC may make two transmits on one transmit request.

*1: Transfer request source is defined by RS[3:0] bit in DMA Channel Control Registers (CHCR0 to CHCR5) and DMA Extended Resource Selectors (DMARS0 to DMARS2).
*2: Bit 0 in DMA Channel Control Registers (CHCR0 to CHCR5).
*3: Bit 0 in DMA Operation Register 0 (DMAOR0).
*4: Bit 2 in DMA Operation Register 0 (DMAOR0).