HITACHI SEMICONDUCTOR TECHNICAL UPDATE

DATE	October 27, 1999	No.	TN-SH7-192 A/E
THEME	Usage notice when using DMAC at clock mode 3 or 4		
CLASSIFICATION	☐ Spec. change ☐ Supplement of Documents	■ Limitation on Use	
PRODUCT NAME	HD6417709A, HD6417729		
REFERENCE DOCUMENTS	SH7709A (HD6417709A) Hardware manual SH7729 (HD6417729) Hardware manu	Effective Date From	Permanent

The following is a usage notice for SH7709A and SH7729.

<Condition>

When using DMAC at clock mode 3 or 4, illegal bus cycle may be occurred by the jitter of embedded PLL due to the noise on Vcc/Vss line.

<Phenomenon>

(1) When using DMAC at clock mode 3 or 4, please take steps to reduce the influence of noise; for example, mounting decoupling capacitors in each Vcc/Vss pair. Condenser capacity value is differ from on-board condition.

Vcc/Vss pairs:

19-21, 27-39, 33-35, 45-47, 57-59, 69-71, 79-81, 83-85, 95-97, 109-111,
132-134, 153-154, 161-163, 173-175, 181-183, 205-208
3-6, 145-147, 148-150

Please refer to the following chapter of the hardware manual.

a) SH7709A hardware manual : 9.11 Notes on Board Design
b) SH7729 hardware manual : 10.11 Notes on Board Design

(2) When the above (1) is insufficient, please use the clock mode 0,1,2 or 7 with DMAC.