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RENESAS TECHNICAL UPDATE

1753, Shimonumabe, Nakahara-ku, Kawasaki-shi, Kanagawa 211-8668 Japan
Renesas Electronics Corporation

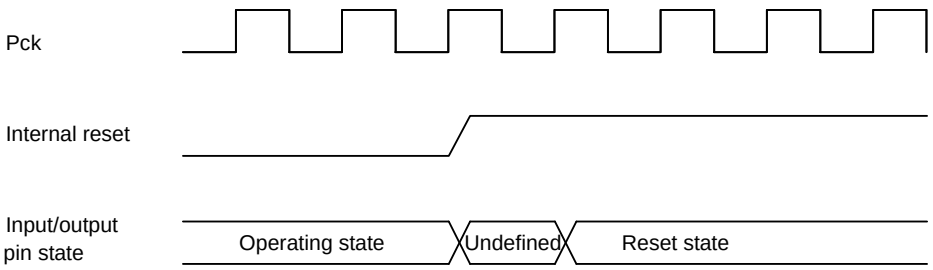
Product Category	MPU/MCU		Document No.	TN-SH7-A820A/E	Rev.	1.00
Title	Usage notes regarding internal reset		Information Category	Technical Notification		
Applicable Product	SH7450 Group, SH7451 Group SH7455 Group, SH7456 Group	Lot No.	Reference Document	SH7450 Group, SH7451 Group Hardware Manual REV.1.00 SH7455 Group, SH7456 Group User's Manual REV.0.50		

We would like to inform you of the usage notes regarding internal reset.

<Usage Note>

When the microcontroller is changing to reset status caused by an internal reset, there will be a period of one peripheral clock (Pck), where I/O ports will be undefined. Undefined state could be either high level output or low level output or high impedance states.

The microcontroller, including I/O ports, will correctly transfer to reset status after this period.



<Additional Information>

All I/O ports have this phenomenon; with the exception of input dedicated or output dedicated ports.

Internal resets can be caused by the following.

1. Reset by Watchdog timer (WDT) overflow
2. H-UDI reset during debug
3. Reset by exception

Reset by inputting a low signal to RESET# pin is not an internal reset.