NEC Microcomputer Technical Information

CP(K), O

μPD789830 Subseries Usage Restrictions		Document No.	SBG-DT-0017-E		1/1
		Date issued	October 5, 2001		
		Issued by	Microcomputer Group Sales Engineering Div. NEC Electron Devices NEC Corporation		
Related documents	User's manual (U13679EJ1V0UM00) Data sheet (U14284EJ1V0DS00) Data sheet (U13477EJ1V0DS00)	Notification classification	√	Usage restriction	
				Upgrade	
				Document modification	
				Other notification	

1. Affected products

   μPD789830

   μPD78F9831

2. Technical information

   The following restriction has been found in the above products.

   - The LSB should be read first in UART reception. Under certain conditions, however, the MSB of the receive data is read first.

3. Workaround

   Implement the workaround described in Attachment 4 to avoid the restriction above.

4. Correction

   Regard the restriction added in this document as a usage restriction.

5. List of restrictions

   The restriction history and detailed information is described in Attachment 1.

List of Usage Restrictions in μPD789830 Subseries

1. Product History

<Mask ROM version>

Description		UPD789830
	Rank	All Ranks
Item 1	Restriction on 16-bit timer	Δ
Item 2	Restriction on 8-bit timer	Δ
Item 3	Restriction on UART	Δ

<Flash memory version>

Description		UPD78F9831
	Rank	All Ranks
Item 1	Restriction on 16-bit timer	Δ
Item 2	Restriction on 8-bit timer	Δ
Item 3	Restriction on UART	Δ

Notes 1. The rank is indicated by the fifth character from the left in the lot number marked on the package.

2. The meaning of each symbol is as follows.

–: Restriction does not apply

√: Restriction already corrected

×: Restriction applies (correction is planned)

Δ: Restriction applies (correction is not planned)

2. Details of Usage Restrictions

Item 1: Refer to Attachment 2 for details.

Item 2: Refer to Attachment 3 for details.

Item 4: A restriction added this time. Refer to Attachment 4 for details.

Item 1. Restriction on 16-bit timer

[Description]
When the value of the compare register is overwritten in the interrupt routine for a match between the count value and the 16-bit compare register (CRxx) when the 16-bit timer is used as an interval timer, be sure to perform the following processing before overwriting the value.

<1> Mask the interrupt.
<2> Disable inversion control (TOCxx) of the timer output data.

An interrupt request may be generated if the value of the compare register is overwritten while interrupts are enabled.

Item 2. Restriction on 8-bit timer

[Description]
When the 8-bit timer is used in the interval timer mode, the value of the compare registers (CRxx) should be overwritten while the timer operation is disabled.
If the value of the compare register (CRxx) is overwritten while the timer operation is enabled, a match signal may be generated. (An interrupt request is generated when interrupts are enabled.)

Item 3. Restriction on UART

[Description]

The LSB should be read first in UART reception. Under certain conditions, however, the MSB of the receive data is read first.

[Workaround]

(1) Read the receive data when RXE = 1.

(2) If it is necessary to use the receive data before changing RXE from 1 to 0, read the receive data first, after the receive interrupt is generated, and then change RXE.

(3) When changing RXE from 1 to 0 before reading the receive data, insert a wait equivalent to 1 or more cycles of the source clock selected by BRGC before changing RXE.

```
MOV   BRGC,#00H   ; A wait equivalent to 1 cycle of the source clock selected by BRGC00 is
                  ; necessary. (e.g. 0.4 μs @ fx = 5 MHz)
```

Insert a wait according to the selected source clock (see the examples below.)

```
CLR1  RXE         ;
MOV   A,RXB       ; Read the receive data.
```

(Example)

♦ When 1 source clock cycle ≥ 3.2 μs is selected

```
        MOV   A,#01H        ; 6 clocks (1.2 μs @ fx = 5 MHz)
LABEL: DEC    A             ; 4 clocks (0.8 μs @ fx = 5 MHz)
        BNZ   BNZ   LABEL   ; 6 clocks (1.2 μs @ fx = 5 MHz)
```

♦ When 1 source clock cycle ≤ 3.2 μs is selected

```
        NOP                 ; 2 clocks (0.4 μs @ fx = 5 MHz)
```

(4) When changing RXE from 1 to 0 without inserting a wait equivalent to 1 or more cycles of the source clock selected by BRGC, read the receive data when RXE = 0 and DIR = 1.

```
SET1  DIR         ; Set the DIR flag to LSB-first.
CLR1  RXE         ;
MOV   A,RXB       ; Read the receive data.
```