NEC Microcomputer Technical Information

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1. Affected products

   μPD789477, 78F9478

2. Technical information

   The following restriction has been found in the above products.

   - Restriction on UART (mask ROM/flash memory products)

     The LSB should be read first in UART reception. Under certain conditions, however, the MSB of the receive data is read first.

3. Workaround

   Implement the workaround described in Attachment 3 to avoid the restriction above.

4. Correction

   Regard the restriction added in this document as a usage restriction.

5. List of restrictions

   The restriction history and detailed information is described in Attachment 1.

List of Usage Restrictions in μPD789477 Subseries

1. Product History

<Mask ROM version>

Description		UPD789477
	Rank	All Ranks
Item 1	Restriction on 16-bit timer	Δ
Item 2	Restriction on UART	Δ

<Flash memory version>

Description		UPD78F9478
	Rank	All Ranks
Item 1	Restriction on 16-bit timer	Δ
Item 2	Restriction on UART	Δ

Notes 1. The rank is indicated by the fifth character from the left in the lot number marked on the package.

2. The meaning of each symbol is as follows.
√: Corrected, Δ: Restriction will apply in future, ×: Bug occurs, –: Not relevant

2. Details of Usage Restrictions

Item 1: Refer to Attachment 2 for details.

Item 2: A restriction added this time. Refer to Attachment 3 for details.

3. Other Cautions

None.

Item 1. Restriction on 16-bit timer

[Description]

When the 16-bit timer (timer 20) are used as an interval timer, the interval may become twice the expected value depending on the timing at which the compare register is written.

In addition, when the timer output is being used, a waveform shorter than expected or twice the frequency expected is output if the above conditions are met.

[Workaround]

Implement one of the following workarounds when rewriting the compare register (CR20) of the 16-bit timer (timer 20)

(1) Write writing using 8-bit access

Write to the 16-bit CR20 register by writing the highest byte first, then the lowest byte. At this time, be sure to clear the interrupt request flag (TMIF20) before enabling timer interrupts and timer output inversion.

After writing to CR20, do not set TOC20 until at least half a cycle of the count clock has passed since the start of an interrupt. (The signal INTTM20 is high for a period of half a cycle of the count clock after an interrupt is generated. If TOC20 is set within this period, the output is inverted.)

<Program example>

(When count clock = 64/fx, CPU clock = fx)

```
TM20_VCT:           SET1    TMMK20      ; Disable timer interrupts (6 clock pulses)
                    CLR1    TOC20       ; Disable timer output inversion (6 clock pulses)
                    MOV     A,#xxH      ; Set value to write highest byte (6 clock pulses)
  32 clock          MOV     !0FF17H,A   ; Write higher byte of CR20 (8 clock pulses)
  pulses in total   MOV     A,#xxH      ; Set value to write lowest byte (6 clock pulses)
                    MOV     !0FF16H,A   ; Write lowest byte of CR20 (8 clock pulses)
                    CLR1    TMIF20      ; Clear interrupt request flag (6 clock pulses)
                    CLR1    TMMK20      ; Enable interrupts (6 clock pulses)
                    SET1    TOC20       ; Enable output inversion
```

(2) When writing using 16-bit access

After the instruction (MOVW CR20, AX) that writes to CR20, be sure to insert a wait of at least 1 clock cycle of the count clock before enabling timer interrupts and timer output inversion.

<Program example>

(When count clock = 64/fx, CPU clock = fx)

```
SET1    TMMK20    ; Disable timer interrupts
CLR1    TOC20     ; Disable timer output inversion
MOVW    AX,#xxH   ; Set value to write CR20
MOVW    CR20,AX   ; Write CR20
NOP               }
NOP               }
  :               } ; 32 x NOP (64/fx wait)
NOP               }
NOP               }
CLR1    TMIF20    ; Clear interrupt request flag
CLR1    TMMK20    ; Enable interrupts
SET1    TOC20     ; Enable output inversion
```

Also, be sure to disable timer interrupts and output inversion before writing CR20.

Item 2. Restriction on UART

[Description]

The LSB should be read first in UART reception. Under certain conditions, however, the MSB of the receive data is read first.

[Workaround]

(1) Read the receive data when RXE = 1.

(2) If it is necessary to use the receive data before changing RXE from 1 to 0, read the receive data first, after the receive interrupt is generated, and then change RXE.

(3) When changing RXE from 1 to 0 before reading the receive data, insert a wait equivalent to 1 or more cycles of the source clock selected by BRGC before changing RXE.

```
MOV   BRGC,#00H   ; A wait equivalent to 1 cycle of the source clock selected by BRGC00 is
                  ; necessary. (e.g. 0.4 μs @ fx = 5 MHz)
```

Insert a wait according to the selected source clock (see the examples below.)

```
CLR1  RXE         ;
MOV   A,RXB       ; Read the receive data.
```

(Example)

♦ When 1 source clock cycle ≥ 3.2 μs is selected

```
        MOV   A,#01H        ; 6 clocks (1.2 μs @ fx = 5 MHz)
LABEL: DEC    A             ; 4 clocks (0.8 μs @ fx = 5 MHz)
        BNZ   BNZ   LABEL   ; 6 clocks (1.2 μs @ fx = 5 MHz)
```

♦ When 1 source clock cycle ≤ 3.2 μs is selected

```
        NOP                 ; 2 clocks (0.4 μs @ fx = 5 MHz)
```

(4) When changing RXE from 1 to 0 without inserting a wait equivalent to 1 or more cycles of the source clock selected by BRGC, read the receive data when RXE = 0 and DIR = 1.

```
SET1  DIR         ; Set the DIR flag to LSB-first.
CLR1  RXE         ;
MOV   A,RXB       ; Read the receive data.
```