Microcomputer Technical Information

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μPD789014 Subseries Usage Restrictions	Document No.	SBG-DT-03-0185-E		1/2
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	Issued by	Microcomputer Group 2nd Solutions Division Solutions Operations Unit NEC Electronics Corporation		
Related documents μPD789014 Subseries User's manual: U11187EJ3V0UM00 μPD789011, 789012 Data sheet: U11095EJ1V1DS00 μPD78P9014 Data sheet: U10912EJ1V0DS00	Notification classification	√	Usage restriction	
			Upgrade	
		√	Document modification	
			Other notification	

1. Affected products

μPD789011, 789012

μPD78P9014

2. Details of modification and added restriction

(1) Error on starting 8-bit timer

The description in **6.5 Notes on Using 8-Bit Timer/Event Counters (1) Error on starting timer** in the user's manual (U11187EJ3V0UMJ1) has been corrected as follows.

(Incorrect)

An error of up to 1 clock occurs after the timer has been started until a match signal is generated.

(Correct)

An error of up to 1.5 clocks occurs after the timer has been started until a match signal is generated.

(2) Restriction when an external event is selected for the timer count clock

If an external event (TIx pin input) is selected for the timer count clock when the 8-bit timer/event counter is used, the count may be incremented after the count operation flag (TCExx) is set, depending on the status of the valid edge and TI pin.

See attachment 5 for details.

3. Correction

Regard the restriction added in this document as a usage restriction.

4. List of restrictions

The restriction history and detailed information is described in attachment 1.

5. Document revision history

μPD789014 Subseries Usage Restrictions

Document Number	Date Issued	Description
SBG-DT-0009-E	October 5, 2001	Newly created.
SBG-DT-03-0185-E	July 18, 2003	2nd edition Addition of new restriction (No.4)

List of Usage Restrictions in μPD789014 Subseries

1. Product History

<Mask ROM version>

Description		μPD789011, 789012
	Rank	All Ranks
1	Restriction on 8-bit timer (1)	Δ
2	Restriction on serial interface	Δ
3	Restriction on UART	Δ
4	Restriction on 8-bit timer (2)	Δ

<PROM version>

Description		μPD78P9014
	Rank	All Ranks
1	Restriction on 8-bit timer (1)	Δ
2	Restriction on serial interface	Δ
3	Restriction on UART	Δ
4	Restriction on 8-bit timer (2)	Δ

Notes 1. The rank is indicated by the fifth character from the left in the lot number marked on the package.

2. The meaning of each symbol is as follows.

–: Restriction does not apply

√: Restriction already corrected

×: Restriction applies (correction is planned)

Δ: Restriction applies (correction is not planned)

2. Details of Usage Restrictions

No.1: Refer to Attachment 2 for details.

No.2: Refer to Attachment 3 for details.

No.3: Refer to Attachment 4 for details.

No.4: A restriction added this time. Refer to Attachment 5 for details.

No.1 Restriction on 8-bit timer (1)

[Description]

When the 8-bit timer is used, the value of the compare register (CRxx) should be overwritten while the timer operation is disabled.

If the value of the compare register (CRxx) is overwritten while the timer operation is enabled, a match signal may be generated. (An interrupt request is generated when interrupts are enabled.)

No.2 Restriction on serial interface

[Description]

(1) Switching serial operation and general-purpose output port

(1)-1. 3-wire SIO mode

The output port that is alternately used by SO0 cannot be used as a general-purpose output port when data is transmitted/received in serial SIO mode and the operation is aborted (CSIE = 0), or when the operation enable flag is cleared (CSIE = 0) when neither transmission nor reception is performed.

(1)-2. UART mode

The output port that is alternately used by TXD cannot be used as a general-purpose output port when data is transmitted in UART mode and the operation is aborted (TXE = 0).

(2) Reading UART receive data

An overrun error occurs when a receive interrupt occurs in UART mode and if the RXB register is read before the clocks set in the “number of clocks to elapse until RXB is read” in the following table have elapsed after the start of the interrupt routine.

Table. Number of Clocks To Elapse Until RXB Is Read

BRGC Setting	Transfer Rate Note 1	Number of Clocks To Elapse Until RXB Is Read	
		Main High-Speed Operation (PCC1 = 0)	Main Medium-Speed Operation (PCC1 = 1)
00H	153.6 Kbps	0	0
10H	76.8 Kbps	0	0
20H	38.4 Kbps	0	0
30H	19.2 Kbps	7	2
40H	9.2 Kbps	23	6
50H	4.8 Kbps	55	14
60H	2.4 Kbps	119	30
70H	1.2 Kbps	247	62
80H	Satisfy the following expression for the external clock. EXCL1 (Hz) > f_{CPU} (Hz) / (9 clocks + X clocks) “EXCL1” is an external clock frequency and can be obtained by multiplying the transfer rate by 2^4. “f_{CPU}” is the operating frequency of the CPU. “9 clocks” are the total of the 1 clock from the occurrence of an interrupt until the start of the interrupt servicing, and the 8 clocks that are required for the interrupt servicing. “X clocks” are the number of clocks to elapse until the RXB register is read. The timing at which the RXB register is read differs depending on the application. **Example** The transfer rate is 300 bps, the CPU is operating at 1 MHz, and a 4.8 kHz external clock is input via EXCL1 4.8 kHz > 1 MHz/(9 + X) X > (1 MHz/4.8 kHz) – 9 X > 199.3 Therefore, 200 clocks should elapse before the RXB register is read.		

Remark f_X = 4.9152 MHz

[Workaround]

(1) Switching serial operation and general-purpose output port

(1)-1. 3-wire SIO mode

- Do not clear the operation enable flag (CSIE) until the end of the transmission/reception.
- Send FFH before clearing the operation enable flag (CSIE) when terminating 3-wire SIO mode, or send FFH as a UART transmission before clearing the transmit operation enable flag (TXE).

Example 1 3-wire SIO transmission

```
MOV CSIM0,#02H
MOV BRGC,#00H
MOV ASIM,#00H
MOV TXS,#0FFH
CLR1 CSIE
```

The SO pin goes high 4 clocks after TXS is written.
However the clock is supplied to the clock pin of SCK.

Example 2 UART transmission

```
MOV CSIM0,#00H
MOV BRGC,#00H
MOV ASIM,#80H
MOV TXS,#0FFH
CLR1 TXE
```

The SO pin goes high 16 to 32 clocks after TXS is written.
At this time, the SCK pin is held low.

(1)-2. UART mode

- Do not set the transmit operation enable flag (TXE) to 0 when a data transmission is in progress when transmission operations are enabled (TXE = 1). (If it is necessary to switch to the general-purpose output port, clear the transmit operation enable flag after the transmission is complete.)

Example Switch to the general-purpose output port after UART transmissions complete

```
MOV CSIM0,#00H
MOV BRGC,#40H      ; Baud rate: 9600bps
MOV ASIM,#88H      ; Data length: 8 bits, stop bit: 1 bit, without parity
WAIT:
BF STIF,$WAIT
CLR1 TXE
```

(2) Reading UART receive data

Read the RXB register after the clocks set in the “number of clocks to elapse until RXB is read” in the above table have elapsed in the UART receive interrupt routine.

No.3 Restriction on UART

[Description]

The LSB should be read first in UART reception. Under certain conditions, however, the MSB of the receive data is read first.

[Workaround]

(1) Read the receive data when RXE = 1.

(2) If it is necessary to use the receive data before changing RXE from 1 to 0, read the receive data first, after the receive interrupt is generated, and then change RXE.

(3) When changing RXE from 1 to 0 before reading the receive data, insert a wait equivalent to 1 or more cycles of the source clock selected by BRGC before changing RXE.

```
MOV    BRGC,#00H    ; A wait equivalent to 1 cycle of the source clock selected by BRGC00 is
                    ; necessary. (e.g. 0.4 μs @ fx = 5 MHz)
```

Insert a wait according to the selected source clock (see the examples below.)

```
CLR1   RXE          ;
MOV    A,RXB        ; Read the receive data.
```

(Example)

♦ When 1 source clock cycle ≥ 3.2 μs is selected

```
        MOV   A,#01H          ; 6 clocks (1.2 μs @ fx = 5 MHz)
LABEL:  DEC   A               ; 4 clocks (0.8 μs @ fx = 5 MHz)
        BNZ   BNZ     LABEL   ; 6 clocks (1.2 μs @ fx = 5 MHz)
```

♦ When 1 source clock cycle ≤ 3.2 μs is selected

```
        NOP                   ; 2 clocks (0.4 μs @ fx = 5 MHz)
```

(4) When changing RXE from 1 to 0 without inserting a wait equivalent to 1 or more cycles of the source clock selected by BRGC, read the receive data when RXE = 0 and DIR = 1.

```
SET1   DIR          ; Set the DIR flag to LSB-first.
CLR1   RXE          ;
MOV    A,RXB        ; Read the receive data.
```

No.4 Restriction on 8-bit timer (2)

(1) Error upon timer start

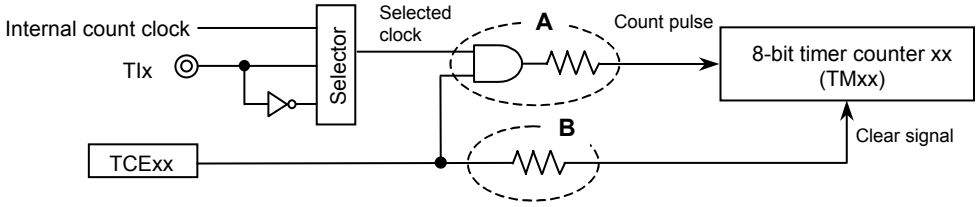
When the 8-bit timer/event counter is used, an error of up to 1.5 clocks is generated after the timer has been started until a match signal is generated. This is because a rising edge is detected when the timer is started while the selected clock is high, which results in the count value getting incremented.

[Details of restriction]

The basic timer configuration applicable to this restriction is shown in the figure below.

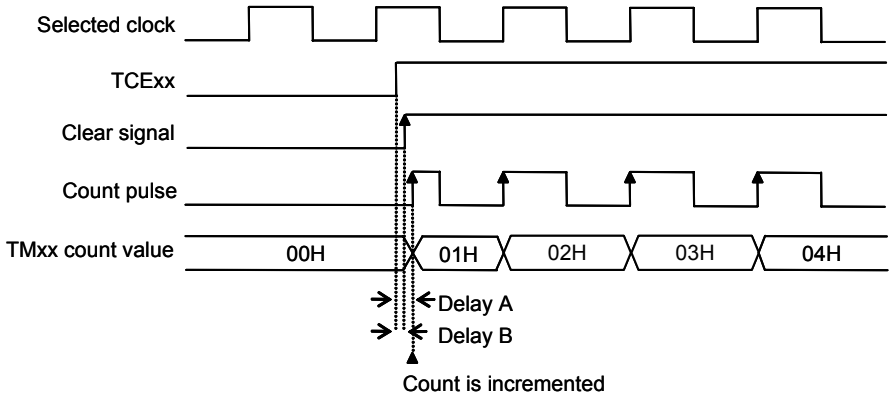
- The selected clock and the count operation flag (TCExx) are ANDed, and the result is supplied to the counter
- The TMxx counter value is cleared when the count operation flag (TCExx) is set

Basic Timer Configuration



If a count pulse is delayed for the clear signal (“delay A > delay B”) as the result of setting the count operation flag (TCExx) while the selected clock is high, the TMxx count value is incremented. An error of up to 1.5 clocks is generated.

Case when an error of up to 1.5 clocks is generated



Remark See Basic Timer Configuration above for details of the selected clock, TCE, clear signal, and count pulse.

(2) Restriction when an external event is selected for the timer count clock

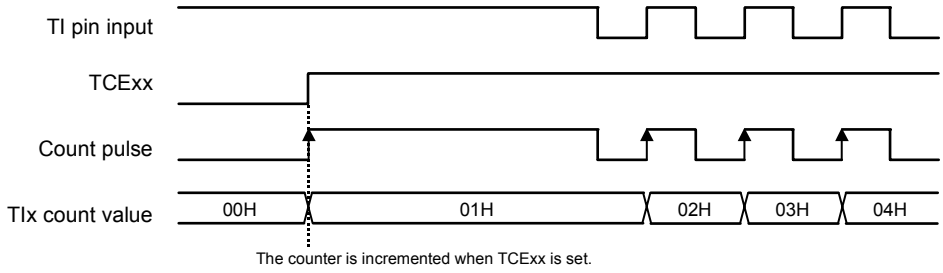
If an external event (TIx pin input) is selected for the timer count clock when the 8-bit timer/event counter is used, the count may be incremented after the count operation flag (TCExx) is set, depending on the status of the valid edge and TI pin.

[Details of restriction]

In the case of “delay A > delay B” as described in (1), the TMxx count value is incremented if any of the following conditions is satisfied.

- The count operation flag (TCExx) is set while the TI pin is high and the rising edge is selected.
- The count operation flag (TCExx) is set while the TI pin is low and the falling edge is selected.

Count Operation When Timer Is Started
While TI Pin Is High and Rising Edge Is Selected



[Workaround]

Make allowances for 1-count error in the counter, or implement one of workarounds (1) and (2) below.

Workaround (1)

- Always start the timer while the TI pin is low if the rising edge is selected.
- Always start the timer while the TI pin is high if the falling edge is selected.

Workaround (2)

- Save the count value upon timer start in the control register. When reading the count value, subtract this value from the count value saved in the control register and use the result as a true count value.