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μPD780862 Microcontrollers Technical Update		Document No.	ZBG-CC-06-0055	1/1
		Date issued	December 5, 2006	
		Issued by	1st Solution Group Multipurpose Microcomputer Systems Division 4th Systems Operations Unit NEC Electronics Corporation	
Related documents	μPD780862 Subseries User's Manual: U16418EJ3V0UD00	Notification classification	√	Usage condition
				Upgrade
				Document modification
				Other notification

1. Affected products

μPD780861, μPD780862

μPD78F0862, μPD78F0862A

2. Notification

The following item has been added. See attachment 5 for details.

When a reset input by the low-voltage detector (LVI) conflicts with write to the low-voltage detection register (LVIM) or low-voltage detection level selection register (LVIS), the write-enabled bits of the register may be set to 1.

3. Workaround

Do not write to the LVIM and LVIS registers after the LVI is set as a reset source. Make sure that bit 7 (LVION) of LVIM is 0 before writing to the LVIM or LVIS register. When setting both, set LVIS first. If LVION is 1, do not set LVIM and LVIS.

4. Modification schedule

The device will not be revised for this item, so please regard it as a caution on use.

5. Content listing

See attachment 1.

6. Document revision history

μPD780862 Microcontrollers Technical Update

Document Number	Date Issued	Description
SBG-DT-03-0007-E	Jan. 14, 2003	Newly created.
SBG-DT-03-0157-E	May 28, 2003	Addition of restriction (No. 2)
ZBG-CC-04-0019	October 4, 2004	Addition of restriction (No. 3)
ZBG-CC-04-0025	October 26, 2004	Change of document number
ZBG-CC-06-0055	December 5, 2006	Addition of usage condition (No. 4)

Usage Condition Updates in μPD780862 Microcontrollers

1. Product History

Mask ROM version

No.	Description	μPD780861, μPD780862
1	Restriction on SBF transmission using UART6	△
2	Restriction on 16-bit timer output	△
3	Restriction on oscillation stabilization time	△
4	Low-voltage detector (LVI) function	△

Flash memory version (sample)

No.	Description	μPD78F0862	μPD78F0862A
1	Restriction on SBF transmission using UART6	△	△
2	Restriction on 16-bit timer output	△	△
3	Restriction on oscillation stabilization time	△	△
4	Low-voltage detector (LVI) function	△	△

Remark The meaning of each symbol is as follows.

–: No relevant

○: Restriction already corrected

×: Restriction applies (correction is planned)

△: Restriction applies (correction is not planned)

3. Update Details

Item 1: See attachment 2.

Item 2: See attachment 3.

Item 3: See attachment 4.

Item 4: Item added in this edition. See attachment 5 for details.

No. 1 Restriction on SBF transmission using UART6

[Description]

If SyncBreakField transmission is performed when LIN operates as the master in UART6 supporting the LIN-bus, the following illegal operation may be performed.

(1) A SyncBreakField field length shorter than the set value is output.

(2) Illegal UART transmission may be performed before SyncBreakField transmission is performed

There is no problem when LIN operates as a slave with which SyncBreakField transmission is not performed and when UART6 is used as a UART function.

[Workaround]

Implement the following workaround by software.

Perform 13- to 20-bit low-level SyncBreakField transmission by adjusting the baud rate value of the normal UART transmit function.

Do not use the SyncBreakField transmission function. Specifically, do not set bit 5 (SBTT6) of asynchronous serial interface control register 6 (ASICL6) to 1.

<How to set>

Set the UART data length to 8 bits, parity to 0 parity or even parity and transmit 00H.

As a result, 10-bit low-level transmission (start bit (1 bit) + data (8 bits) + parity (1 bit)) can be performed. Adjust the baud rate value so that this 10-bit low level matches the target SyncBreakField length.

(Example) When conditions of the transmitted LIN are:

UART6 basic clock = 5 MHz ←This value is set by clock select register 6 (CKSR6)

Target baud rate value = 19200 [bps]

The value set to the baud rate generator control register (BRGC6) to implement the above baud rate value is 130. Therefore, the 13-bit SyncBreakField length is: 0.2 μs $\times$ 130 $\times$ 2 $\times$ 13 = **676 μs**

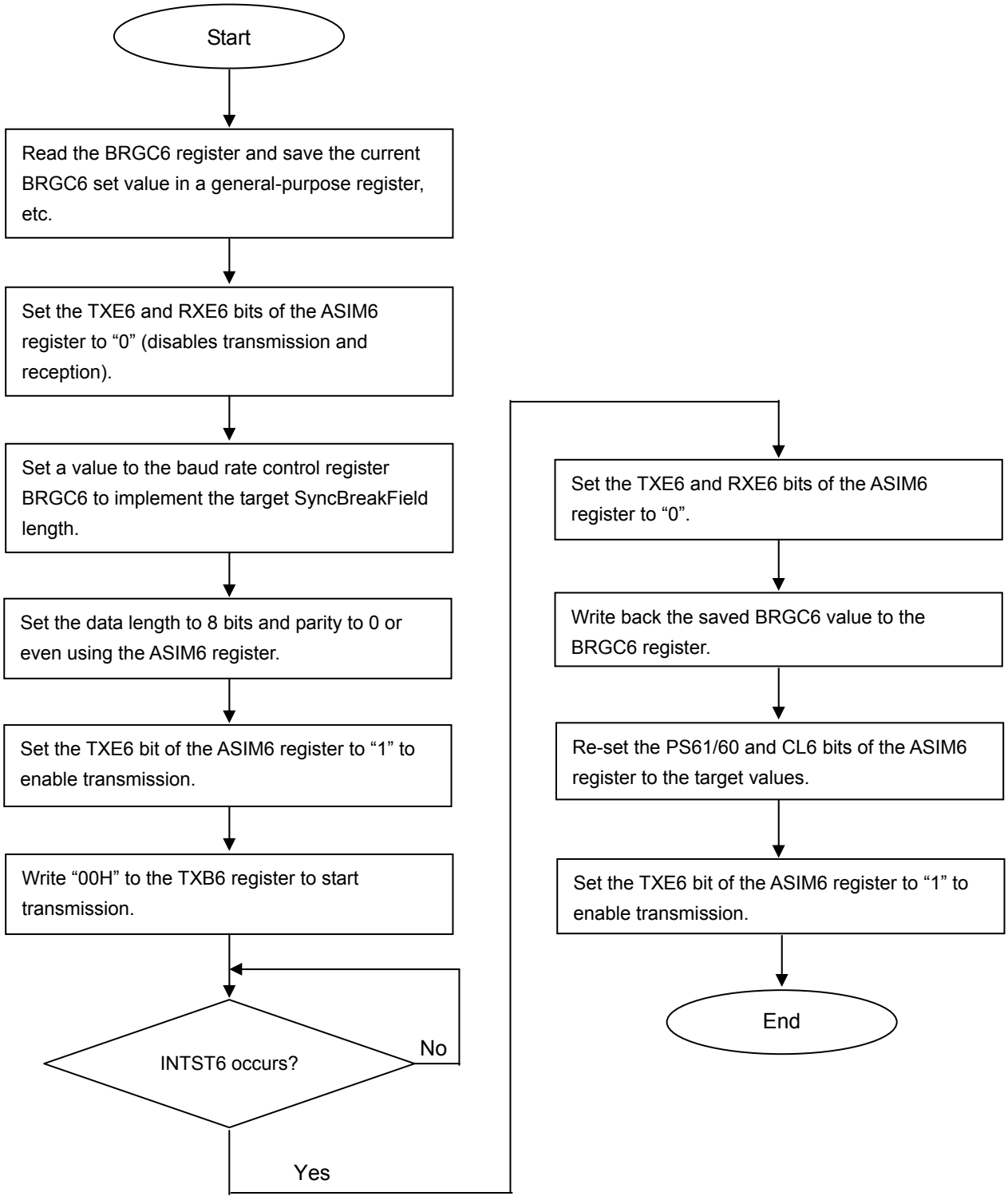
To implement this 13-bit field length in 10 bits, set a value 1.3 times the target baud rate to BRGC6. In this example, set BRGC6 to 169. The 10-bit low-level transmission length is: 0.2 μs $\times$ 169 $\times$ 2 $\times$ 10 = **676 μs**

Consequently, the value matches that of the 13-bit SyncBreakField length.

If the setting to the BRGC6 register is not sufficient for setting the bit, also select the UART6 basic clock.

The following shows the flowchart of the software setting procedure.

<Flowchart of software setting procedure>



[Modification]

Regard this item as a usage restriction. The user's manual and device file will be corrected.

<Details of correction in user's manual and device file>

Description of bits 2 to 5 related to the SyncBreakField transmit function of asynchronous serial interface control register 6 (ASICL6) will be deleted from the user's manual page 209. In addition, these bits are fixed to the initial values and writing to these bits is disabled.

The correction will be reflected in the device file.

[Before modification]

Address: FF58H After reset: 16H R/W

Note Bit 7 is read-only.

Symbol	7	6	5	4	3	2	1	0
ASICL6	SBRF6	SBRT6	SBTT6	SBL62	SBL61	SBL60	DIR6	TXDLV6

[After modification]

Address: FF58H After reset: 16H R/W**Note**

Note Bits 2 to 5 and 7 are read-only.

Symbol	7	6	5	4	3	2	1	0
ASICL6	SBRF6	SBRT6	0	1	0	1	DIR6	TXDLV6

In line with this correction, SBRT6 will be added to the assembler reserved words, and to the header file (sfrbit.h) in the C compiler.

No. 2 Restriction on 16-bit timer output

[Description]

When setting the timer output F/F status using 16-bit timer/event counter 00, the setting may not be performed correctly depending on the TOC00 (timer output control register) setting timing.

If LVS00 is set to 1 before setting TOE00, the LVS00 settings are invalid and a low level is output. If LVS00 and TOE00 are set to 1 simultaneously, the timer output is undefined.

<16-bit timer output control register format>

Symbol	7	6	5	4	3	2	1	0
TOC00	0	OSPT00	OSPE00	TOC004	LVS00	LVR00	TOC001	TOE00

LVS00	LVR00	Setting of timer output F/F
0	0	No change
0	1	Timer output F/F is reset (0)
1	0	Timer output F/F is set (1)
1	1	Setting prohibited

TOE00	Timer output control
0	Output disabled
1	Output enabled

[Workaround]

When setting LVS00 to 1 to output a high level from the timer, be sure to set TOE00 to 1 first to enable timer output, and then set LVS00 to 1. The following shows a program example.

<Program example>

```
                :
MOV     TOC00,#00000001B        ; 16-bit timer output enabled
MOV     TOC00,#00011011B        ; Other settings and timer output F/F are set to high level
                                  (Timer output level is set to high.)
                :
MOV     TMC00,#00001100B        ; Timer operation started
```

No. 3 Restriction on oscillation stabilization time

[Description]

When the OSTS register (oscillation stabilization time select register) is used with a specific setting other than the initial value and the main clock oscillation stabilization time is checked using the OSTC register (oscillation stabilization time counter status register), the correct value may not be read.

<Condition>

OSTC Operating Status	OSTS Value Setting	OSTS Value Change Pattern (OSTS Initial Value = 05H)	Whether or Not This Restriction Is Applicable
Count status after reset or standby release	OSTS value is not set (Initial value is used)	–	Not applicable
	OSTS value is set	05H (101) → 05H (101)	Not applicable
		05H (101) → 04H (100)	Not applicable
		05H (101) → 03H (011)	Applicable
		05H (101) → 02H (010)	Applicable
		05H (101) → 01H (001)	Not applicable
		Consult NEC Electronics in regards to change patterns other than above.	–
Other than above	–	–	Not applicable

[Workaround]

Do not use the OSTS register under the condition to which this restriction applies.

When using the OSTS register under the condition to which this restriction applies, check the oscillation stabilization time using the OSTC register before setting the OSTS register.

No. 4 Low-voltage detector (LVI) function

[Affected products]

μPD780862, μPD780862, μPD78F0862, μPD780862A

[Affected usage]

When the low-voltage detector (LVI) is used as a reset source

(This item does not affect operations when the LVI is not used, or when it is used as an interrupt source.)

[Description]

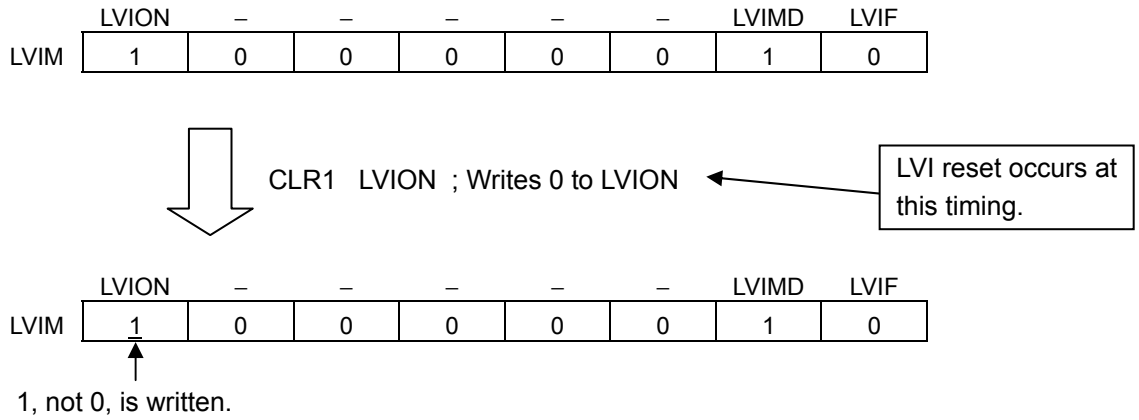
When a reset input by the low-voltage detector (LVI) conflicts with write to a register that sets the LVI operation (LVIM or LVIS), the write-enabled bits of the register may be set to 1. As a result, the following two phenomena occur.

- The reset by the LVI may not stop.
- The voltage detected by the LVI may be lower than the set value or the default value.

These phenomena do not occur in cases other than the LVI reset.

Figure 1 shows an example when these phenomena occur due to manipulation of the LVION flag.

Figure 1 When LVION Flag Value Is Changed from 1 to 0



In the case of LVIS, the default value (4.3 V ±0.2 V) is detected if bit 3 is set to 1.

[Cause]

The bus connected to LVIM and LVIS becomes High (“1”) after reset. In addition, the values of these registers are not cleared by an LVI reset, according to the specifications.

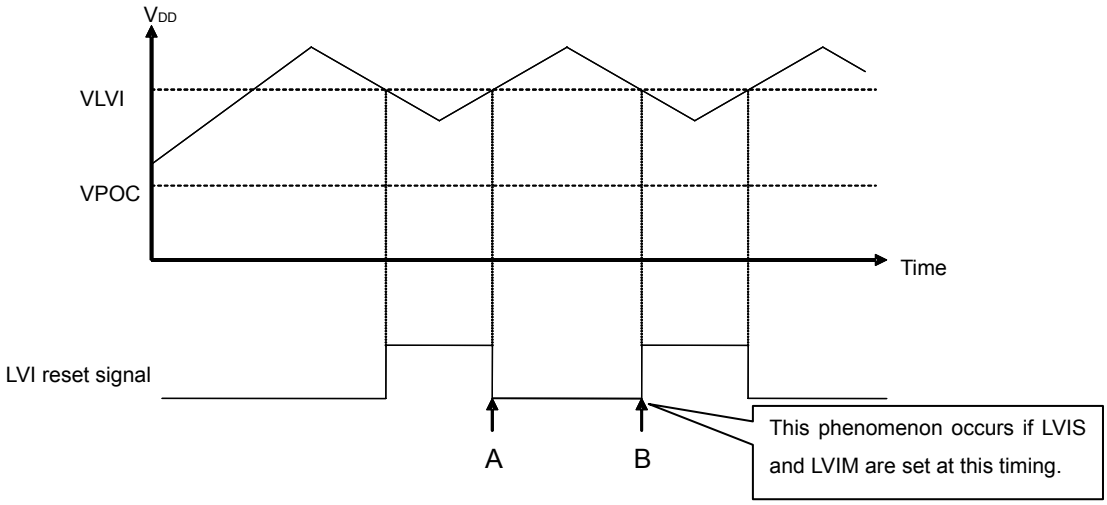
When a value is written to these registers, the CPU first sets the write value to the bus. This value is written to the target register when a write signal occurs. If the register is written when the internal bus is reset by an LVI reset, however, the reset value of the bus (1) may be written. This also applies to 1-bit manipulation instructions.

Registers other than LVIM and LVIS are not affected by this case.

[Occurrence example]

If the VDD voltage varies around the LVI detection voltage (VLVI), the LVI reset occurs several times. In programs in which LVIM and LVIS are always initialized after reset release, if the period from LVI reset release (A in Figure 2) until a LVI reset occurrence (B in Figure 2) matches the time from reset release until initial setting of LVIM and LVIS, this phenomenon occurs.

Figure 2 Example of Conflict Between LVI Reset and LVIM Register Write



[Workarounds]

Implement the following two software measures.

(1) Do not write to the LVIM and LVIS registers after the LVI is set as a reset source.

(2) Make sure that bit 7 (LVION) of LVIM is 0 before setting the LVIM or LVIS register. If LVION is 1, do not set LVIM and LVIS. By taking this measure, setting of LVIM and LVIS will be performed upon external reset input, POC reset, watchdog timer (WDT) reset or clock monitor (CLM) reset, but will not be performed upon LVI reset.

Because the reset control flag register (RESF) is not cleared by reset input from the LVI, WDT, or CLM according to the specifications, LVIRF, WDTRF and CLMRF may be set to 1. Whether the LVI reset has been input can be judged by checking LVIRF, but an additional instruction is required to judge if LVIM or LVIS has been cleared by WDT or CLM reset. Therefore, use LVION for workarounds of this case.