Microcomputer Technical Information

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μPD780344 Subseries μPD780354 Subseries μPD780344Y Subseries μPD780354Y Subseries Usage Restrictions		Document No.	SBG-DT-02-0027-E		1/1
		Date issued	December 11, 2002		
		Issued by	Microcomputer Group 2nd Solutions Division Solutions Operations Unit NEC Electronics Corporation		
Related documents	μPD780344, 780354, 780344Y, 780354Y Preliminary User's Manual (U15798EJ1V0UM00)	Notification classification	√	Usage restriction	
				Upgrade	
				Document modification	
				Other notification	

1. Affected products

μPD780343, 780344

μPD780353, 780354

μPD780343Y, 780344Y

μPD780353Y, 780354Y

μPD78F0354, 78F0354Y

2. List of restrictions

The restriction history and detailed information is described in Attachment 1.

List of Usage Restrictions in μPD780354, 780344, 780354Y, 780344Y Subseries Subseries

1. Product Version

- μPD780343, 780344: Rank k
- μPD780353, 780354: Rank K
- μPD780343Y, 780344Y: Rank K
- μPD780353Y, 780354Y: Rank K
- μPD78F0354, 78F0354Y: Rank K

* The rank is indicated by the fifth character from the left in the lot number marked on the package.

2. Product History

Description		μPD780343, 780344 μPD780353, 780354 μPD780343Y, 780344Y μPD780353Y, 780354Y μPD78F0354, 78F0354Y
	Rank	K
Item 1	Erroneous description on A/D converter	Δ

Notes 1. The rank is indicated by the fifth character from the left in the lot number marked on the package.

2. The meaning of each symbol is as follows.

–: Restriction does not apply

√: Restriction already corrected

×: Restriction applies (correction is planned)

Δ: Restriction applies (correction is not planned)

2. Details of Usage Restrictions

Item 1: Refer to Attachment 1 for details.

3. Cautions

None.

No.1 Erroneous description on A/D converter

[Description]

Erroneous descriptions on the A/D converter were found in the μPD780344, 780354, 780344Y, 780354Y Preliminary User's Manual. The correct descriptions are shown below.

(1) Correction of pin name

Incorrect: AV_{REF}

Correct: AV_{DD}

Remark Use the products with $AV_{DD} = V_{DD}$ regardless of whether the A/D converter is used or not.

(2) Correction of A/D converter specifications

(a) 8-bit A/D converter (T_A = –40 to +85°C, $AV_{DD} = V_{DD}$ = 2.2 to 5.5 V, $AV_{SS} = V_{SS}$ = 0 V)

Parameter	Symbol	Conditions	MIN.	TYP.	MAX.	Unit
Resolution			8	8	8	bit
Overall error Note		4.5 V ≤ AV_{DD} ≤ 5.5 V		±0.2	±0.4	%FSR
		2.7 V ≤ AV_{DD} < 4.5 V		±0.3	±0.6	%FSR
		2.2 V ≤ AV_{DD} < 2.7 V		±0.6	±1.2	%FSR
Conversion time	t_{CONV}	4.5 V ≤ AV_{DD} ≤ 5.5 V	14		100	ms
		2.7 V ≤ AV_{DD} < 4.5 V	19		100	ms
		2.2 V ≤ AV_{DD} < 2.7 V			100	ms
Analog input voltage	V_{IAN}		0		AV_{DD}	V
Resistance between AV_{REF} and AV_{SS}	R_{REF}	At A/D conversion operation	20	40		kΩ

Note Overall error excluding quantization error ±1/2 LSB). It is indicated as a ratio (%FSR) to the full-scale value.

(b) 10-bit A/D converter (T_A = –40 to +85°C, $AV_{DD} = V_{DD}$ = 2.2 to 5.5 V, $AV_{SS} = V_{SS}$ = 0 V)

Parameter	Symbol	Conditions	MIN.	TYP.	MAX.	Unit
Resolution			10	10	10	Bit
Overall error Note		4.5 V ≤ AV_{DD} ≤ 5.5 V		±0.2	±0.4	%FSR
		2.7 V ≤ AV_{DD} < 4.5 V		±0.3	±0.6	%FSR
		2.2 V ≤ AV_{DD} < 2.7 V		±0.6	±1.2	%FSR
Conversion time	t_{CONV}	4.5 V ≤ AV_{DD} ≤ 5.5 V	14		100	ms
		2.7 V ≤ AV_{DD} < 4.5 V	19		100	ms
		2.2 V ≤ AV_{DD} < 2.7 V	28		100	ms
Zero-scale error Note		4.5 V ≤ AV_{DD} ≤ 5.5 V			±0.4	%FSR
		2.7 V ≤ AV_{DD} < 4.5 V			±0.6	%FSR
		2.2 V ≤ AV_{DD} < 2.7 V			±1.2	%FSR
Full-scale error Note		4.5 V ≤ AV_{DD} ≤ 5.5 V			±0.4	%FSR
		2.7 V ≤ AV_{DD} < 4.5 V			±0.6	%FSR
		2.2 V ≤ AV_{DD} < 2.7 V			±1.2	%FSR
Integral linearity error Note		4.5 V ≤ AV_{DD} ≤ 5.5 V			±2.5	LSB
		2.7 V ≤ AV_{DD} < 4.5 V			±4.5	LSB
		2.2 V ≤ AV_{DD} < 2.7 V			±8.5	LSB
Integral linearity error		4.5 V ≤ AV_{DD} ≤ 5.5 V			±1.5	LSB
		2.7 V ≤ AV_{DD} < 4.5 V			±2.0	LSB
		2.2 V ≤ AV_{DD} < 2.7 V			±3.5	LSB
Analog input impedance		Sampling			100	kΩ
		Non-sampling		10		kΩ
Analog input voltage	V_{IAN}		0		AV_{DD}	V
Resistance between AV_{REF} and AV_{SS}	R_{REF}	At A/D conversion operation	20	40		kΩ

Note Overall error excluding quantization error ±1/2 LSB). It is indicated as a ratio (%FSR) to the full-scale value.