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# RENESAS TECHNICAL UPDATE

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| Product Category | MPU/MCU | | Document No. | TN-SH7-A806A/E | Rev. | 1.00 |
|---|---|---|---|---|---|---|
| Title | Treatment of Unused Pins of SH7786 | | Information Category | Technical Notification | | |
| Applicable Product | SH7786 Group | Lot No.<br>All lots | Reference Document | SH7786 Group User's Manual: Hardware<br>Rev.1.00 Nov. 30, 2010<br>(REJ09B0501-0100) | | |

Description of the handling of unused pins is newly added to SH7786 Group Hardware User's Manual as follows.

[Description]

Table 1 Treatment of Unused Pins

#: Low active or inverted-signal of differential signal-pair

| Pin Name (LSI level) | Signal Name (Module level) | Module | I/O | When Not in Use |
|---|---|---|---|---|
| A[25:0] | A[25:0] | LBSC | O | Open[*1] |
| D[31:8] | D[31:8] | LBSC | IO | Open |
| D[7:0]/FD[7:0] | D[7:0] (default) | LBSC | IO | Must be used |
| | FD[7:0] | FLCTL | IO | |
| CS0# | CS0# | LBSC | O | Must be used |
| CS1#/A26 | CS1#/A26 | LBSC | O | Open |
| CS[6:2]# | CS[6:2]# | LBSC | O | Open |
| RD#/FRAME#/FRE# | RD#/FRAME# | LBSC | O | Open |
| | FRE# | FLCTL | O | |
| R/W# | R/W# | LBSC | O | Open |
| BS# | BS# | LBSC | O | Open |
| RDY# | RDY# | LBSC | I | Pulled-down to VSS |
| WE0#/REG# | WE0#/REG# | LBSC | O | Open |
| WE1#/FWE# | WE1#/FWE# | LBSC | O | Open |
| | FWE# | FLCTL | O | |
| WE2#/IORD# | WE2#/IORD# | LBSC | O | Open |
| WE3#/IOWR# | WE3#/IOWR# | LBSC | O | Open |
| CLKOUTENB | CLKOUTENB | CPG | O | Open |
| CLKOUT | CLKOUT | CPG | O | Open |
| PRESET# | PRESET# | RESET | I | Must be used |
| NMI | NMI | INTC | I | Pulled-up to VCCQ |
| IRL[3:0]# | IRL[3:0]# | INTC | I | Pulled-up to VCCQ |
| DR0/ETH_TXD0 | Port A0 (default) | GPIO | IO | Open |
| | DR0 | DU | O | |
| | ETH_TXD0 | Ether | O | |

| Pin Name (LSI level) | Signal Name (Module level) | Module | I/O | When Not in Use |
|---|---|---|---|---|
| DR1/ETH_TXD1 | Port A1 (default) | GPIO | IO | |
| | DR1 | DU | O | Open |
| | ETH_TXD1 | Ether | O | |
| DR2/ETH_TXD2 | Port A2 (default) | GPIO | IO | |
| | DR2 | DU | O | Open |
| | ETH_TXD2 | Ether | O | |
| DR3/ETH_TXD3 | Port A3 (default) | GPIO | IO | |
| | DR3 | DU | O | Open |
| | ETH_TXD3 | Ether | O | |
| DR4/ETH_TX_EN | Port A4 (default) | GPIO | IO | |
| | DR4 | DU | O | Open |
| | ETH_TX_EN | Ether | O | |
| DR5/ETH_TX_ER | Port A5 (default) | GPIO | IO | |
| | DR5 | DU | O | Open |
| | ETH_TX_ER | Ether | O | |
| DISP/ETH_LINK | Port A6 (default) | GPIO | IO | |
| | DISP | DU | O | Open |
| | ETH_LINK | Ether | I | |
| CDE/ETH_MAGIC | Port A7 (default) | GPIO | IO | |
| | CDE | DU | O | Open |
| | ETH_MAGIC | Ether | O | |
| DG0/ETH_CRS | Port B0 (default) | GPIO | IO | |
| | DG0 | DU | O | Open |
| | ETH_CRS | Ether | I | |
| DG1/ETH_TX_CLK | Port B1 (default) | GPIO | IO | |
| | DG1 | DU | O | Open |
| | ETH_TX_CLK | Ether | I | |
| DG2/ETH_COL | Port B2 (default) | GPIO | IO | |
| | DG2 | DU | O | Open |
| | ETH_COL | Ether | I | |
| DG3/ETH_MDC | Port B3 (default) | GPIO | IO | |
| | DG3 | DU | O | Open |
| | ETH_MDC | Ether | O | |
| DG4/ETH_RX_CLK | Port B4 (default) | GPIO | IO | |
| | DG4 | DU | O | Open |
| | ETH_RX_CLK | Ether | I | |
| DG5/ETH_MDIO | Port B5 (default) | GPIO | IO | |
| | DG5 | DU | O | Open |
| | ETH_MDIO | Ether | IO | |
| ODDF/HSPI_CS# | Port B6 (default) | GPIO | IO | |
| | ODDF | DU | IO | Open |
| | HSPI_CS# | HSPI | IO | |
| VSYNC#/HSPI_CLK | Port B7 (default) | GPIO | IO | |
| | VSYNC# | DU | IO | Open |
| | HSPI_CLK | HSPI | IO | |
| DB0/ETH_RX_ER | Port C0 (default) | GPIO | IO | |
| | DB0 | DU | O | Open |
| | ETH_RX_ER | Ether | I | |

| Pin Name (LSI level) | Signal Name (Module level) | Module | I/O | When Not in Use |
|---|---|---|---|---|
| DB1/ETH_RX_DV | Port C1 (default) | GPIO | IO | Open |
| | DB1 | DU | O | |
| | ETH_RX_DV | Ether | I | |
| DB2/ETH_RXD0 | Port C2 (default) | GPIO | IO | Open |
| | DB2 | DU | O | |
| | ETH_RXD0 | Ether | I | |
| DB3/ETH_RXD1 | Port C3 (default) | GPIO | IO | Open |
| | DB3 | DU | O | |
| | ETH_RXD1 | Ether | I | |
| DB4/ETH_RXD2 | Port C4 (default) | GPIO | IO | Open |
| | DB4 | DU | O | |
| | ETH_RXD2 | Ether | I | |
| DB5/ETH_RXD3 | Port C5 (default) | GPIO | IO | Open |
| | DB5 | DU | O | |
| | ETH_RXD3 | Ether | I | |
| HSYNC#/HSPI_TX | Port C6 (default) | GPIO | IO | Open |
| | HSYNC# | DU | IO | |
| | HSPI_TX | HSPI | O | |
| DCLKIN/HSPI_RX | Port C7 (default) | GPIO | IO | Open |
| | DCLKIN | DU | I | |
| | HSPI_RX | HSPI | I | |
| DREQ0#/USB_OVC0 | Port D0 | GPIO | IO | Open |
| | DREQ0# | DMAC | I | |
| | USB_OVC0 (default) | USB | I | |
| DREQ1#/BREQ#/USB_OVC1 | Port D1 | GPIO | IO | Open |
| | DREQ1# | DMAC | I | |
| | BREQ# | LBSC | I | |
| | USB_OVC1 (default) | USB | I | |
| DACK0#/FCLE | Port D2 | GPIO | IO | Open |
| | DACK0# | DMAC | O | |
| | FCLE (default) | FLCTL | O | |
| DACK1#/BACK#/FALE | Port D3 | GPIO | IO | Open |
| | DACK1# | DMAC | O | |
| | BACK# | LBSC | O | |
| | FALE (default) | FLCTL | O | |
| SCIF1_TXD | Port D4 (default) | GPIO | IO | Open |
| | SCIF1_TXD | SCIF | O | |
| SCIF1_RXD | Port D5 (default) | GPIO | IO | Open |
| | SCIF1_RXD | SCIF | I | |
| SCIF1_SCK | Port D6 (default) | GPIO | IO | Open |
| | SCIF1_SCK | SCIF | IO | |
| DCLKOUT | Port D7 (default) | GPIO | IO | Open |
| | DCLKOUT | DU | O | |
| USB_PENC0 | Port E6 | GPIO | IO | Open |
| | USB_PENC0 (default) | USB | O | |
| USB_PENC1 | Port E7 | GPIO | IO | Open |
| | USB_PENC1 (default) | USB | O | |

| Pin Name (LSI level) | Signal Name (Module level) | Module | I/O | When Not in Use |
|---|---|---|---|---|
| HAC0_BITCLK/SSI0_CLK/SDIF1D0 | Port F0 (default) | GPIO | IO | Open |
| | HAC0_BITCLK | HAC | I | |
| | SSI0_CLK | SSI | I | |
| | SDIF1D0 | SDIF | IO | |
| HAC0_SYNC/SSI0_WS/SDIF1D1 | Port F1 (default) | GPIO | IO | Open |
| | HAC0_SYNC | HAC | O | |
| | SSI0_WS | SSI | IO | |
| | SDIF1D1 | SDIF | IO | |
| HAC0_SDIN/SSI0_SCK/SDIF1D2 | Port F2 (default) | GPIO | IO | Open |
| | HAC0_SDIN | HAC | I | |
| | SSI0_SCK | SSI | IO | |
| | SDIF1D2 | SDIF | IO | |
| HAC0_SDOUT/SSI0_SDATA/SDIF1D3 | Port F3 (default) | GPIO | IO | Open |
| | HAC0_SDOUT | HAC | O | |
| | SSI0_SDATA | SSI | IO | |
| | SDIF1D3 | SDIF | IO | |
| HAC1_BITCLK/SSI1_CLK/SDIF1CLK | Port F4 (default) | GPIO | IO | Open |
| | HAC1_BITCLK | HAC | I | |
| | SSI1_CLK | SSI | I | |
| | SDIF1CLK | SDIF | O | |
| HAC1_SYNC/SSI1_WS/SDIF1WP | Port F5 (default) | GPIO | IO | Open |
| | HAC1_SYNC | HAC | O | |
| | SSI1_WS | SSI | IO | |
| | SDIF1WP | SDIF | I | |
| HAC1_SDIN/SSI1_SCK/SDIF1CD# | Port F6 (default) | GPIO | IO | Open |
| | HAC1_SDIN | HAC | I | |
| | SSI1_SCK | SSI | IO | |
| | SDIF1CD# | SDIF | I | |
| HAC1_SDOUT/SSI1_SDATA/SDIF1CMD | Port F7 (default) | GPIO | IO | Open |
| | HAC1_SDOUT | HAC | O | |
| | SSI1_SDATA | SSI | IO | |
| | SDIF1CMD | SDIF | IO | |
| SCIF3_TXD/HAC_RES#/SSI2_WS | Port G5 (default) | GPIO | IO | Open |
| | SCIF3_TXD | SCIF | O | |
| | HAC_RES# | HAC | O | |
| | SSI2_WS | SSI | IO | |
| SCIF3_RXD/TCLK/SSI2_SCK | Port G6 (default) | GPIO | IO | Open |
| | SCIF3_RXD | SCIF | I | |
| | TCLK | TMU | I | |
| | SSI2_SCK | SSI | IO | |
| SCIF3_SCK/SSI2_SDATA | Port G7 (default) | GPIO | IO | Open |
| | SCIF3_SCK | SCIF | IO | |
| | SSI2_SDATA | SSI | IO | |
| MODE0/SCIF0_TXD/IRL4#/SDIF0D0 | MODE0 (power-on reset) | RESET | I | Must be used during power-on reset |
| | Port H0 (default) | GPIO | IO | Open |
| | SCIF0_TXD | SCIF | O | |
| | IRL4# | INTC | I | |
| | SDIF0D0 | SDIF | IO | |

| Pin Name (LSI level) | Signal Name (Module level) | Module | I/O | When Not in Use |
|---|---|---|---|---|
| MODE1/SCIF0_RXD/IRL5#/SDIF0D1 | MODE1 (power-on reset) | RESET | I | Must be used during power-on reset |
| | Port H1 (default) | GPIO | IO | Open |
| | SCIF0_RXD | SCIF | I | |
| | IRL5# | INTC | I | |
| | SDIF0D1 | SDIF | IO | |
| MODE2/SCIF0_SCK/IRL6#/SDIF0D2 | MODE2 (power-on reset) | RESET | I | Must be used during power-on reset |
| | Port H2 (default) | GPIO | IO | Open |
| | SCIF0_SCK | SCIF | IO | |
| | IRL6# | INTC | I | |
| | SDIF0D2 | SDIF | IO | |
| MODE3/SCIF0_RTS#/IRL7#/SDIF0D3 | MODE3 (power-on reset) | RESET | I | Must be used during power-on reset |
| | Port H3 (default) | GPIO | IO | Open |
| | SCIF0_RTS# | SCIF | IO | |
| | IRL7# | INTC | I | |
| | SDIF0D3 | SDIF | IO | |
| MODE4/SCIF0_CTS#/DREQ2#/SDIF 0CLK | MODE4 (power-on reset) | RESET | I | Must be used during power-on reset |
| | Port H4 (default) | GPIO | IO | Open |
| | SCIF0_CTS# | SCIF | IO | |
| | DREQ2# | DMAC | I | |
| | SDIF0CLK | SDIF | O | |
| MODE5/DREQ3#/SDIF0WP | MODE5 (power-on reset) | RESET | I | Must be used during power-on reset |
| | Port H5 (default) | GPIO | IO | Open |
| | DREQ3# | DMAC | I | |
| | SDIF0WP | SDIF | I | |
| MODE6/DACK2#/SDIF0CD# | MODE6 (power-on reset) | RESET | I | Must be used during power-on reset |
| | Port H6 (default) | GPIO | IO | Open |
| | DACK2# | DMAC | O | |
| | SDIF0CD# | SDIF | I | |
| MODE7/DACK3#/SDIF0CMD | MODE7 (power-on reset) | RESET | I | Must be used during power-on reset |
| | Port H7 (default) | GPIO | IO | Open |
| | DACK3# | DMAC | O | |
| | SDIF0CMD | SDIF | IO | |
| MODE8/SCIF4_TXD/DRAK0#/SSI3_S CK/FSE# | MODE8 (power-on reset) | RESET | I | Must be used during power-on reset |
| | Port J1 (default) | GPIO | IO | Open |
| | SCIF4_TXD | SCIF | O | |
| | DRAK0# | DMAC | O | |
| | SSI3_SCK | SSI | IO | |
| | FSE# | FLCTL | O | |
| MODE9/SCIF4_RXD/DRAK1#/SSI3_ SDATA | MODE9 (power-on reset) | RESET | I | Must be used during power-on reset |
| | Port J2 | GPIO | IO | Open |
| | SCIF4_RXD | SCIF | I | |
| | DRAK1# | DMAC | O | |
| | SSI3_SDATA | SSI | IO | |

| Pin Name (LSI level) | Signal Name (Module level) | Module | I/O | When Not in Use |
|---|---|---|---|---|
| MODE10/SCIF4_SCK/DRAK2#/SSI3_WS | MODE10 (power-on reset) | RESET | I | Must be used during power-on reset |
| | Port J3 (default) | GPIO | IO | Open |
| | SCIF4_SCK | SCIF | IO | |
| | DRAK2# | DMAC | O | |
| | SSI3_WS | SSI | IO | |
| MODE11/DRAK3#/CE2A# | MODE11 (power-on reset) | RESET | I | Must be used during power-on reset |
| | Port J4 (default) | GPIO | IO | Open |
| | DRAK3# | DMAC | O | |
| | CE2A# | LBSC | O | |
| MODE12/SCIF5_TXD/CE2B# | MODE12 (power-on reset) | RESET | I | Must be used during power-on reset |
| | Port J5 (default) | GPIO | IO | Open |
| | SCIF5_TXD | SCIF | O | |
| | CE2B# | LBSC | O | |
| MODE13/SCIF5_RXD/IOIS16# | MODE13 (power-on reset) | RESET | I | Must be used during power-on reset |
| | Port J6 (default) | GPIO | IO | Open |
| | SCIF5_RXD | SCIF | I | |
| | IOIS16# | LBSC | I | |
| MODE14/SCIF5_SCK/FRB# | MODE14 (power-on reset) | RESET | I | Must be used during power-on reset |
| | Port J7 (default) | GPIO | IO | Open |
| | SCIF5_SCK | SCIF | IO | |
| | FRB# | FLCTL | I | |
| I2C_SCL0/SCIF2_RXD | I2C_SCL0 (default) | I2C | IO | Open |
| | SCIF2_RXD | SCIF | I | |
| I2C_SDA0/SCIF2_TXD | I2C_SDA0 (default) | I2C | IO | Open |
| | SCIF2_TXD | SCIF | O | |
| I2C_SCL1/SCIF2_SCK | I2C_SCL1 (default) | I2C | IO | Open |
| | SCIF2_SCK | SCIF | IO | |
| I2C_SDA1/IRQOUT# | I2C_SDA1 (default) | I2C | IO | Open |
| | IRQOUT# | RESET | O | |
| STATUS0/SSI2_CLK | STATUS0 | RESET | O | Open |
| | SSI2_CLK | SSI | I | |
| STATUS1/SSI3_CLK | STATUS1 | RESET | O | Open |
| | SSI3_CLK | SSI | I | |
| EXTAL | EXTAL | CPG | I | Must be used |
| XTAL | XTAL | CPG | O | Open |
| USB_EXTAL | USB_EXTAL | USB | I | Pulled-up to VCCQ |
| USB_XTAL | USB_XTAL | USB | O | Open |
| MPMD | MPMD | H-UDI | I | Must be used |
| ASEBRK#/BRKACK | ASEBRK#/BRKACK | H-UDI | IO | Open |
| TRST# | TRST# | H-UDI | I | Pulled-down to VSS or connect to PRESET# |
| TDO | TDO | H-UDI | O | Open |
| TDI | TDI | H-UDI | I | Open |
| TMS | TMS | H-UDI | I | Open |
| TCK | TCK | H-UDI | I | Open |

| Pin Name (LSI level) | Signal Name (Module level) | Module | I/O | When Not in Use |
|---|---|---|---|---|
| AUDCK | AUDCK | H-UDI | O | Open |
| AUDSYNC | AUDSYNC | H-UDI | O | Open |
| AUDATA[3:0] | AUDATA[3:0] | H-UDI | O | Open |
| MBA[2:0] | MBA[2:0] | DBSC3 | O | Open |
| MA[15:0] | MA[15:0] | DBSC3 | O | Open |
| MDQ[31:0] | MDQ[31:0] | DBSC3 | IO | Open |
| MDM[3:0] | MDM[3:0] | DBSC3 | O | Open |
| MDQS[3:0] | MDQS[3:0] | DBSC3 | IO | Open |
| MDQS[3:0]# | MDQS[3:0]# | DBSC3 | IO | Open |
| MCS[1:0]# | MCS[1:0]# | DBSC3 | O | Open |
| MRAS# | MRAS# | DBSC3 | O | Open |
| MCAS# | MCAS# | DBSC3 | O | Open |
| MWE# | MWE# | DBSC3 | O | Open |
| MCKE[1:0] | MCKE[1:0] | DBSC3 | O | Open |
| MODT[1:0] | MODT[1:0] | DBSC3 | O | Open |
| MCK[1:0] | MCK[1:0] | DBSC3 | O | Open |
| MCK[1:0]# | MCK[1:0]# | DBSC3 | O | Open |
| MRESET# | MRESET# | DBSC3 | O | Open |
| SDBUP | SDBUP | DBSC3 | I | Pulled-up to VCCQ-DDR15 |
| MBKPRST# | MBKPRST# | DBSC3 | I | Pulled-up to VCCQ-DDR15 |
| MVREF[1:0] | MVREF[1:0] | DBSC3 | - | Pulled-down to VSS |
| MZQ | MZQ | DBSC3 | - | Pulled-down to VSS |
| USB_DP0 | USB_DP0 | USB | IO | Open |
| USB_DM0 | USB_DM0 | USB | IO | Open |
| USB_OVC0 | USB_OVC0 | USB | I | Open |
| USB_DP1 | USB_DP1 | USB | IO | Open |
| USB_DM1 | USB_DM1 | USB | IO | Open |
| USB_VBUS1_OVC1 | USB_VBUS1_OVC1 | USB | I | Open |
| USB_REXT | USB_REXT | USB | - | Pulled-down to VSS |
| PCIE_RX1_0# | PCIE_RX1# | PCIEC | I | Open |
| PCIE_RX1_0 | PCIE_RX1 | PCIEC | I | Open |
| PCIE_TX1_0# | PCIE_TX1# | PCIEC | O | Open |
| PCIE_TX1_0 | PCIE_TX1 | PCIEC | O | Open |
| PCIE_RX0_[3:0]# | PCIE_RX0_[3:0]# | PCIEC | I | Open |
| PCIE_RX0_[3:0] | PCIE_RX0_[3:0] | PCIEC | I | Open |
| PCIE_TX0_[3:0]# | PCIE_TX0_[3:0]# | PCIEC | O | Open |
| PCIE_TX0_[3:0] | PCIE_TX0_[3:0] | PCIEC | O | Open |
| GCLK | GCLK | PCIEC | I | Open |
| GCLK# | GCLK# | PCIEC | I | Open |
| VTHREF | PA_VTHREF | Thermal sensor | O | Open |
| VTHSENSE | PA_VTHSENSE | Thermal sensor | O | Open |

[Note] Handling of the some unused pin which belongs to the enable module should be followed the description of the module manual. If there is no description for unused pins in the module manual, follow the above table for handling of unused pins.

*1: “Must be used” for the minimum number of pins that is necessary for the SH7786 system operation.

- End of text -