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MESC TECHNICAL NEWS

No. M7700-52-9909

Notes on Using PLP and PUL Instructions in 7900 Series MCUs

Please take note of the following problem in using the **PLP** and **PUL** instructions in the 7900 Series MCUs

1. Products Concerned

All of the 7900 Series MCUs

2. Problem

When the interrupt disable flag (flag I) = "0" (interrupt enabled) and one of the following two conditions is satisfied, the interrupt request bit of a maskable interrupt, which is requested immediately before the **PLP** or **PUL** instruction execution, may be cleared in error. (This will result in the interrupt being not generated.)

[Conditions]

- (1) The processor interrupt priority level (IPL) of the processor status register is changed to a higher one, by executing the **PLP** or **PUL** instruction. Also, this new IPL is the same as or higher than the level specified by the interrupt priority select bits of the interrupt control register.
- (2) The status of flag I is changed from "0" (enabled) to "1" (disabled) by executing the **PLP** or **PUL** instruction.

3. Workaround

Execute the **PLP** or **PUL** instruction with flag I = "1".

Moreover, note that flag I must be set to "1" by executing the **SEI** instruction. (Refer to "**Technical News No. M7700-45-9906 Notes on Programming in 7900 Series MCUs**").