To our customers,

Old Company Name in Catalogs and Other Documents

On April 1st, 2010, NEC Electronics Corporation merged with Renesas Technology Corporation, and Renesas Electronics Corporation took over all the business of both companies. Therefore, although the old company name remains in this document, it is a valid Renesas Electronics document. We appreciate your understanding.

Renesas Electronics website: http://www.renesas.com

April 1st, 2010
Renesas Electronics Corporation

Issued by: Renesas Electronics Corporation (http://www.renesas.com)

Send any inquiries to http://www.renesas.com/inquiry.

GRADE A

RENESAS TECHNICAL NEWS

No.ASSP-13-0309

M66291 IN-Direction DMA Transfer Limitations

Classification	Concerned Products
Corrections and supplementary explanation of document √ Notes Knowhow Others	USB ASSP M66291GP/M66291HP

1. Phenomenon

In a system that uses D0_FIFO or D1_FIFO (Dn_FIFO hereon) for DMA transfers to an endpoint set to the IN-direction (IN-endpoint), if the DMA disable process (write DMAEN = "0") is executed after DMA transfer is complete, a zero-length (Null) packet may be output in response to the IN Token in the endpoint on the USB bus.

2. Occurring Conditions

This phenomenon does not occur in systems that do not perform DMA transfers to IN endpoints.

The phenomenon described above may occur when all of the following conditions are present (see Diagram 1):

Condition 1: The endpoint designated to the Dn_FIFO is set to the IN direction

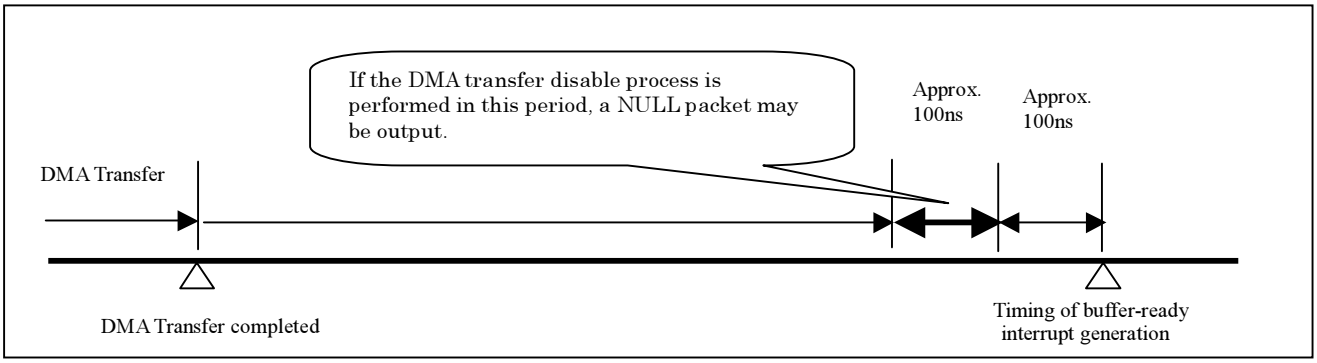
Condition 2: In the DMA transfer under Condition 1, the DMA transfer disable process (write DMAEN = "0") is executed after transfer completion.

Condition 3: The DMA transfer disable process (Condition 2) is performed immediately before (approx. –200ns to –100ns) the timing of the endpoint buffer-ready interrupt occurs.

*When this phenomenon occurs, the buffer-ready interrupt will not actually occur.

*This phenomenon does not occur when the DMA transfer disable process is executed after the buffer-ready interrupt is generated.

Figure 1. Occurring Conditions



3. Solutions

Either of the following solutions can be used to work around this phenomenon.

(1) After transfer is complete, perform the DMA transfer disable process after the buffer-ready interrupt of the endpoint has been generated.

(2) Disable DMA transfer (DMAEN = "0") using the following 2 processes in the order indicated.

1). Write the following settings to the Dn_FIFO Select Register
DMA transfer enable (DMAEN = "1") and designated endpoint clear (DMA_EP = "0000")

2). Write the following settings to the Dn_FIFO Select Register
DMA transfer disable (DMAEN = "0") and designated endpoint set (DMA_EP = "0000").

4. Non-Occurring Conditions

This phenomenon will not occur under the following conditions. Please use this information to determine whether or not your system may be affected by this phenomenon.

(1) When the endpoint is set to single-buffer

The size of the DMA transfer affects whether or not the phenomenon will occur.

-The phenomenon will not occur when the size of the transfer fits description #4 below under Condition A or B.

-The phenomenon will not occur when the size of the transfer fits description #5 below under Condition C, D or E.

#4 When the DMA transfer size is multiples of the FIFO buffer size, and

A.after DMA transfer is complete, the DMA transfer disable process is executed after the buffer-ready interrupt of the endpoint has been generated, or

B.after the last of the DMA transfer data is written, the DMA transfer disable process is executed within the [Non-Occurring Periods] indicated in List 1.

#5 When the DMA transfer size is different than the FIFO buffer size (including short packet) and

C.after DMA transfer is complete, the DMA transfer disable process is executed and then the IN-buffer write complete process (write IVAL = "1") is executed, or

D.after DMA transfer is complete, the DMA transfer disable process is executed within 7us after the IN-buffer write process is executed, or

E.after DMA transfer is complete, the IN-buffer write process is executed, the buffer-ready interrupt is generated to the corresponding endpoint, and then the DMA transfer disable process is executed.

(2) When the endpoint is set to double-buffer

The size of the DMA transfer affects whether or not the phenomenon will occur.

When the DMA transfer size is as described in #6 below, the phenomenon will not occur under Condition F or G.

When the DMA transfer size fits the description in #7 below, the phenomenon will not occur under Condition H, I or J.

#6 When the DMA transfer size is multiples of the FIFO buffer size, and

F.after DMA transfer is completed, the buffer-ready interrupt is generated to the endpoint, and then the DMA transfer disable process is executed, or

G.during DMA transfer, the endpoint buffer-ready interrupt is generated when the [DMA transfer size – FIFO buffer size] is written, and then the DMA transfer disable process is executed within the [Non-Occurring Periods] shown in Table 1.

#7 When DMA transfer size is the different than the FIFO buffer size (including short packet), and

H.after DMA transfer is complete, the DMA transfer disable process is executed and then the IN-buffer write process (write IVAL = "1") is executed, or

I.during DMA transfer, the endpoint buffer-ready interrupt is generated when the [DMA transfer size – FIFO buffer size] is written, and then the DMA transfer disable process is executed within a [Non-Occurring Period] shown in Table 1, or

J.after DMA transfer is complete, the IN-buffer write process is executed, and then the DMA transfer disable process is executed after the endpoint buffer ready interrupt is generated.

Table 1. Non-Occurring Periods

(Periods for DMA Transfer (IN) that will not trigger a NULL packet)

NO	Corresponding Endpoint FIFO Buffer Size(bytes)	Non-Occurring Periods (us)
1	64	49.6
2	128	99.2
3	192	148.9
4	256	198.5
5	320	248.1
6	384	297.8
7	448	347.4
8	512	397.0
9	576	446.7
10	640	496.3
11	704	545.9
12	768	595.6
13	832	645.2
14	896	694.8
15	960	744.5
16	1024	794.1

[Supplement] Table 1 shows the shortest period (logic value) for sending data (FIFO buffer size) to the Host. If data is sent within the indicated periods, the FIFO buffer on the SIE-side will go to the "now transferring" status and the buffer-ready interrupt will not be generated.