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Additional Information Concerning Three-phase Waveform Mode of 7754/53 Group

This document contains additional information concerning the three-phase motor drive waveform output mode (three-phase waveform mode). This information is critical for system development using the three-phase waveform mode in the 7754/53 groups. (Please note that the term "group" will be eliminated in the following explanations. Ex: "7754" indicates "7754 group".)

1. Corrected name and function for "Valid Output Polarity Select Bit for Interrupt Request" (three-phase mode 1)

Please make corrections (1) and (2) to the following datasheets of 7754 and 7753 (PDF File, Rev. 1.01 and before):

- M37754M8C-XXXGP, M37754M8C-XXXHP, M37754S4CGP, M37754S4CHP
- M37753M8C-XXXFP, M37753M8C-XXXHP, M37753S4CFP, M37753S4CHP

[Corrections]

(1) Bit function in three-phase mode 1

0: Timer B2 interrupt request generated at each even-numbered underflow of timer B2

1: Timer B2 interrupt request generated at each odd-numbered underflow of timer B2

(2) Bit name in three-phase mode 1

The bit name has been changed to properly indicate the bit function.

New name: Interrupt Validity Output Select Bit (*7754/53: Bit 1 of address 1C₁₆)

Note: The corrected datasheets (PDF file, Rev. 2.00) will be released at the end of Apr. 1999.

2. Three-phase mode 1 start operation

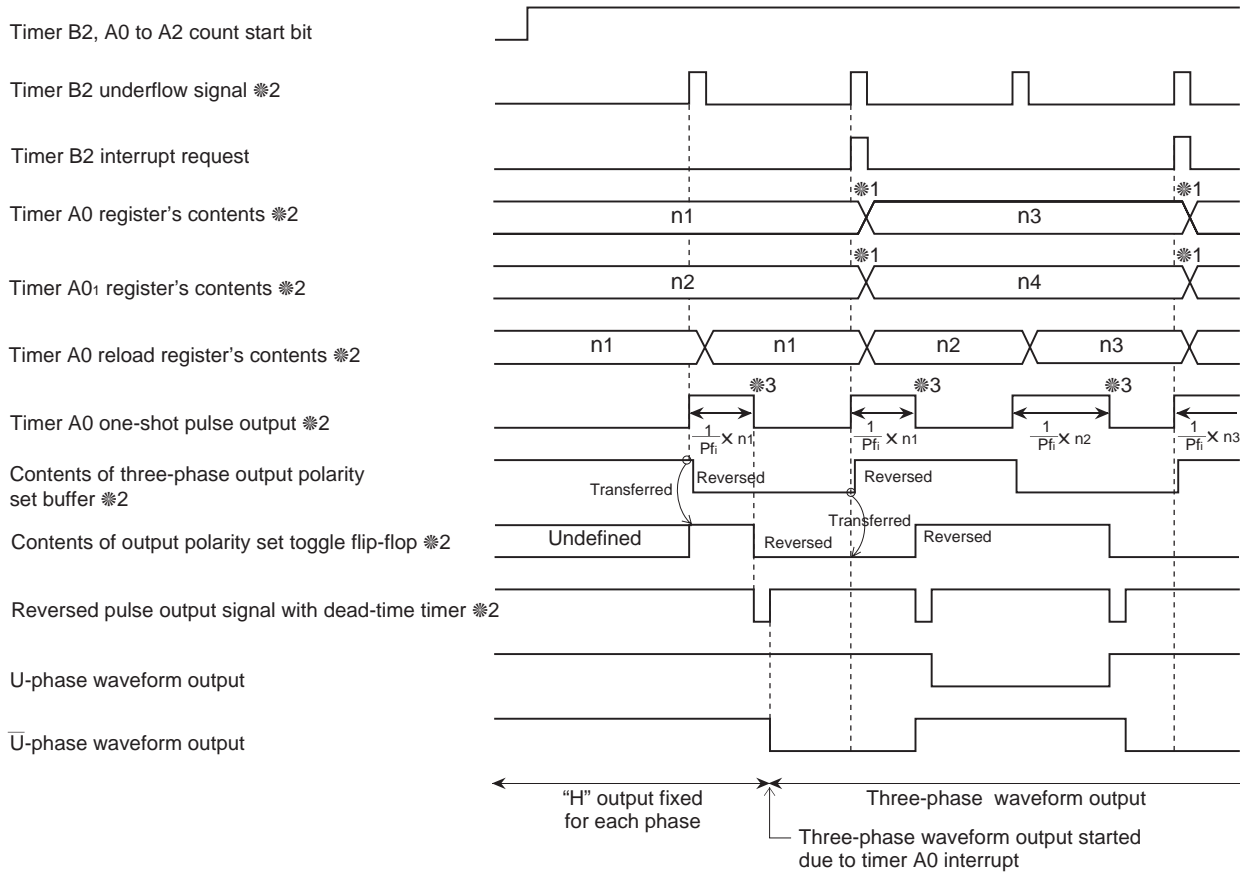
(1) Operation

The values of the timer A_i register ($i = 0$ to 2) and the timer A_{i1} register are alternately counted when three-phase mode 1 is used. However, immediately after the timer A_i starts counting, the timer A_i register's value is counted twice, consecutively. At this time, the timer A_i one-shot pulse also remains the same length twice. (See Figure 1.)

(2) Three-phase Mode 1 Application Example

Figures 1 through 4 show examples of three-phase mode 1. Figure 1 shows this mode's operations according to the settings indicated in Figures 2 through 4. The descriptions in Figure 1 are mainly for timer A0, U phase, and \bar{U} phase.

In this example, a timer A0 interrupt is used to start the waveform output after all three-phase output levels are stabilized. Therefore, it is assumed that the initial one-shot pulse width of timer A0 is larger than those of timers A1 and A2.



- **1 : Written by software.
 - **2 : Internal signal which cannot be read externally.
 - **3 : The contents of the timer A0 reload register are transferred to the counter at every falling edge of the timer A0 one-shot pulse output.
- P_{fi}: Count source for timer A0

Fig. 1 Three-phase Mode 1 Application Example: output waveforms

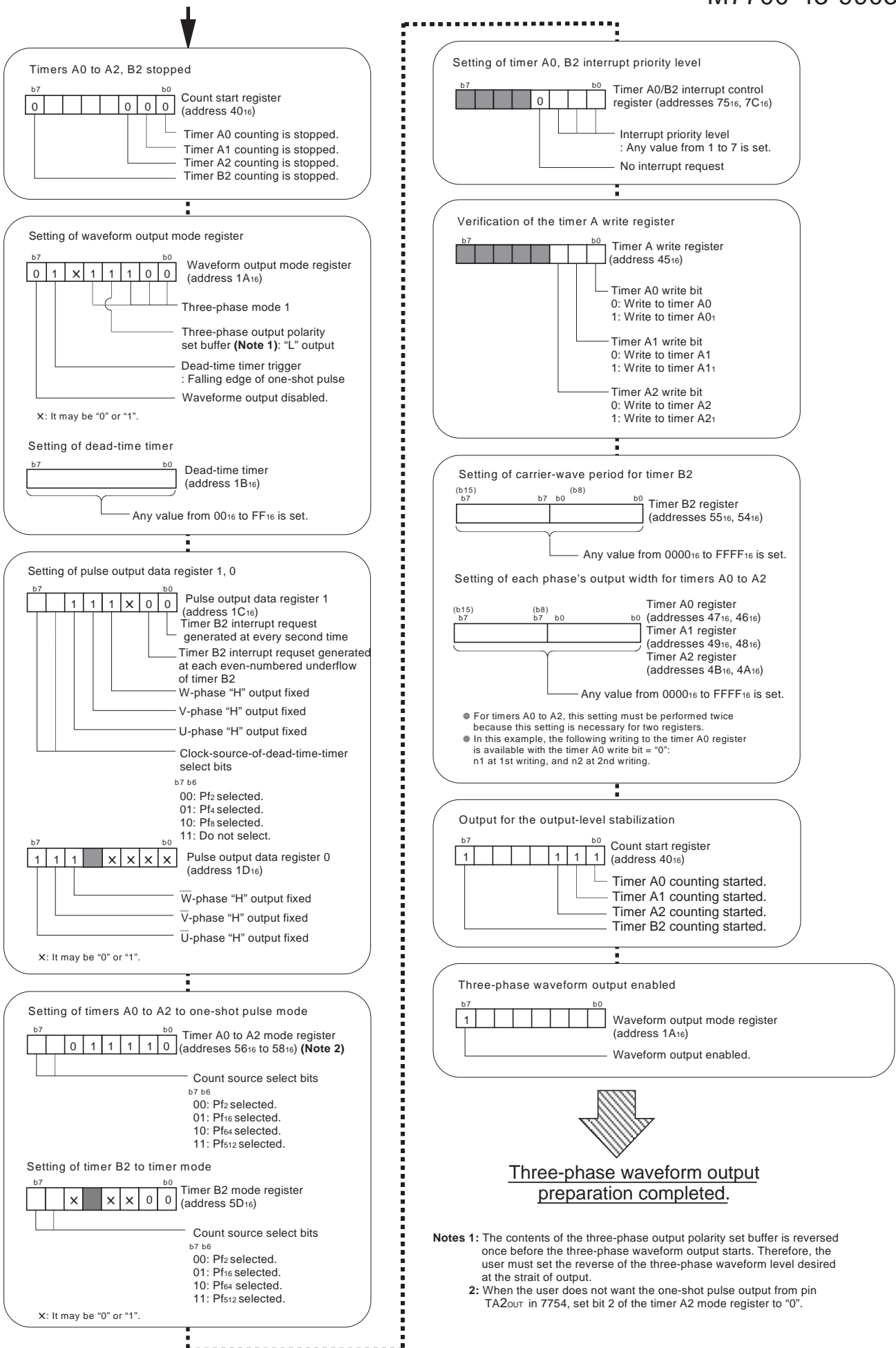


Fig. 2 Three-phase Mode 1 Application Example: initial setting example for related registers

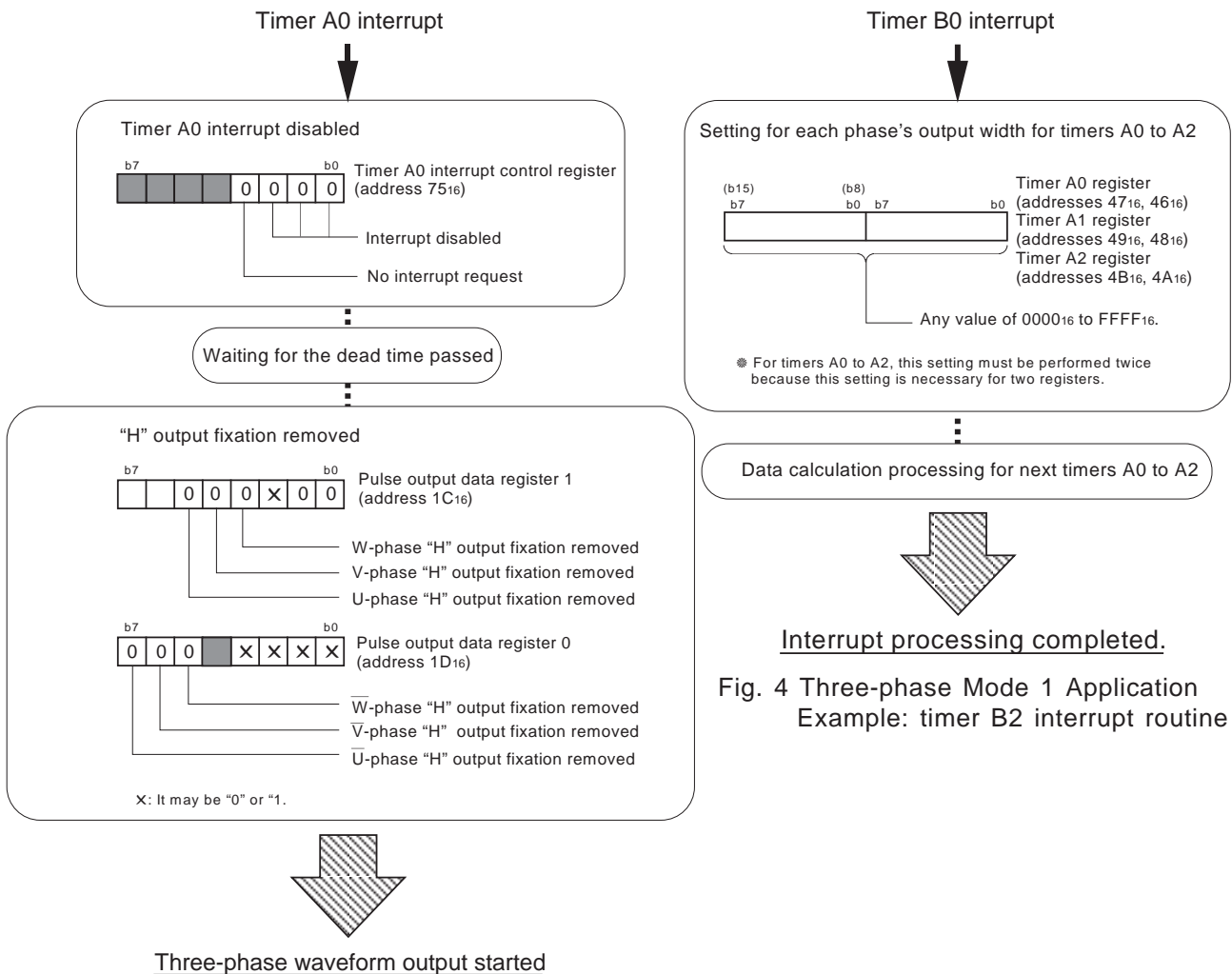


Fig. 3 Three-phase Mode 1 Application Example : timer A0 interrupt routine

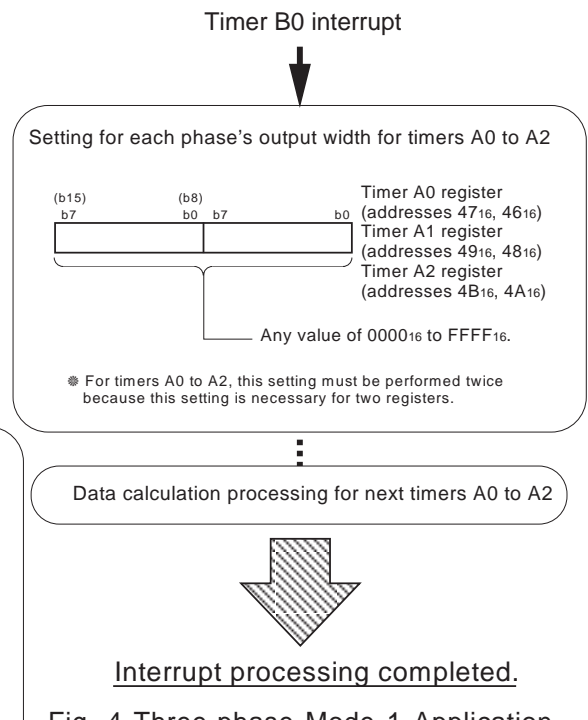


Fig. 4 Three-phase Mode 1 Application Example: timer B2 interrupt routine

3. How to Switch Pin Used for Three-phase Waveform Mode to Output Port Pin
 When a pin used for the three-phase waveform mode is needed to be switched to an output port pin, the following settings must be completed. In addition, these settings must be made while the waveform output control bit^{*1} = "0" (waveform output disabled).

- (1) Switching pin used for three-phase waveform mode to output port pin
 - ① Set output data to bit y^{*3} of the port Px^{*2} register. ^{*4}
 - ② Set bit y^{*3} of the port Px^{*2} direction register to "1" (output). ^{*4}
 - ③ Set bit 2 of the timer Az^{*5} mode register to "0".
 - ④ Set the waveform output select bit^{*6} to "000₂" (port).
- (2) Switching output port pin back to pin for three-phase waveform mode
 To switch an output port pin which has been switched in step (1) back to a pin for the three-phase waveform mode:
 - ① Set bit 2 of the timer Az^{*5} mode register to "1".
 - ② Set the waveform output select bit^{*6} to "100₂" (three-phase waveform mode).

^{*1}: 7754/53: bit 7 at address 1A₁₆
^{*2}, ^{*3}: 7754: bits 0 to 3 of port P5, bits 1 and 2 of port P9,
 7753: bits 0 to 5 of port P5
^{*4}: This can be omitted if already set by the initial settings, etc.
^{*5}: 7754: timers A0 and A1, 7753: timers A0 to A2
^{*6}: 7754/53: bits 2 to 0 at address 1A₁₆