

To our customers,

Old Company Name in Catalogs and Other Documents

On April 1st, 2010, NEC Electronics Corporation merged with Renesas Technology Corporation, and Renesas Electronics Corporation took over all the business of both companies. Therefore, although the old company name remains in this document, it is a valid Renesas Electronics document. We appreciate your understanding.

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April 1st, 2010
Renesas Electronics Corporation

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MSC TECHNICAL NEWS

No. M720-23-9707

Additional information of 4250 Group (Rev.B)

The error of 4250 Group exists in the following documents.
Please refer to the corrected information as shown below.

- Data Book "1997 Mitsubishi Single-chip 4-bit Microcomputers" [document number: H-DF463-A]
- 4250 Group User's Manual [document number: H-EF489-A]

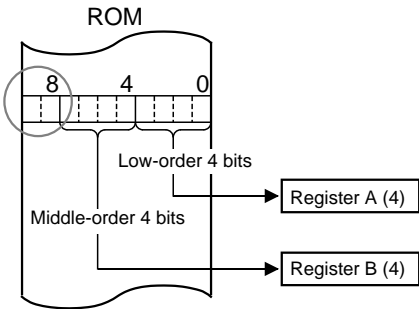
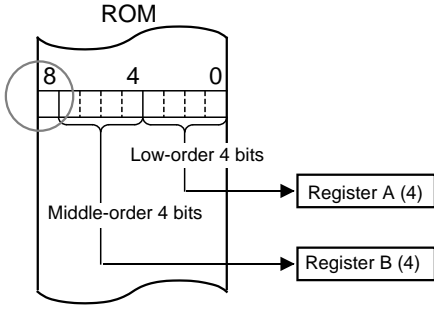
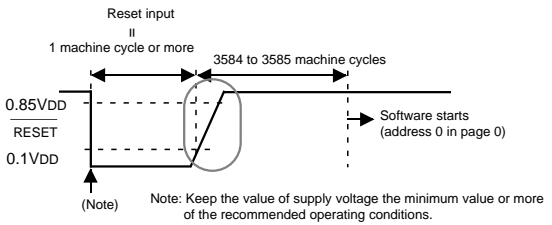
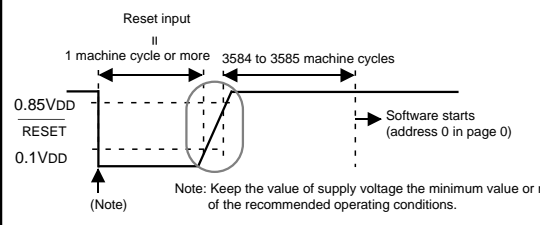
Corrected information of 420 Group (Rev.B)

(1) Data Book "1997 Mitsubishi Single-chip 4-bit Microcomputers" [document number: H-DF463-A]

Page	Error	Correct																					
2-7 CONNECTIONS OF UNUSED PINS	Refer to page 3.																						
2-8 PORT FUNCTION	<table border="1"> <tr> <td>Port G</td> <td>G₀/INT</td> <td>⋮ K₀</td> <td rowspan="3">Pull-up functions (programmable) Key-on wakeup functions (programmable)</td> </tr> <tr> <td></td> <td>G₁/T_{OUT}</td> <td>⋮ K₀</td> </tr> <tr> <td></td> <td>G₂, G₃</td> <td>⋮ K₀</td> </tr> </table>	Port G	G ₀ /INT	⋮ K ₀	Pull-up functions (programmable) Key-on wakeup functions (programmable)		G ₁ /T _{OUT}	⋮ K ₀		G ₂ , G ₃	⋮ K ₀	<table border="1"> <tr> <td>Port G</td> <td>G₀/INT</td> <td>⋮ K₀</td> <td rowspan="2">Pull-up function Key-on wakeup function (Only pull-up function is programmable)</td> </tr> <tr> <td></td> <td>G₁/T_{OUT}</td> <td>⋮ K₀</td> </tr> <tr> <td></td> <td>G₂, G₃</td> <td>⋮ K₀</td> <td>Pull-up function (programmable) Key-on wakeup function (programmable)</td> </tr> </table>	Port G	G ₀ /INT	⋮ K ₀	Pull-up function Key-on wakeup function (Only pull-up function is programmable)		G ₁ /T _{OUT}	⋮ K ₀		G ₂ , G ₃	⋮ K ₀	Pull-up function (programmable) Key-on wakeup function (programmable)
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2-13 FUNCTIONAL BLOCK OPERATIONS Fig.4																							
2-26 RESET FUNCTION Fig.21																							
2-32 © Notes on unused pins	Refer to page 4.																						

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(2) 4250 Group User's Manual [document number: H-EF489-A]

Page	Error	Correct																						
1-7 CONNECTIONS OF UNUSED PINS	Refer to page 3.																							
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1-32 ⑥ Notes on unused pins	Refer to page 4.																							
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3-9 ⑥ Notes on unused pins	Refer to page 4.																							

CONNECTIONS OF UNUSED PINS (corrected)

CONNECTIONS OF UNUSED PINS

Pin	Connection	Pin	Connection
F ₀ , F ₁	Connect to V _{SS} pin.	D ₀ , D ₁	Connect to V _{SS} pin.
G ₀ /INT, G ₁ /T _{OUT}	Open or connect to V _{SS} pin. (Note 1)	D ₂ /C, D ₃ /K	Open or connect to V _{SS} pin. (Note 3)
G ₂ , G ₃			
S ₀ –S ₃	Connect to V _{SS} pin. (Note 2)		

Notes 1: When pins G₀/INT, G₁/T_{OUT}, G₂ and G₃ are connected to V_{SS} pin, turn off their pull-up transistors (Pull-up control register PU0="X0₂") and also invalidate the key-on wakeup functions of pins G₁/T_{OUT}, G₂ and G₃ (Key-on wakeup control register K0="XX0X₂") by software. When the POF instruction is executed while these pins are connected to V_{SS} and the key-on wakeup functions are left valid, the system returns from RAM back-up state by recognizing the return condition immediately after going into the RAM back-up state. When these pins are open, turn on their pull-up transistors (Pull-up control register PU0="X1₂") by software.

2: When ports S₀–S₃ are connected to V_{SS} pin, invalidate the key-on wakeup functions (Key-on wakeup control register K0="XXX0₂") by software. When the POF instruction is executed while these pins are connected to V_{SS} and the key-on wakeup functions are left valid, the system returns from RAM back-up state by recognizing the return condition immediately after going into the RAM back-up state.

3: When ports D₂/C and D₃/K are connected to V_{SS} pin, turn off their pull-up transistors (register PU0="0X₂") by software. When these pins are open, turn on their pull-up transistors (register PU0="1X₂") by software.

(Note when connecting to V_{SS} and V_{DD})

- Connect the unused pins to V_{SS} or V_{DD} at the shortest distance and use the thick wire against noise.

≈ Notes on unused pins (corrected)

LIST OF PRECAUTIONS

① Noise and latch-up prevention

Connect a capacitor on the following condition to prevent noise and latch-up;

- connect a bypass capacitor (approx. 0.01 μF) between pins V_{DD} and V_{SS} at the shortest distance,
- equalize its wiring in width and length, and
- use the thickest wire.

In the One Time PROM version, CNV_{SS} pin is also used as V_{PP} pin. Connect this pin to V_{SS} through the resistor about 5 kΩ which is assigned to CNV_{SS}/V_{PP} pin as close as possible at the shortest distance.

② Prescaler

Stop the prescaler operation to change its frequency dividing ratio.

③ Timer count source

Stop timer 1 counting to change its count source.

④ Program counter

Make sure that the P_{CH} does not specify after the last page of the built-in ROM.

⑤ G₀/INT pin

When the interrupt valid waveform of the G₀/INT pin is changed with the bit 2 of register K₀ in software, be careful about the following notes.

- After clear the bit 0 of register V₁ to "0" (Figure 29①), change the interrupt valid waveform of G₀/INT pin with the bit 2 of register K₀.
- Set a value to bit 2 of register K₀ and execute the SNZ₀ instruction to clear the external interrupt request flag (EXF₀) after executing at least one instruction (refer to Figure 29②). Depending on the input state of the G₀/INT pin, the EXF₀ flag may be set when the interrupt valid waveform is changed.

⑥ Notes on unused pins

- When pins G₀/INT, G₁/T_{OUT}, G₂ and G₃ are connected to V_{SS} pin, turn off their pull-up transistors (register PU₀="X0₂") and also invalidate the key-on wakeup functions of pins G₁/T_{OUT}, G₂ and G₃ (register K₀="XX0X₂") by software. When the POF instruction is executed while these pins are connected to V_{SS} and the key-on wakeup functions are left valid, the system returns from RAM back-up state by recognizing the return condition immediately after going into the RAM back-up state. When these pins are open, turn on their pull-up transistors (register PU₀="X1₂") by software.
- When ports S₀–S₃ are connected to V_{SS} pin, invalidate the key-on wakeup functions (register K₀="XXX0₂") by software. When the POF instruction is executed while these pins are connected to V_{SS} and the key-on wakeup functions are left valid, the system returns from RAM back-up state by recognizing the return condition immediately after going into the RAM back-up state.
- When ports D₂/C and D₃/K are connected to V_{SS} pin, turn off their pull-up transistors (register PU₀="0X₂") by software. When these pins are open, turn on their pull-up transistors (register PU₀="1X₂") by software.

(Note when connecting to V_{SS} and V_{DD})

- Connect the unused pins to V_{SS} or V_{DD} at the shortest distance (within 20 mm) and use the thick wire against noise.

⑦ Multifunction

- G₀/INT pin can be also used as an I/O port G₀ even when it is used as INT pin.
- G₁/T_{OUT} pin can be also used as input port G₁ even when it is used as T_{OUT} pin.
- D₂/C pin can be also used as I/O port D₂ even when it is used as port C.
- D₃/K pin can be also used as I/O port D₃ even when it is used as port K.

```

:
LA 4      ; (XXX02)
TV1A     ; The SNZ0 instruction is valid ..... ①
LA 4
TK0A     ; Change of the interrupt valid waveform
NOP      ..... ②
SNZ0     ; The SNZ0 instruction is executed
NOP
:

```

X : this bit is not related to the setting of G₀/INT pin.

Fig. 29 External interrupt program example

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Table 2.1.3 connections of unused pins (corrected)

Table 2.1.3 connections of unused pins	
Pin	Connection
F0, F1	Connect to Vss pin.
G0/INT, G1/TOUT, G2, G3	Open or connect to Vss pin. (Note 1)
S0–S3	Connect to Vss pin. (Note 2)
D0, D1	Connect to Vss pin.
D2/C, D3/K	Open or connect to Vss pin. (Note 3)

Notes 1: When pins G0/INT, G1/TOUT, G2 and G3 are connected to Vss pin, turn off their pull-up transistors (register PU0="X02") and also invalidate the key-on wakeup functions of pins G1/TOUT, G2 and G3 (register K0="XX0X2") by software. When the **POF** instruction is executed while these pins are connected to Vss and the key-on wakeup functions are left valid, the system returns from RAM back-up state by recognizing the return condition immediately after going into the RAM back-up state. When these pins are open, turn on their pull-up transistors (register PU0="X12") by software.

2: When ports S0–S3 are connected to Vss pin, invalidate the key-on wakeup functions by software (register K0 = "XXX02"). When the **POF** instruction is executed while these pins are connected to Vss and the key-on wakeup functions are left valid, the system returns from RAM back-up state by recognizing the return condition immediately after going into the RAM back-up state.

3: When ports D2/C and D3/K are connected to Vss pin, turn off their pull-up transistors (register PU0="0X2") by software. When these pins are open, turn on their pull-up transistors (register PU0="1X2") by software.

(Note when connecting to Vss and VDD)

- Connect the unused pins to Vss or VDD at the shortest distance and use the thickest possible wire against noise.