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RENESAS TECHNICAL UPDATE

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Product Category	MPU/MCU		Document No.	TN-RZ*-A0148A/E	Rev.	1.00
Title	System SRAM Exclusive Access issue		Information Category	Technical Notification		
Applicable Product	RZ/T2M Group RZ/T2ME Group RZ/T2L Group RZ/N2L Group	Lot No. All	Reference Document	RZ/T2M Group User's Manual: Hardware Rev.1.20 (R01UH0916EJ0120) RZ/T2ME Group User's Manual: Hardware Rev.1.00 (R01UH1062EJ0100) RZ/T2L Group User's Manual: Hardware Rev.1.20 (R01UH0985EJ0120) RZ/N2L Group User's Manual: Hardware Rev.1.30 (R01UH0955EJ0130)		

This document describes an issue with the System SRAM Exclusive Access.

1. Issue

When exclusive access instructions from CPU are used to System SRAM, it may cause illegal operation as follows.

- Normal value can't be written for not only exclusive write but also other non-exclusive write.
- Read operations return the same value each 16 bytes even read address is different when ECC is enabled.

Target exclusive access instructions:

- Load-Exclusive: LDREXB, LDAEXB, LDREXH, LDAEXH, LDREX, LDAEX, LDREXD, LDAEXD
- Store-Exclusive: STREXB, STLEXB, STREXH, STLEXH, STREX, STLEX, STREXD, STLEXD
- Other: CLREX

2. Workaround

Do not use exclusive access instructions to System SRAM. For exclusive control, perform either of the methods below.

- Use Semaphore Register (SYTSEMF) for RZ/T2M and RZ/T2ME or mailbox and semaphore (MBXSEM) for RZ/T2L and RZ/N2L instead of exclusive access instruction.
- Use exclusive access to TCM (not via AXIS).
- Use exclusive access to System SRAM when it is configured as Cacheable and Non-shareable in the CPU's MPU setting. In this case, transaction of exclusive access is not transferred to System SRAM since exclusive monitor in CPU is used.

3. User's Manual revision

User's Manual: Hardware will be revised as follows:

RZ/T2M, RZ/T2ME

12. Internal Buses

12.4 Usage Notes

Current	Revision (Added)
- (No description)	**12.4.5 Restriction of Exclusive access** Exclusive access instructions for synchronization and semaphores in Cortex-R52 are prohibited to System SRAM. For exclusive control, perform either of the methods below, • Use Semaphore Register (SYTSEMF) instead of exclusive access instruction. • Use exclusive access to TCM (not via AXIS). • Use exclusive access to System SRAM when it is configured as Cacheable and Non-shareable in the CPU's MPU setting. In this case, transaction of exclusive access is not transferred to System SRAM. Target exclusive access instructions: • Load-Exclusive: LDREXB, LDAEXB, LDREXH, LDAEXH, LDREX, LDAEX, LDREXD, LDAEXD • Store-Exclusive: STREXB, STLEXB, STREXH, STLEXH, STREX, STLEX, STREXD, STLEXD • Other: CLREX

43. System SRAM (SYSRAM)

43.1 Overview

Table 43.1 System SRAM specifications

Current	Revision (Added)
- (No description)	Exclusive access: Not supported. It is prohibited to use exclusive access instruction from CPU.

43.4 Usage Notes

Current	Revision (Added)
- (No description)	**43.4.4 Exclusive access** It is prohibited to use exclusive access instruction from CPU to System SRAM. If used, operation results are not guaranteed including other non-exclusive access instruction to System SRAM. One exception is when System SRAM is configured as Cacheable and Non-shareable in the CPU's MPU setting. In this case, use of exclusive access instruction to System SRAM is allowed since exclusive monitor in CPU is used and transaction of exclusive access is not transferred to System SRAM. See also 12.4.5 Restriction of Exclusive access.

RZ/T2L

12. Internal Buses

12.4 Usage Notes

Current	Revision (Added)
- (No description)	**12.4.5 Restriction of Exclusive access** Exclusive access instructions for synchronization and semaphores in Cortex-R52 are prohibited to System SRAM. For exclusive control, perform either of the methods below, • Use mailbox and semaphore (MBXSEM) instead of exclusive access instruction. • Use exclusive access to TCM (not via AXIS). • Use exclusive access to System SRAM when it is configured as Cacheable and Non-shareable in the CPU's MPU setting. In this case, transaction of exclusive access is not transferred to System SRAM. Target exclusive access instructions: • Load-Exclusive: LDREXB, LDAEXB, LDREXH, LDAEXH, LDREX, LDAEX, LDREXD, LDAEXD • Store-Exclusive: STREXB, STLEXB, STREXH, STLEXH, STREX, STLEX, STREXD, STLEXD • Other: CLREX

42. System SRAM

42.1 Overview

Table 42.1 System SRAM specifications

Current	Revision (Added)
- (No description)	<table><tr><td>Exclusive access</td><td>Not supported. It is prohibited to use exclusive access instruction from CPU.</td></tr></table>

42.4 Usage Notes

Current	Revision (Added)
- (No description)	**42.4.4 Exclusive access** It is prohibited to use exclusive access instruction from CPU to System SRAM. If used, operation results are not guaranteed including other non-exclusive access instruction to System SRAM. One exception is when System SRAM is configured as Cacheable and Non-shareable in the CPU's MPU setting. In this case, use of exclusive access instruction to System SRAM is allowed since exclusive monitor in CPU is used and transaction of exclusive access is not transferred to System SRAM. See also 12.4.5 Restriction of Exclusive access.

RZ/N2L

12. Internal Buses

12.4 Usage Notes

Current	Revision (Added)
- (No description)	**12.4.5 Restriction of Exclusive access** Exclusive access instructions for synchronization and semaphores in Cortex-R52 are prohibited to System SRAM. For exclusive control, perform either of the methods below, • Use mailbox and semaphore (MBXSEM) instead of exclusive access instruction. • Use exclusive access to TCM (not via AXIS). • Use exclusive access to System SRAM when it is configured as Cacheable and Non-shareable in the CPU's MPU setting. In this case, transaction of exclusive access is not transferred to System SRAM. Target exclusive access instructions: • Load-Exclusive: LDREXB, LDAEXB, LDREXH, LDAEXH, LDREX, LDAEX, LDREXD, LDAEXD • Store-Exclusive: STREXB, STLEXB, STREXH, STLEXH, STREX, STLEX, STREXD, STLEXD • Other: CLREX

43. System SRAM

43.1 Overview

Table 43.1 System SRAM specifications

Current	Revision (Added)
- (No description)	<table><tr><td>Exclusive access</td><td>Not supported. It is prohibited to use exclusive access instruction from CPU.</td></tr></table>

43.4 Usage Notes

Current	Revision (Added)
- (No description)	**43.4.4 Exclusive access** It is prohibited to use exclusive access instruction from CPU to System SRAM. If used, operation results are not guaranteed including other non-exclusive access instruction to System SRAM. One exception is when System SRAM is configured as Cacheable and Non-shareable in the CPU's MPU setting. In this case, use of exclusive access instruction to System SRAM is allowed since exclusive monitor in CPU is used and transaction of exclusive access is not transferred to System SRAM. See also 12.4.5 Restriction of Exclusive access.