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RENESAS TECHNICAL UPDATE

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Product Category	MPU/MCU		Document No.	TN-RZ*-A0155A/E	Rev.	1.00
Title	System SRAM Exclusive Access issue		Information Category	Technical Notification		
Applicable Product	RZ/V2M RZ/V2MA	Lot No. All	Reference Document	RZ/V2M User's Manual: Hardware Rev.2.01 (Additional Document) RZ/V2MA User's Manual: Hardware Rev.1.11 (Additional Document)		

This document describes an issue with the System SRAM Exclusive Access.

1. Issue

When exclusive access instructions from CPU are used to System SRAM, it may cause illegal operation as follows.

- Normal value can't be written for not only exclusive write but also other non-exclusive write.
- Read operations return the same value each 16 bytes even read address is different when ECC is enabled.

Target exclusive access instructions:

For Cortex-A53 AArch64 mode (64 bit)

- Load-Exclusive: LDXRB, LDAXRB, LDXRH, LDAXRH, LDXR, LDAXR, LDXP, LDAXP
- Store-Exclusive: STXRB, STLXRB, STXRH, STLXRH, STXR, STLXR, STXP, STLXP
- Other: CLREX

For Cortex-A53 AArch32 mode (32 bit)

- Load-Exclusive: LDREX, LDREXB, LDREXH, LDREXD
- Store-Exclusive: STREX, STREXB, STREXH, STREXD
- Other: CLREX

2. Workaround

Exclusive access instructions for synchronization and semaphores in Cortex-A53 are prohibited to RAMA. For exclusive control, perform either of the methods below,

- Use exclusive access to LPDDR4 SDRAM, RAMB0～RAMB3
- Use exclusive access to RAMA when it is configured as Cacheable and Non-shareable in the CPU's MPU setting. In this case, transaction of exclusive access is not transferred to RAMA.

3. User's Manual revision

User's Manual: Hardware will be revised as follows:

RZ/V2M	RZ/V2MA
Section 12 RAM A (RAMA)	Section 12 RAM A (RAMA)
12.1 Functional Overview	12.1 Functional Overview

[From]

12.1 Functional Overview

This unit is a RAM with ECC error detection and correction functions.

This unit has a function to detect and correct errors by ECC of data recorded in the internal RAM. It also has a FIFO function that retains transactions when accesses from various channels to the RAM are in conflict and access is not possible.

[To]

12.1 Functional Overview

This unit is a RAM with ECC error detection and correction functions.

This unit has a function to detect and correct errors by ECC of data recorded in the internal RAM. It also has a FIFO function that retains transactions when accesses from various channels to the RAM are in conflict and access is not possible.

Exclusive access to this unit is not supported. It is prohibited to use exclusive access instructions from the CPU.

RZ/V2M	RZ/V2MA
Section 12 RAM A (RAMA)	Section 12 RAM A (RAMA)
12.6 Usage Note	12.6 Usage Note
12.6.2 Exclusive Access	12.6.2 Exclusive Access

[From]

12.6.2 Exclusive Access

When an exclusive read is performed for the same access information with different AxIDs (AXI bus IDs), the portion of the exclusive read that can be monitored succeeds, and the AxID and address information are monitored separately. After this, when an exclusive write is performed, the exclusive access succeeds only for the first exclusive write that has occurred, and the exclusive access monitor for the same AxID, including its own and others, which was set in the same access information, is cleared, and subsequent exclusive writes fail.

[To]

12.6.2 Exclusive Access

It is prohibited to use exclusive access instructions from the CPU to the system SRAM. If used, operation results are not guaranteed, including those of other non-exclusive access instructions to the system SRAM.

One exception is when the system SRAM is configured as Cacheable and Non-shareable in the CPU's MPU setting. In this case, the use of exclusive access instructions to the system SRAM is allowed, since the exclusive monitor in the CPU is used and the transaction of the exclusive access is not transferred to the system SRAM. See also **Section 46.6.1, Restriction of Exclusive access**.

RZ/V2M	RZ/V2MA
Section 46 Interconnect Bus (ICB)	Section 35 Interconnect Bus (ICB)

The revision information about Interconnect Bus (ICB) will be documented in the User's Manual (NDA-based).
These are expected to be available in May, 2026. For further details, please contact your local sales office.