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RENESAS TECHNICAL UPDATE

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Product Category	MPU/MCU		Document No.	TN-RZ*-A0149A/E	Rev.	1.00
Title	System SRAM Exclusive Access issue		Information Category	Technical Notification		
Applicable Product	RZ/T2H and RZ/N2H Groups	Lot No. All	Reference Document	RZ/T2H and RZ/N2H Groups User's Manual: Hardware Rev.1.10 (R01UH1039EJ0110)		

This document describes an issue with the System SRAM Exclusive Access.

1. Issue

When exclusive access instructions from CPU are used to System SRAM, it may cause illegal operation as follows.

- Normal value can't be written for not only exclusive write but also other non-exclusive write.
- Read operations return the same value each 16 bytes even read address is different when ECC is enabled.

Target exclusive access instructions:

For Cortex-A55

- Load-Exclusive: LDXRB, LDAXRB, LDXRH, LDAXRH, LDXR, LDAXR, LDXP, LDAXP
- Store-Exclusive: STXRB, STLXRB, STXRH, STLXRH, STXR, STLXR, STXP, STLXP
- Other: CLREX

For Cortex-R52

- Load-Exclusive: LDREXB, LDAEXB, LDREXH, LDAEXH, LDREX, LDAEX, LDREXD, LDAEXD
- Store-Exclusive: STREXB, STLEXB, STREXH, STLEXH, STREX, STLEX, STREXD, STLEXD
- Other: CLREX

2. Workaround

Do not use exclusive access instructions to System SRAM. For exclusive control, perform either of the methods below.

- Use mailbox and semaphore (MBXSEM) instead of exclusive access instruction.
- Use exclusive access to LPDDR4 SDRAM.
- Use exclusive access to System SRAM when it is configured as Cacheable and Non-shareable in the CPU's MPU or MMU setting. In this case, transaction of exclusive access is not transferred to System SRAM since exclusive monitor in CPU is used.

3. User's Manual revision

User's Manual: Hardware will be revised as follows:

13. Internal Buses

13.5 Usage Notes

Current	Revision (Changed)
13.5.5 Exclusive Access Exclusive access instructions for synchronization and semaphores, and atomic instructions in Cortex-R52 and Cortex-A55 are not supported in the sharable areas. Use mailbox and semaphore (MBXSEM) for exclusive control. For details of the target instructions, see the below sections in Arm Architecture Reference Manual for A-profile architecture (DDI 0487). ● For AArch64 - B2.17 Synchronization and semaphores - C3.2.12 Atomic instructions ● For AArch32 - E2.10 Synchronization and semaphores	**13.5.5 Restriction of Exclusive access** Exclusive access instructions for synchronization and semaphores in Cortex-R52 and Cortex-A55 are prohibited to System SRAM. For exclusive control, perform either of the methods below, • Use mailbox and semaphore (MBXSEM) instead of exclusive access instruction. • Use exclusive access to LPDDR4 SDRAM. • Use exclusive access to System SRAM when it is configured as Cacheable and Non-shareable in the CPU's MPU or MMU setting. In this case, transaction of exclusive access is not transferred to System SRAM. Target exclusive access instructions: For Cortex-A55 • Load-Exclusive: LDXRB, LDAXRB, LDXRH, LDAXRH, LDXR, LDAXR, LDXP, LDAXP • Store-Exclusive: STXRB, STLXRB, STXRH, STLXRH, STXR, STLXR, STXP, STLXP • Other: CLREX For Cortex-R52 • Load-Exclusive: LDREXB, LDAEXB, LDREXH, LDAEXH, LDREX, LDAEX, LDREXD, LDAEXD • Store-Exclusive: STREXB, STLEXB, STREXH, STLEXH, STREX, STLEX, STREXD, STLEXD • Other: CLREX

44. System SRAM (SYSRAM)

44.1 Overview

Table 44.1 System SRAM specifications

Current	Revision (Added)
- (No description)	Exclusive access: Not supported. It is prohibited to use exclusive access instruction from CPU.

44.5 Usage Notes

Current	Revision (Added)
- (No description)	**44.5.4 Exclusive access** It is prohibited to use exclusive access instruction from CPU to System SRAM. If used, operation results are not guaranteed including other non-exclusive access instruction to System SRAM. One exception is when System SRAM is configured as Cacheable and Non-shareable in the CPU's MPU or MMU setting. In this case, use of exclusive access instruction to System SRAM is allowed since exclusive monitor in CPU is used and transaction of exclusive access is not transferred to System SRAM. See also 13.5.5 Restriction of Exclusive access.

57. LPDDR4 SDRAM Subsystem (DDRSS)

57.1 Overview

Table 57.1 Specifications of DDRSS

Current	Revision (Added)
MC • Fully pipelined command, read and write data interfaces to the controller. • Advanced bank look-ahead features for high memory throughput. • A programmable register interface to control memory parameters and protocols including auto pre-charge. • Full initialization of memory on controller reset. • Supports the Weighted Round-Robin arbitration schema for arbitrating request from the ports. • ECC function for single-bit and double-bit error reporting, single-bit error correction, and programmable removal of ECC storage. • Built-in Self test (BIST) for external DRAM memories.	MC • Fully pipelined command, read and write data interfaces to the controller. • Advanced bank look-ahead features for high memory throughput. • A programmable register interface to control memory parameters and protocols including auto pre-charge. • Full initialization of memory on controller reset. • Supports the Weighted Round-Robin arbitration schema for arbitrating request from the ports. • ECC function for single-bit and double-bit error reporting, single-bit error correction, and programmable removal of ECC storage. • Built-in Self test (BIST) for external DRAM memories. • Supports exclusive access instruction each port up to 2 transactions.

57.6 Usage Notes

Table 57.35 Restrictions

Current	Revision (Added)
- (No description)	Exclusive access: Each port can monitor the exclusivity of up to 2 transactions. If the exclusive monitor buffer is full and a new exclusive access command is received, the oldest exclusive access entry will be overwritten. As a result, performance may decrease.