RENESAS TECHNICAL UPDATE

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Product Category	MPU/MCU		Document No.	TN-RX*-A176A/E	Rev.	1.00
Title	Supplementary Information on and Errata to the SD Slave Interface (SDSI),12-Bit A/D Converter (S12ADFa) and Electrical Characteristics for the RX65N Group, RX651 Group		Information Category	Technical Notification		
Applicable Product	RX65N Group, RX651 Group	Lot No. All	Reference Document	RX65N Group, RX651 Group User's Manual: Hardware Rev.1.00 (R01UH0590EJ0100)		

This document describes the supplementary information and errata to sections I/O Registers, Interrupt Controller (ICUB), SD Slave Interface (SDSI), 12-Bit A/D Converter (S12ADFa), and Electrical Characteristics of the RX65N Group, RX651 Group User's Manual: Hardware, Rev.1.00.

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An access size of 8 bits is added to the FN1 data registers in Table 5.1, List of I/O Registers (Address Order) (45/57) as follows.

Before correction

Address	Module Symbol	Register Name	Register Symbol	Number of Bits	Access Size	Number of Access Cycles		Related Function	Reference Page
						ICLK ≥ PCLK	ICLK < PCLK		
Omitted									
0009 5800h to 0009 58FFh	SDSI	FN1 Data Register 10 to 163	FN1DATAR10 to 163	32	32	10,11 PCLKB	2 to 6 ICLK	SDSI	2041
0009 5900h to 0009 59FFh	SDSI	FN1 Data Register 20 to 263	FN1DATAR20 to 263	32	32	10,11 PCLKB	2 to 6 ICLK	SDSI	2041
0009 5A00h to 0009 5AFFh	SDSI	FN1 Data Register 30 to 363	FN1DATAR30 to 363	32	32	10,11 PCLKB	2 to 6 ICLK	SDSI	2042
0009 5B00h	SDSI	FN1 Interrupt Vector Register	FN1INTVECR	8	8	7,8 PCLKB	2 to 5 ICLK	SDSI	2042
0009 5B01h	SDSI	FN1 Interrupt Clear Register	FN1INTCLRR	8	8	7,8 PCLKB	2 to 5 ICLK	SDSI	2043
0009 5C00h to 0009 5FFFh	SDSI	FN1 Data Register 50 to 5255	FN1DATAR50 to 5255	32	32	7,8 PCLKB	2 to 5 ICLK	SDSI	2043
Omitted									

After correction

Address	Module Symbol	Register Name	Register Symbol	Number of Bits	Access Size	Number of Access Cycles		Related Function	Reference Page
						ICLK ≥ PCLK	ICLK < PCLK		
Omitted									
0009 5800h to 0009 58FFh	SDSI	FN1 Data Register 10 to 163	FN1DATAR10 to 163	32	8, 32	10,11 PCLKB	2 to 6 ICLK	SDSI	2041
0009 5900h to 0009 59FFh	SDSI	FN1 Data Register 20 to 263	FN1DATAR20 to 263	32	8, 32	10,11 PCLKB	2 to 6 ICLK	SDSI	2041
0009 5A00h to 0009 5AFFh	SDSI	FN1 Data Register 30 to 363	FN1DATAR30 to 363	32	8, 32	10,11 PCLKB	2 to 6 ICLK	SDSI	2042
0009 5B00h	SDSI	FN1 Interrupt Vector Register	FN1INTVECR	8	8	7,8 PCLKB	2 to 5 ICLK	SDSI	2042
0009 5B01h	SDSI	FN1 Interrupt Clear Register	FN1INTCLRR	8	8	7,8 PCLKB	2 to 5 ICLK	SDSI	2043
0009 5C00h to 0009 5FFFh	SDSI	FN1 Data Register 50 to 5255	FN1DATAR50 to 5255	32	8, 32	7,8 PCLKB	2 to 5 ICLK	SDSI	2043
Omitted									

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The name of the SDIOI interrupt for group BL2 in Table 15.7, Group Interrupt Requests (2/2) is corrected as follows.

Before correction

Group	No.	Interrupt Request Source	Name	GEN[BA][EL]m.ENj Bit	GRP[BA][EL]m.ISj Flag	GCRBEm.CLRj Bit	Vector No. (IRn.IR)
Omitted							
BL2	0	SDSI	SDIOI (direct mode end)	GENBL2.EN0	GRPBL2.IS0	—	107
	1 to 31	Reserved	—	—	—	—	
Omitted							

After correction

Group	No.	Interrupt Request Source	Name	GEN[BA][EL]m.ENj Bit	GRP[BA][EL]m.ISj Flag	GCRBEm.CLRj Bit	Vector No. (IRn.IR)
Omitted							
BL2	0	SDSI	SDIOI (SDSI interrupt)	GENBL2.EN0	GRPBL2.IS0	—	107
	1 to 31	Reserved	—	—	—	—	
Omitted							

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Table 44.3, SDSI Register Map is modified as follows.

Before correction

SDIO Space	Function	SD Host		CPU	
		R/W	Address	R/W	Address
CIA (Function 0)	CCCR	R/W	000000h to 0000FFh	—	—
	FBR	R/W	000100h to 0001FFh	—	—
	CIS	R	001000h to 00106Bh	R/W*3	00095200h to 0009526Bh
Function Unique (Function 1)	Register 1 (256 bytes)	R/W*1	000000h to 0000FFh	R/W	00095800h to 000958FFh
	Register 2 (256 bytes)	R*1	000100h to 0001FFh	W	00095900h to 000959FFh
	Register 3 (256 bytes)	W*1	000200h to 0002FFh	R	00095A00h to 00095AFFh
	Register 4 (2 bytes)*4	R/W*1	000300h to 000301h	R/W	00095B00h to 00095B01h
	Register 5 (1 Kbytes)	R/W*1, *2	000400h to 0007FFh	R/W*2	00095C00h to 00095FFFh

Note 1. No access while a DMA transfer is in progress.
Note 2. Simultaneous access from both the SD host and CPU is not available.
Note 3. Complete the setting before starting the communication with the SD host.
Note 4. FN1 Interrupt Vector Register (FN1INTVECR) and FN1 Interrupt Clear Register (FN1INTCLRR)

After correction

SDIO Space	Function	SD Host Address	SD Host R/W	CPU Register	CPU Address	CPU R/W
CIA (Function 0)	CCCR	000000h, 000001h	R	—	—	—
		000002h	R/W	SDSICR1	0009500Ah	R
		000003h	R	SDSICR1	0009500Ah	W
		000004h to 000011h	R/W	—	—	—
		000012h	R/W	SDSICR1, SDSICR3	0009500Ah, 00095104h	R/W
		000013h	R/W	—	—	—
	FBR	000100h, 000101h	R	FBR1	00095270h	R/W
		000102h	R/W	SDSICR1, SDSICR3	0009500Ah, 00095104h	R/W
		000103h	R	FBR2	00095274h	R/W
		000104h, 000105h	R	FBR3	00095278h	R/W
		000106h, 000107h	R	FBR4	0009527Ch	R/W
		000108h	R	FBR5	00095280h	R/W
		000109h to 00010Bh	R	—	—	—
		000110h, 000111h	R/W	—	—	—
	CIS	001000h to 00106Bh	R	CISDATARi*3	00095200h to 0009526Bh	R/W
Function Unique (Function 1)	Register 1 (256 bytes)	000000h to 0000FFh	R/W	FN1DATAR1i*1	00095800h to 000958FFh	R/W
	Register 2 (256 bytes)	000100h to 0001FFh	R	FN1DATAR2i*1	00095900h to 000959FFh	W
	Register 3 (256 bytes)	000200h to 0002FFh	W	FN1DATAR3i*1	00095A00h to 00095AFFh	R
	Register 4 (2 bytes)	000300h	R	FN1INTVECR*1	00095B00h	R/W
		000301h	W	FN1INTCLRR*1	00095B01h	R
	Register 5 (1 Kbytes)*2	000400h to 0007FFh	R/W	FN1DATAR5i*1, *2	00095C00h to 00095FFFh	R/W

Note 1. These registers are not used when DMA transfer is enabled.
Note 2. Simultaneous access from both the SD host and CPU is not available.
Note 3. Complete the setting before starting the communication with the SD host.

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The functional descriptions for the RSWAP bit and WSWAP bit in section 44.3.13, SDSI Control Register 2 (SDSICR2) are corrected as follows.

Before correction

Bit	Symbol	Bit Name	Description	R/W
b0	RSWAP	Read Swap	Enables swapping of the data of Register1 to 5 in Function1 in byte units and reading of the data. 0: No swapping 1: Swap the data in byte units and read the data.	R/W
b1	—	Reserved	This bit is read as 0. The write value should be 0.	R
b2	WSWAP	Write Swap	Enables swapping of the data of Register1 to 5 in Function1 in byte units and reading of the data. 0: No swapping 1: Swap the data in byte units and read the data.	R/W
			Omitted	

After correction

Bit	Symbol	Bit Name	Description	R/W
b0	RSWAP	Read Swap	The data of registers FN1DATAR1i, FN1DATAR2i, FN1DATA3Ri, and FN1DATAR5i can be read with swapping the byte and word positions when reading the data. 0: Read data without swapping 1: Read data with swapping the byte and word positions	R/W
b1	—	Reserved	This bit is read as 0. The write value should be 0.	R
b2	WSWAP	Write Swap	The data of registers FN1DATAR1i, FN1DATAR2i, FN1DATA3Ri, and FN1DATAR5i can be written with swapping the byte and word positions when writing the data. 0: Write data without swapping 1: Write data with swapping the byte and word positions	R/W
			Omitted	

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The functional descriptions for the CDF and CDR flags in section 44.3.16, Interrupt Status Register 2 (INTSR2) are corrected as follows.

Before correction

Bit	Symbol	Bit Name	Description	R/W
b0	CDF	Card Detection Disabled (Fall) Flag	Indicates that the CD-Disable bit in the CCCR has changed from 1 to 0. 0: Card detection disable (fall) has not been changed 1: Card detection disable (fall) has been changed from 0 to 1.	R/W
b1	CDR	Card Detection Disabled (Rise) Flag	Indicates that the CD-Disable bit in the CCCR has changed from 0 to 1. 0: Card detection disable (rise) has not been changed 1: Card detection disable (rise) has been changed from 1 to 0.	R/W
			Omitted	

After correction

Bit	Symbol	Bit Name	Description	R/W
b0	CDF	CD Disable Fall Detected Flag	Indicates that the CD Disable bit in the CCCR has changed from 1 to 0. 0: CD Disable is not changed 1: CD Disable has been changed from 1 to 0	R/W
b1	CDR	CD Disable Rise Detected Flag	Indicates that the CD Disable bit in the CCCR has changed from 0 to 1. 0: CD Disable is not changed 1: CD Disable has been changed from 1 to 0	R/W
			Omitted	

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The functional descriptions for the DMARSWAP[1:0] bits and DMAWSWAP[1:0] bits in section 44.3.17, DMA Control Register 2 (DMACR2) are corrected as follows.

Before correction

Bit	Symbol	Bit Name	Description	R/W
b1, b0	DMARSWAP[1:0]	DMA Transfer Read Swap	Swap the data to be DMA-transferred in byte or word units and read the data. b1 b0 0 0: No swapping 0 1: Swap the data in byte units and read the data. 1 0: Swap the data in word units and read the data. 1 1: Swap the data in byte/word units and read the data.*1	R/W
b3, b2	DMAWSWAP[1:0]	DMA Transfer Write Swap	Swap the data for DMA transfer in byte/word units and write the data. b3 b2 0 0: No swapping 0 1: Swap the data in byte units and read the data. 1 0: Swap the data in word units and read the data. 1 1: Swap the data in byte/word units and read the data.*1	R/W
			Omitted	

After correction

Bit	Symbol	Bit Name	Description	R/W
b1, b0	DMARSWAP[1:0]	DMA Transfer Read Swap	Enables swapping of the data to be transferred by the DMAC in byte and/or word units when reading the data. b1 b0 0 0: Read data with swapping the byte and word positions*1 0 1: Read data with swapping the word position 1 0: Read data with swapping the byte position 1 1: Read data without swapping	R/W
b3, b2	DMAWSWAP[1:0]	DMA Transfer Write Swap	Enables swapping of the data to be transferred by the DMAC in byte and/or word units when writing the data. b3 b2 0 0: Write data with swapping the byte and word positions*1 0 1: Write data with swapping the word position 1 0: Write data with swapping the byte position 1 1: Write data without swapping	R/W
Omitted				

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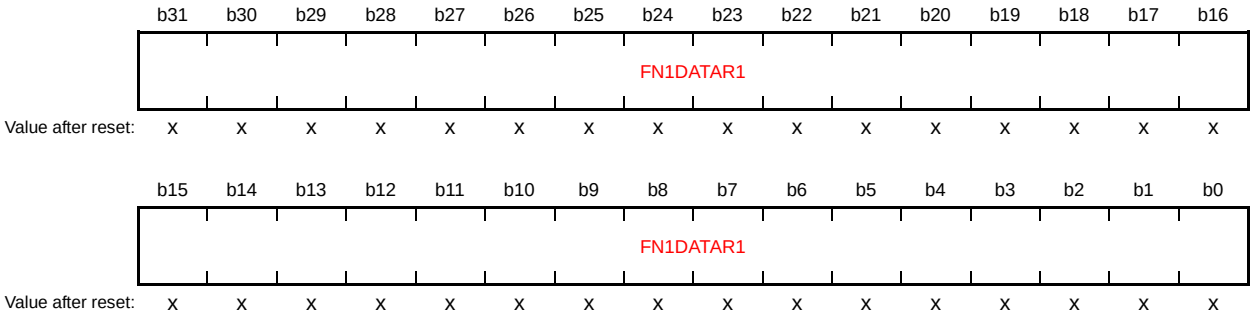
The bit charts and bit description tables in section 44.3.24, FN1 Data Register 1i (FN1DATAR1i) (i = 0 to 63), section 44.3.25, FN1 Data Register 2i (FN1DATAR2i) (i = 0 to 63), section 44.3.26, FN1 Data Register 3i (FN1DATAR3i) (i = 0 to 63), and section 44.3.29, FN1 Data Register 5i (FN1DATAR5i) (i = 0 to 255) are modified as follows.

The following bit chart and bit description table are of the FN1DATAR1i register, and the corresponding charts and tables in the other registers are modified in the same way.

Before correction

Address(es): SDSI.FN1DATAR10 to SDSI.FN1DATAR163 0009 5800h to 0009 58FFh

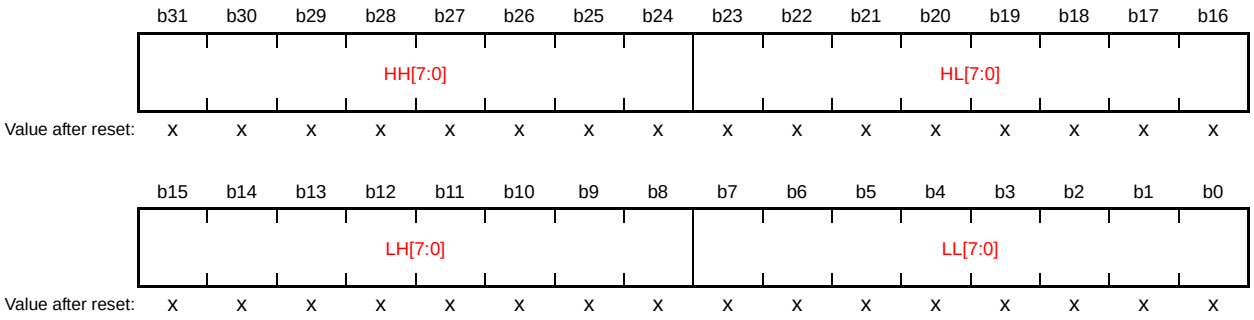


x: Undefined

Bit	Symbol	Bit Name	Description	SD Host R/W	CPU R/W
—	FN1DATAR1	—	Function1 data register 1	R/W	R/W

After correction

Address(es): SDSI.FN1DATAR10 to SDSI.FN1DATAR163 0009 5800h to 0009 58FFh



x: Undefined

Bit	Symbol	Bit Name	Description	SD Host R/W	CPU R/W
b7 to b0	LL[7:0]	—	Function1 data register 1. This register can be accessed in 32- or 8-bit units. The address offsets for every bytes are +0 for the HH[7:0] bits, +1 for the HL[7:0] bits, +2 for the LH[7:0] bits, and +3 for the LL[7:0] bits.	R/W	R/W
b15 to b8	LH[7:0]	—		R/W	R/W
b23 to b16	HL[7:0]	—		R/W	R/W
b31 to b24	HH[7:0]	—		R/W	R/W

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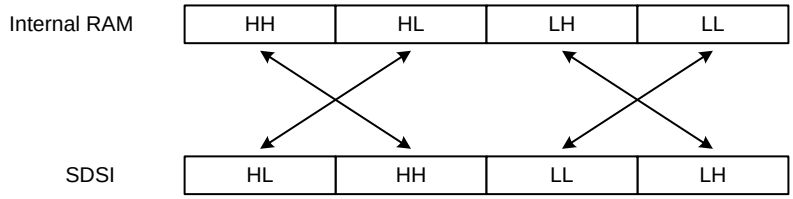
The following figure is added to section 44.4.2, SD Data Format.

After correction

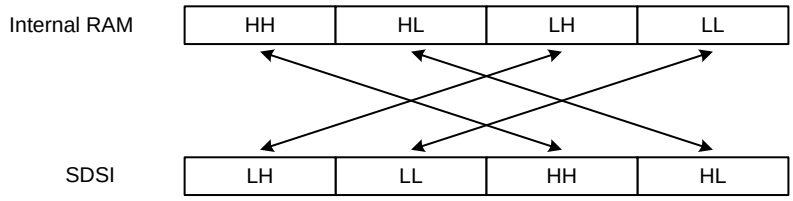
44.4.2 SD Data Format

Figure 44.2 shows the data format when selecting the data swapping.

(1) When swapping the byte position (DMACR2.DMARSWAP[1:0] = 10b, DMACR2.DMAWSWAP[1:0] = 10b)



(2) When swapping the word position (DMACR2.DMARSWAP[1:0] = 01b, DMACR2.DMAWSWAP[1:0] = 01b)



(3) When swapping the byte and word positions (SDSICR2.RSWAP = 1, SDSICR2.WSWAP = 1, DMACR2.DMARSWAP[1:0] = 00b, DMACR2.DMAWSWAP[1:0] = 00b)

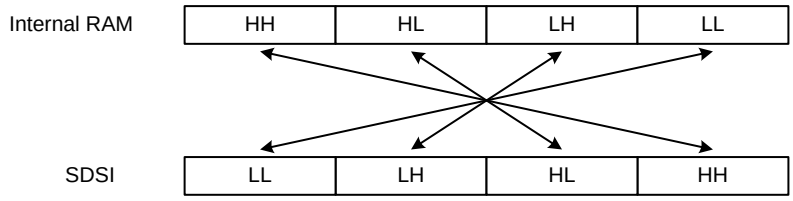


Figure 44.2 Data Formats When Swapping the Data

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The descriptions of (1) When FN1 Data Register is used in section 44.4.2, SD Data Format are modified as follows.

Before correction

(1) When FN1 Data Register is used

Figure 44.2 shows how data are stored in the FN1DATAR registers 1 to 5 (FN1DATAR1 to FN1DATAR5) and the order of transfer of the data over the SD bus when these registers are used for data transfer. Consider the order of the transfer over the SD bus in access to the FN1DATAR registers. These registers can be accessed in byte units by swapping the data.

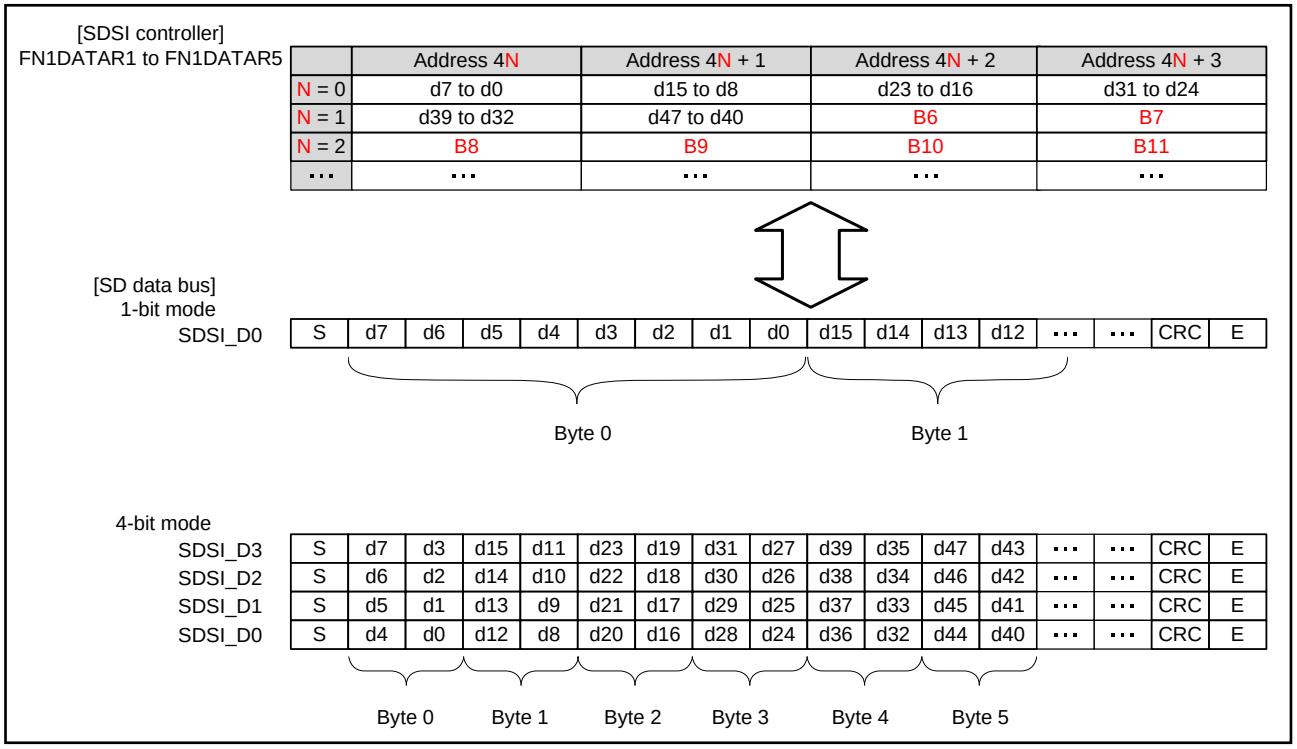

Figure 44.2 Data Format

After correction

(1) When FN1 Data Register is used

Figure 44.3 and Figure 44.4 show how data are stored in the FN1DATAR registers 1 to 5 (FN1DATAR1 to FN1DATAR5) and the order of transfer of the data over the SD bus when these registers are used for data transfer. Consider the order of the transfer over the SD bus in access to the FN1DATAR registers. These registers can be accessed with swapping the byte and word positions of the data.

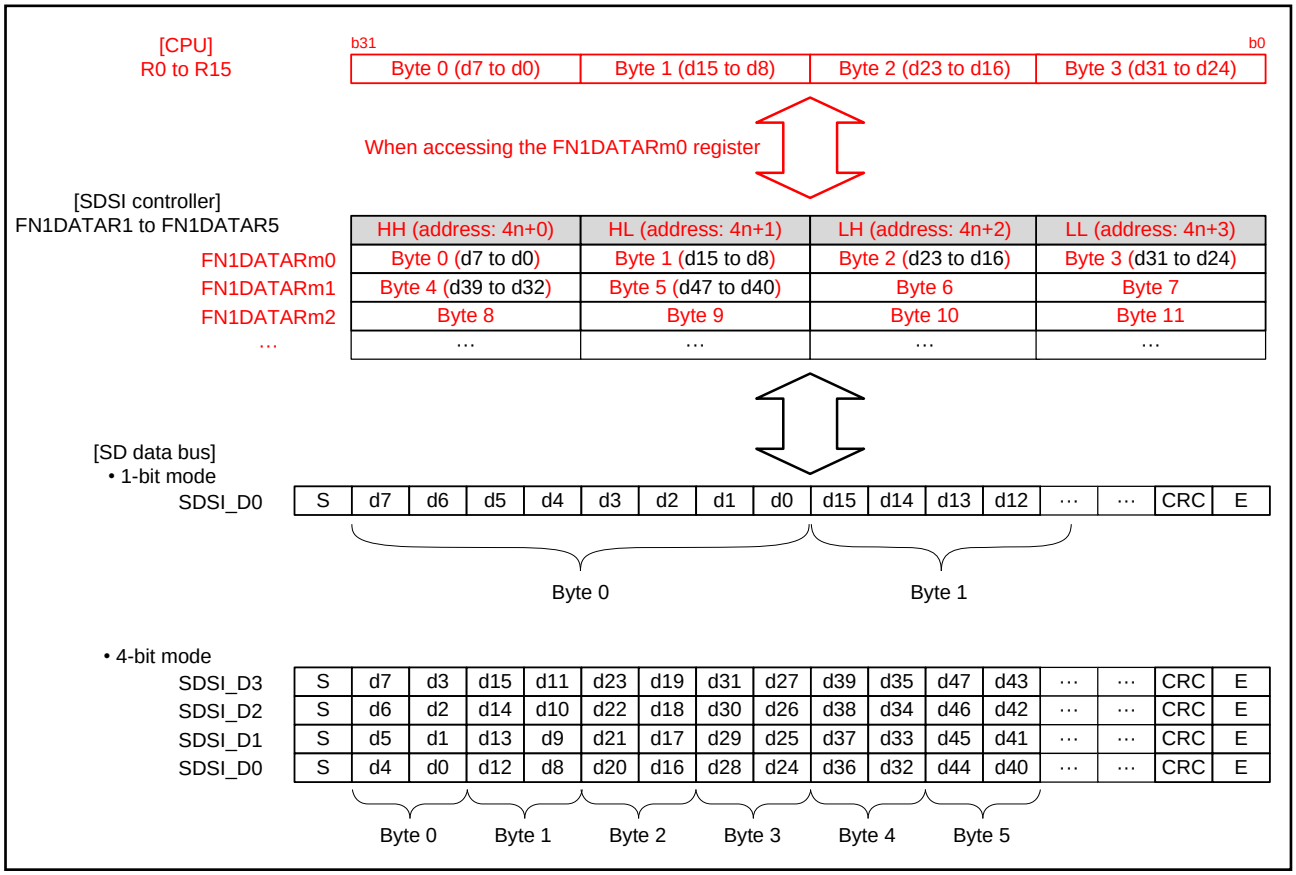

Figure 44.3 Data Format (Without Data Swapping (the SDSICR2.RSWAP and WSWAP bits are 0))

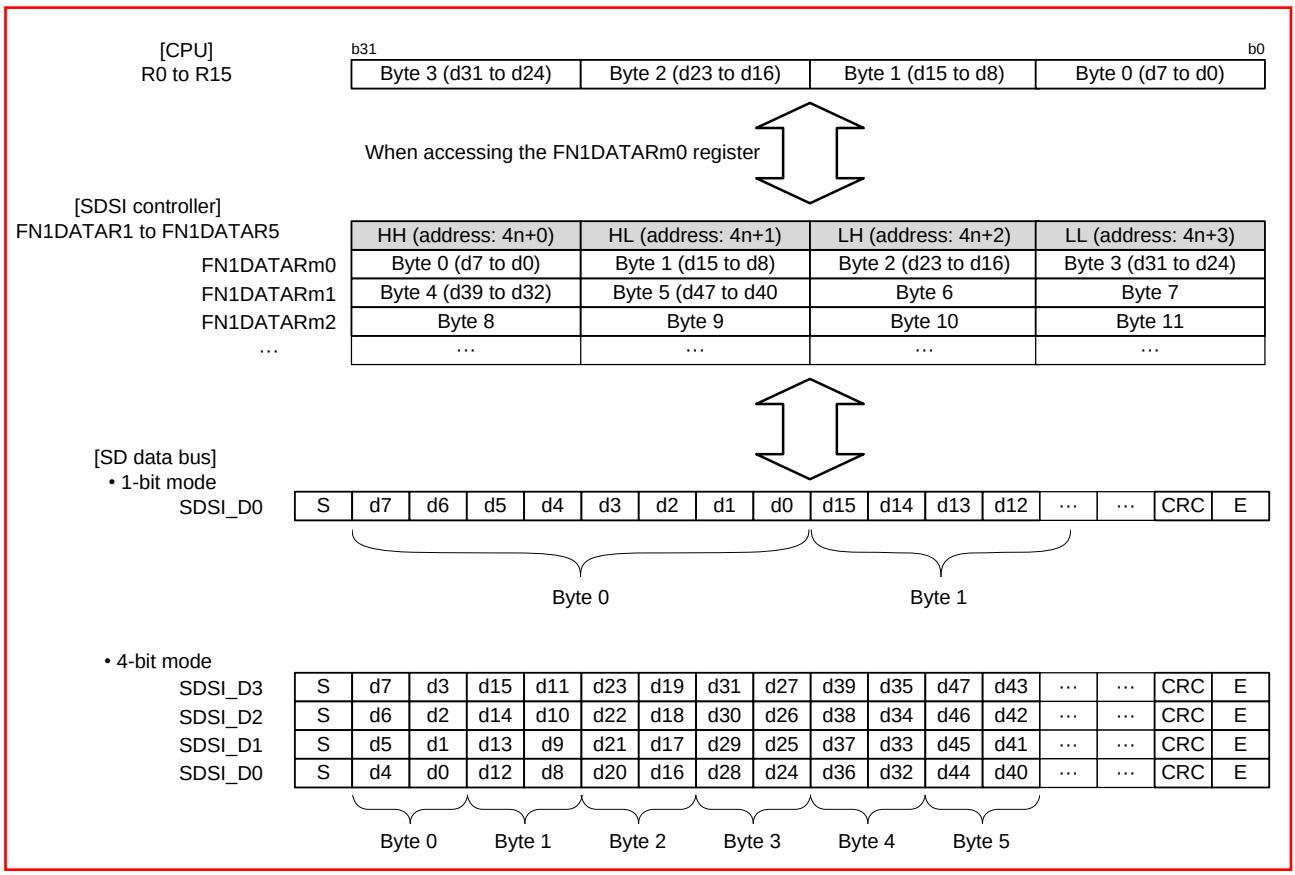

Figure 44.4 Data Format (Swapping the Byte and Word Positions (the SDSICR2.RSWAP and WSWAP bits are 1))

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The descriptions of (2) When DMA transfer is used in section 44.4.2, SD Data Format are modified as follows.

Before correction

(2) When DMA transfer is used

Figure 44.3 shows the stored data of the internal RAM and order of the data transfer on the SD bus when data transfer with DMA transfer is performed.

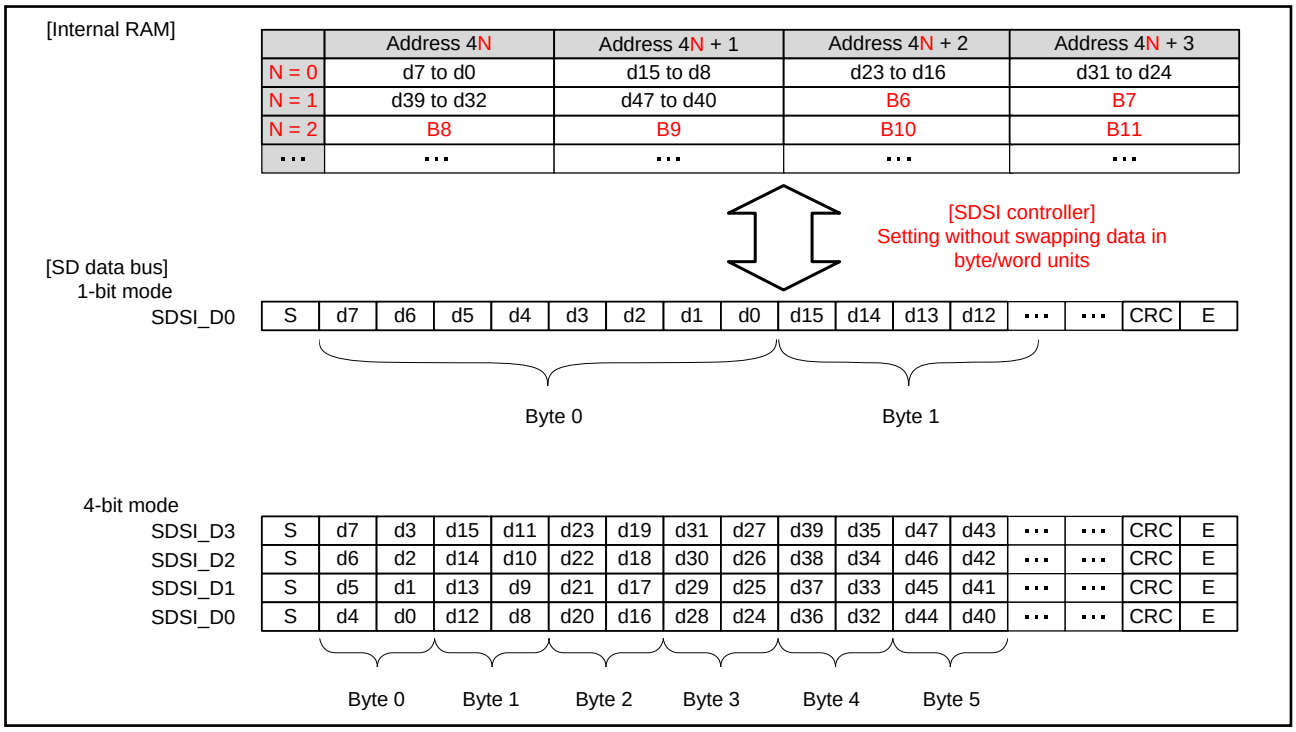

Figure 44.3 Data Format (Without Swapping Data in Byte/Word units)

Figure 44.4 shows the order for the data transfer on the bus for swapping data in byte/word units.

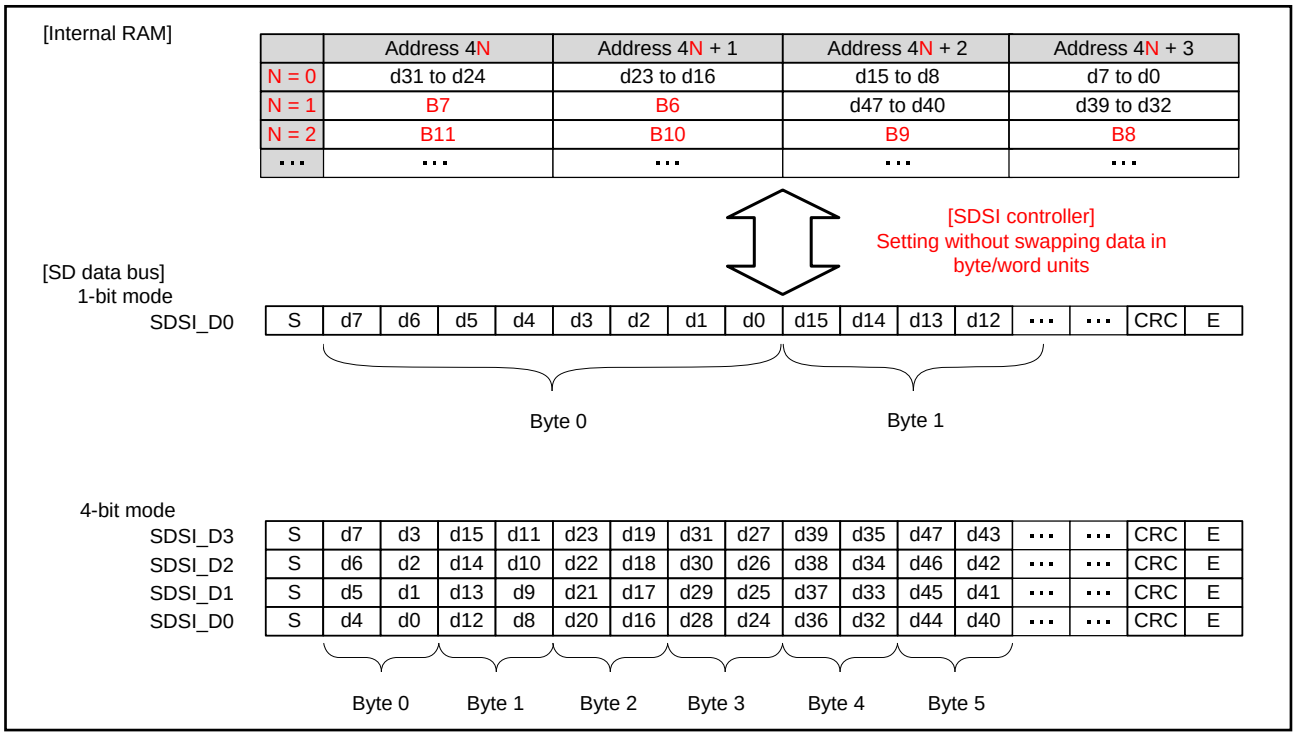

Figure 44.4 Data Format (with Swapping Data in Byte/Word Units)

After correction

(2) When DMA transfer is used

Figure 44.5 to Figure 44.8 show the stored data of the internal RAM and order of the data transfer on the SD bus when data transfer using DMA transfer is performed.

[Internal RAM]

		HH	HL	LH	LL
Little endian		Address: 4n+3	Address: 4n+2	Address: 4n+1	Address: 4n
Big endian		Address: 4n	Address: 4n+1	Address: 4n+2	Address: 4n+3
n	0	Byte 0 (d7 to d0)	Byte 1 (d15 to d8)	Byte 2 (d23 to d16)	Byte 3 (d31 to d24)
	1	Byte 4 (d39 to d32)	Byte 5 (d47 to d40)	Byte 6	Byte 7
	2	Byte 8	Byte 9	Byte 10	Byte 11
	…	…	…	…	…

[SD data bus]

• 1-bit mode

SDSI_D0	S	d7	d6	d5	d4	d3	d2	d1	d0	d15	d14	d13	d12	…	…	CRC	E
		Byte 0								Byte 1							

• 4-bit mode

SDSI_D3	S	d7	d3	d15	d11	d23	d19	d31	d27	d39	d35	d47	d43	…	…	CRC	E
SDSI_D2	S	d6	d2	d14	d10	d22	d18	d30	d26	d38	d34	d46	d42	…	…	CRC	E
SDSI_D1	S	d5	d1	d13	d9	d21	d17	d29	d25	d37	d33	d45	d41	…	…	CRC	E
SDSI_D0	S	d4	d0	d12	d8	d20	d16	d28	d24	d36	d32	d44	d40	…	…	CRC	E
		Byte 0		Byte 1		Byte 2		Byte 3		Byte 4		Byte 5					

Figure 44.5 Data Format (Without Data Swapping)

[Internal RAM]

		HH	HL	LH	LL
Little endian		Address: 4n+3	Address: 4n+2	Address: 4n+1	Address: 4n
Big endian		Address: 4n	Address: 4n+1	Address: 4n+2	Address: 4n+3
n	0	Byte 3 (d31 to d24)	Byte 2 (d23 to d16)	Byte 1 (d15 to d8)	Byte 0 (d7 to d0)
	1	Byte 7	Byte 6	Byte 5 (d47 to d40)	Byte 4 (d39 to d32)
	2	Byte 11	Byte 10	Byte 9	Byte 8
	…	…	…	…	…

[SD data bus]

• 1-bit mode

SDSI_D0	S	d7	d6	d5	d4	d3	d2	d1	d0	d15	d14	d13	d12	…	…	CRC	E
		Byte 0								Byte 1							

• 4-bit mode

SDSI_D3	S	d7	d3	d15	d11	d23	d19	d31	d27	d39	d35	d47	d43	…	…	CRC	E
SDSI_D2	S	d6	d2	d14	d10	d22	d18	d30	d26	d38	d34	d46	d42	…	…	CRC	E
SDSI_D1	S	d5	d1	d13	d9	d21	d17	d29	d25	d37	d33	d45	d41	…	…	CRC	E
SDSI_D0	S	d4	d0	d12	d8	d20	d16	d28	d24	d36	d32	d44	d40	…	…	CRC	E
		Byte 0		Byte 1		Byte 2		Byte 3		Byte 4		Byte 5					

Figure 44.6 Data Format (Swapping the Byte and Word Positions)

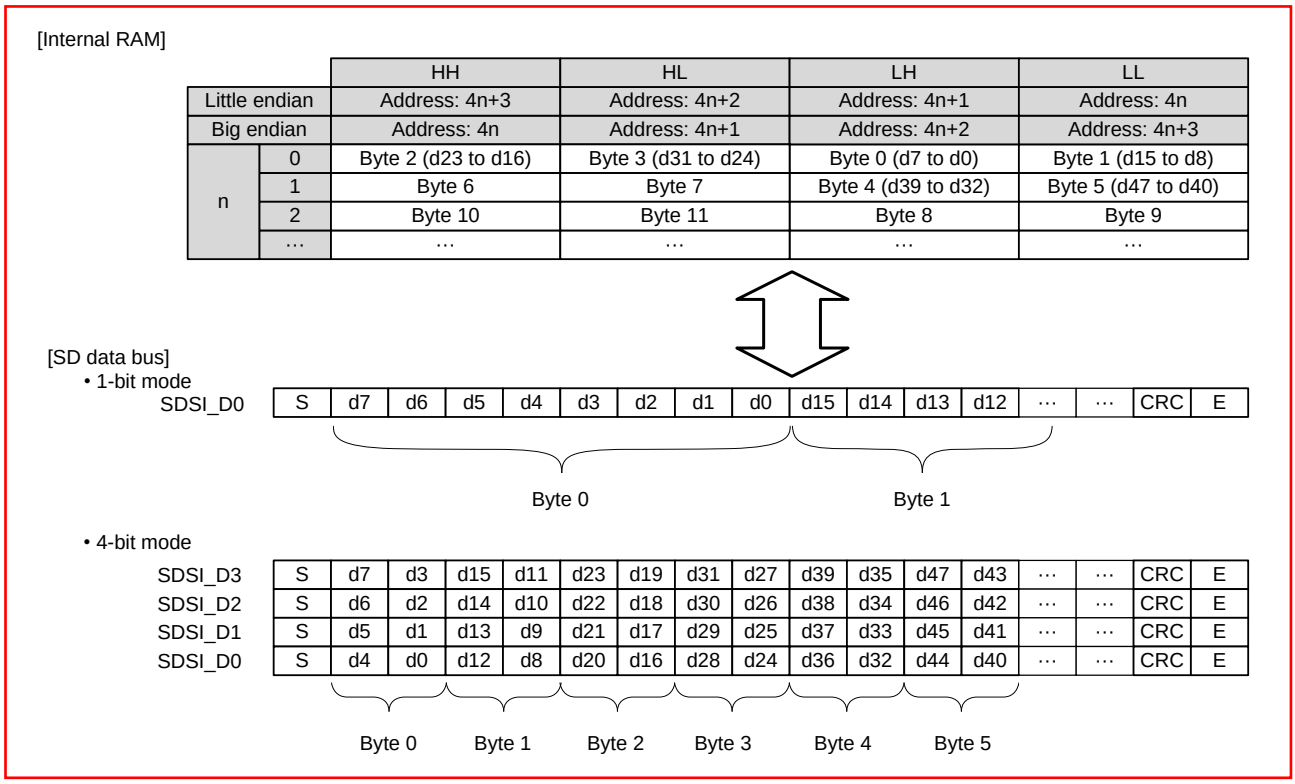

Figure 44.7 Data Format (Swapping the Word Position)

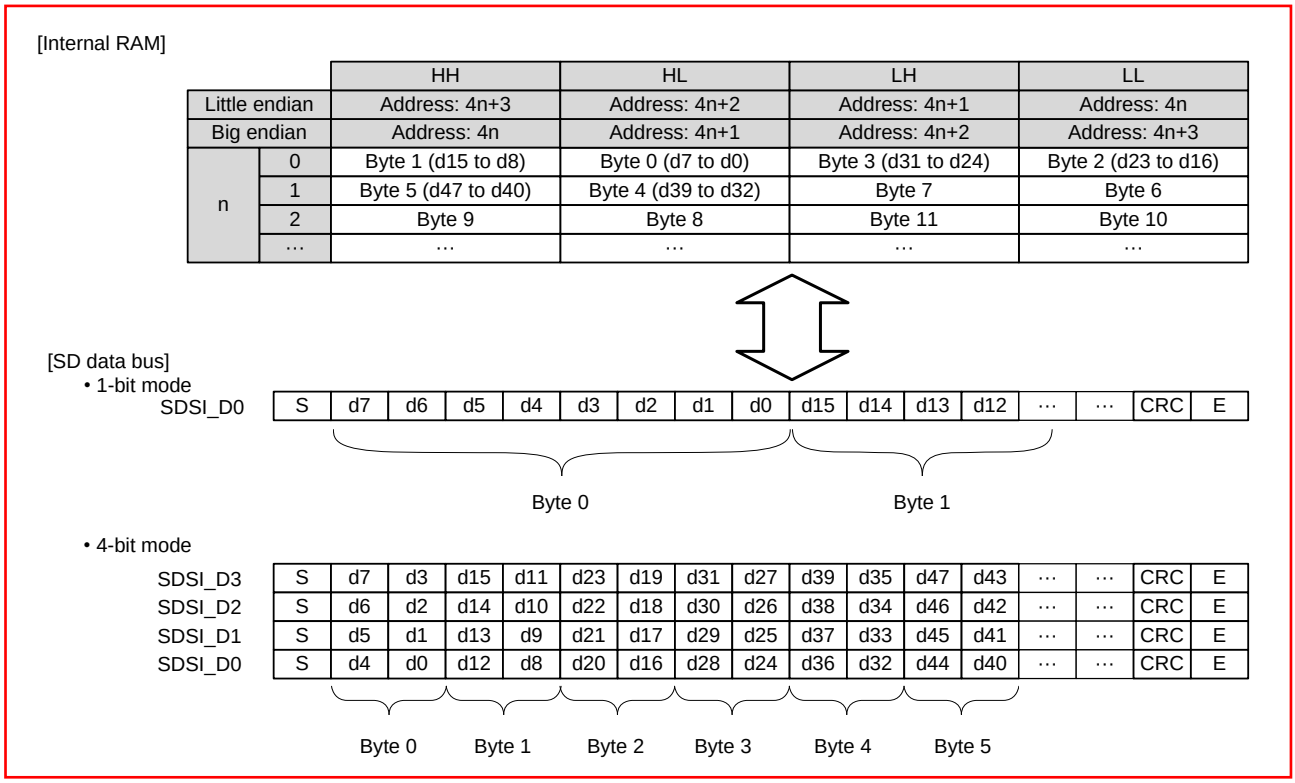

Figure 44.8 Data Format (Swapping the Byte Position)

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The following description is added after section 50.6.7, Notes on Canceling Software Standby Mode.

After correction

50.6.8 Pin Setting When Using the 12-bit A/D Converter

When using the 12-bit A/D converter unit 0, do not use the P40 to P47, P03, P05, and P07 pins as output pins. We also recommend not using the P00 to P02, P90 to P93, PD0 to PD7, and PE0 to PE7 pins as output pins. If any of the P00 to P02, P90 to P93, PD0 to PD7, and PE0 to PE7 pins is used for an output pin, perform A/D conversion several times, eliminate the maximum and minimum values, and obtain the average of the other results.

When using the 12-bit A/D converter unit 1, we recommend not using the P00 to P02, P90 to P93, PD0 to PD7, and PE0 to PE7 pins as output pins. If any of the P00 to P02, P90 to P93, PD0 to PD7, and PE0 to PE7 pins is used for an output pins, perform A/D conversion several times, eliminate the maximum and minimum values, and obtain the average of the other results.

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The Analog power supply current in Table 57.6, DC Characteristics (4) is corrected as follows.

Before correction

Item		Symbol	Min.	Typ.	Max.	Unit	Test Conditions
Analog power supply current*1	Omitted						
	A/D, D/A converter, temperature sensor in standby mode (all units)	AI_{CC}	—	1.4	4.5	µA	IAVCC0 + IAVCC1
Reference power supply current	During 12-bit A/D conversion (unit 0)	AI_{REFH}	—	25	40	µA	IVREFH0
	Waiting for 12-bit A/D conversion (unit 0)		—	0.07	0.4	µA	IVREFH0
	12-bit A/D converter in standby mode (unit 0)		—	0.07	0.2	µA	IVREFH0
Omitted							

After correction

Item		Symbol	Min.	Typ.	Max.	Unit	Test Conditions
Analog power supply current*1	Omitted						
	A/D, D/A converter, temperature sensor in standby mode (all units)	AI_{CC}	—	1.4	6.7	µA	IAVCC0 + IAVCC1
Reference power supply current	During 12-bit A/D conversion (unit 0)	AI_{REFH}	—	25	40	µA	IVREFH0
	Waiting for 12-bit A/D conversion (unit 0)		—	0.07	0.5	µA	IVREFH0
	12-bit A/D converter in standby mode (unit 0)		—	0.07	0.4	µA	IVREFH0
Omitted							

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The characteristic of sub-clock oscillator operating in Table 57.19, Timing of Recovery from Low Power Consumption Modes (1) is corrected as follows.

Before correction

Item		Symbol	Min.	Typ.	Max.		Unit	Test Conditions
					$t_{SBYOSCWT}$*2	t_{SBYSEQ}*3		
Recovery time after cancellation of software standby mode*1	Omitted							
	Sub-clock oscillator operating	t_{SBYSC}	—	—	{(SSTS[7:0] bits × 6384) + 13} / 0.216 + 10 / fFCLK	100 µs + 4 / fl_{CLK} + 2n / f_{SUB}	µs	Figure 57.12
	Omitted							

After correction

Item		Symbol	Min.	Typ.	Max.		Unit	Test Conditions
					$t_{SBYOSCWT}$*2	t_{SBYSEQ}*3		
Recovery time after cancellation of software standby mode*1	Omitted							
	Sub-clock oscillator operating	t_{SBYSC}	—	—	{(SSTS[7:0] bits × 16384) + 13} / 0.216 + 10 / f_{FCLK}	100 µs + 4 / f_{ICLK} + 2n / f_{SUB}	µs	Figure 57.12
	Omitted							

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The characteristics in Table 57.33, RSPI Timing are corrected as follows.

Before correction

Item			Symbol	Min.*1	Max.*1	Unit*1	Test Conditions
RSPI	Omitted						
	RSPCK clock high pulse width	Master	t_{SPCKWH}	(t_{SPcyc} – t_{SCKr} – t_{SCKf}) / 2 – 3	—	ns	
		Slave		(t_{SPcyc} – t_{SCKr} – t_{SCKf}) / 2	—		
	RSPCK clock low pulse width	Master	t_{SPCKWL}	(t_{SPcyc} – t_{SCKr} – t_{SCKf}) / 2 – 3	—	ns	
		Slave		(t_{SPcyc} – t_{SCKr} – t_{SCKf}) / 2	—		
	Omitted						
	Successive transmission delay time	Master	t_{TD}	t_{SPcyc} + 2 × t_{PAcyc}	8 × t_{SPcyc} + 2 × t_{PAcyc}	ns	
		Slave		4 × t_{PAcyc}	—		
	Omitted						
	Slave access time		t_{SA}	—	2 × t_{PAcyc} + 28	t_{PAcyc}	Figure 57.49, Figure 57.50
	Slave output release time		t_{REL}	—	2 × t_{PAcyc} + 28	t_{PAcyc}	

After correction

Item			Symbol	Min.*1	Max.*1	Unit*1	Test Conditions
RSPI	Omitted						
	RSPCK clock high pulse width	Master	t_{SPCKWH}	$(t_{SPcyc} - t_{SPCKr} - t_{SPCKf}) / 2 - 3$	—	ns	
		Slave		$(t_{SPcyc} - t_{SPCKr} - t_{SPCKf}) / 2$	—		
	RSPCK clock low pulse width	Master	t_{SPCKWL}	$(t_{SPcyc} - t_{SPCKr} - t_{SPCKf}) / 2 - 3$	—	ns	
		Slave		$(t_{SPcyc} - t_{SPCKr} - t_{SPCKf}) / 2$	—		
	Omitted						
	Successive transmission delay time	Master	t_{TD}	$t_{SPcyc} + 2 \times t_{PAcyc}$	$8 \times t_{SPcyc} + 2 \times t_{PAcyc}$	ns	
		Slave		$6 \times t_{PAcyc}$	—		
	Omitted						
	Slave access time		t_{SA}	—	$2 \times t_{PAcyc} + 28$	ns	Figure 57.49, Figure 57.50
	Slave output release time		t_{REL}	—	$2 \times t_{PAcyc} + 28$	ns	

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