To our customers,

Old Company Name in Catalogs and Other Documents

On April 1st, 2010, NEC Electronics Corporation merged with Renesas Technology Corporation, and Renesas Electronics Corporation took over all the business of both companies. Therefore, although the old company name remains in this document, it is a valid Renesas Electronics document. We appreciate your understanding.

Renesas Electronics website: http://www.renesas.com

April 1st, 2010
Renesas Electronics Corporation

Issued by: Renesas Electronics Corporation (http://www.renesas.com)

Send any inquiries to http://www.renesas.com/inquiry.

To all our customers

Regarding the change of names mentioned in the document, such as Hitachi Electric and Hitachi XX, to Renesas Technology Corp.

The semiconductor operations of Mitsubishi Electric and Hitachi were transferred to Renesas Technology Corporation on April 1st 2003. These operations include microcomputer, logic, analog and discrete devices, and memory chips other than DRAMs (flash memory, SRAMs etc.) Accordingly, although Hitachi, Hitachi, Ltd., Hitachi Semiconductors, and other Hitachi brand names are mentioned in the document, these names have in fact all been changed to Renesas Technology Corp. Thank you for your understanding. Except for our corporate trademark, logo and corporate statement, no changes whatsoever have been made to the contents of the document, and these changes do not constitute any alteration to the contents of the document itself.

Renesas Technology Home Page: http://www.renesas.com

Renesas Technology Corp.
Customer Support Dept.
April 1, 2003

HITACHI SEMICONDUCTOR TECHNICAL UPDATE

DATE	26th, August, 1998	No.	TN-PSC-335A/E
THEME	The supplement of Usage Note when underrun occurs of HD64572 SCA-II User's Manual .		
CLASSIFICATION	☐ Spec. change ☐ Supplement of Documents ☐ Limitation on Use ■ Correction		
PRODUCT NAME	HD64572FL33 , HD64572AFL33	Lot No.etc.	All lots
REFERENCE DOCUMENTS	———	Effective Date	forever
		From	Now

There are some insufficiency of Usage Notes when underrun occurs in HD64572 SCA-II User's Manual, please make correct it described as below.
Please, take notice of this HITACHI SEMICONDUCTOR TECHNICAL UPDATE.

Section 5 Multiprotocol Serial Communication Interface (MSCI)

5.3 Operation

5.3.2 Byte Synchronous Mode

Error Checking

- Underrun error ··· page 295

(Current)

Notes:1. Underrun is judged to have occurred when the transmit shift register and transmit buffer are both empty, and an end of message command has not been issued.
2. If an underrun error occurs while UDRNC or CRCC0 is 0, the MSCI enters the idle state directly without sending the CRC code.

(Corrected)

Notes:1. Underrun is judged to have occurred when the transmit shift register and transmit buffer are both empty, and an end of message command has not been issued.
2. If an underrun error occurs while UDRNC or CRCC0 is 0, the MSCI enters the idle state directly without sending the CRC code.

Usage Note:

Data (1 to 4 bytes) written into the transmit buffer by the MPU or DMAC at the same time as underrun occurs may be left in the transmit buffer, and not transmitted, depending on the write timing. When data is next written to the transmit buffer by the MPU after clearing the UDRN bit of Status Register 1 (ST1), or data is transferred by the DMAC, the remaining data will be added at the head of the next frame or the remaining data and next frame combine into one frame, and transmitted.
To prevent this, TXINTE bit of Interrupt Enable Register 0 (IE0) and UDRNE bit of Interrupt Enable Register 1 (IE1) set to 1. If an interrupt request is generated by the underrun occurs, please issue the command as following.

(1) TX disable β command.
(2) Transmit Buffer Data Number Register (TBN) to check the number of data bytes in the transmit buffer.
(3) TX buffer clear command.
(4) TX enable command.

5.3.3 Bit Synchronous Mode

Error Checking

- Underrun error ··· page 303

(Current)

Usage Note:

Data (1 to 4 bytes) written into the transmit buffer by the MPU or DMAC at the same time as underrun occurs may be left in the transmit buffer, and not transmitted, depending on the write timing. When data is next written to the transmit buffer by the MPU after clearing the UDRN bit, or data is transferred by the DMAC, the remaining data will be added at the head of the next frame, and transmitted.

To prevent this, use TBN to check the number of data bytes in the transmit buffer after underrun occurs. If there is data left in the transmit buffer, issue a transmit buffer clear command.

(Corrected)

Usage Note:

Data (1 to 4 bytes) written into the transmit buffer by the MPU or DMAC at the same time as underrun occurs may be left in the transmit buffer, and not transmitted, depending on the write timing. When data is next written to the transmit buffer by the MPU after clearing the UDRN bit, or data is transferred by the DMAC, the remaining data will be added at the head of the next frame or the remaining data and next frame combine into one frame, and transmitted.

To prevent this, TXINTE bit of Interrupt Enable Register 0 (IE0) and UDRNE bit of Interrupt Enable Register 1 (IE1) set to 1. If an interrupt request is generated by the underrun occurs, please issue the command as following.

(1) TX disable B command.

(2) Transmit Buffer Data Number Register (TBN) to check the number of data bytes in the transmit buffer.

(3) TX buffer clear command.

(4) TX enable command.

5.3.4 Transparent Mode

Error Checking

- Underrun error ··· page 309

(Current)

An underrun error occurs if the SYNCO pin is low and the transmit buffer is empty.

When underrun is detected, the UDRN bit is set to 1 in status register 1 (ST1), and the TXRDY bit is cleared to 0 in status register 0 (ST0). When the UDRN bit is set to 1, an interrupt request is generated, if enabled. The UDRN bit is cleared to 0 only when a 1 is written to the bit position or ST1 is reset.

(Corrected)

An underrun error occurs if the $\overline{\text{SYNCO}}$ pin is low and the transmit buffer is empty.

When underrun is detected, the UDRN bit is set to 1 in status register 1 (ST1), and the TXRDY bit is cleared to 0 in status register 0 (ST0). When the UDRN bit is set to 1, an interrupt request is generated, if enabled. The UDRN bit is cleared to 0 only when a 1 is written to the bit position or ST1 is reset.

Usage Note:

Data (1 to 4 bytes) written into the transmit buffer by the MPU or DMAC at the same time as underrun occurs may be left in the transmit buffer, and not transmitted, depending on the write timing. When data is next written to the transmit buffer by the MPU after clearing the UDRN bit of Status Register 1 (ST1), or data is transferred by the DMAC, the remaining data will be added at the head of the next frame or the remaining data and next frame combine into one frame, and transmitted.

To prevent this, TXINTE bit of Interrupt Enable Register 0 (IE0) and UDRNE bit of Interrupt Enable Register 1 (IE1) set to 1. If an interrupt request is generated by the underrun occurs, please issue the command as following.

(1) TX disable B command.

(2) Transmit Buffer Data Number Register (TBN) to check the number of data bytes in the transmit buffer.

(3) TX buffer clear command.

(4) TX enable command.