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RENESAS TECHNICAL UPDATE

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Product Category	MPU/MCU		Document No.	TN-SH7-A805A/E	Rev.	1.00
Title	SH7786 Pin States		Information Category	Technical Notification		
Applicable Product	SH7786 Group	Lot No. All lots	Reference Document	SH7786 Group User's Manual: Hardware Rev.1.00 Nov. 30, 2010 (REJ09B0501-0100)		

Description of the pin states is newly added to SH7786 Group Hardware User's Manual as follows.

[Description]

Table 1 Pin States

#: Low active or inverted-signal of differential signal-pair

Pin Name (LSI level)	Signal Name (Module level)	Module	I/O	Reset		Sleep/ Light Sleep	Module Standby	Bus Release
				Power-on	Manual			
A[25:0]	A[25:0]	LBSC	O	PZ	K	K	-	PZ
D[31:8]	D[31:8]	LBSC	IO	Z	K	K	-	Z
D[7:0]/FD[7:0]	D[7:0] (default)	LBSC	IO	Z	K	K	-	Z
	FD[7:0]	FLCTL	IO	Z	K	K	-	Z
CS0#	CS0#	LBSC	O	PZ	K	K	-	PZ
CS1#/A26	CS1#/A26	LBSC	O	PZ	K	K	-	PZ
CS[6:2]#	CS[6:2]#	LBSC	O	PZ	K	K	-	PZ
RD#/FRAME#/FRE#	RD#/FRAME#	LBSC	O	PZ	K	K	-	PZ
	FRE#	FLCTL	O	PZ	K	K	-	PZ
R/W#	R/W#	LBSC	O	PZ	K	K	-	PZ
BS#	BS#	LBSC	O	PZ	K	K	-	PZ
RDY#	RDY#	LBSC	I	PI	K	K	-	I
WE0#/REG#	WE0#/REG#	LBSC	O	PZ	K	K	-	PZ
WE1#/FWE#	WE1#/FWE#	LBSC	O	PZ	K	K	-	PZ
	FWE#	FLCTL	O	PZ	K	K	-	PZ
WE2#/IORD#	WE2#/IORD#	LBSC	O	PZ	K	K	-	PZ
WE3#/IOWR#	WE3#/IOWR#	LBSC	O	PZ	K	K	-	PZ
CLKOUTENB	CLKOUTENB	CPG	O	H	K	K	-	K
CLKOUT	CLKOUT	CPG	O	O	K	K	-	K
PRESET#	PRESET#	RESET	I	I	I	I	-	I
NMI	NMI	INTC	I	PI	K	K	-	K
IRL[3:0]#	IRL[3:0]#	INTC	I	PI	K	K	-	K
DR0/ETH_TXD0	Port A0 (default)	GPIO	IO	PI	K	K	-	K
	DR0	DU	O	-	O	O	O	O
	ETH_TXD0	Ether	O	-	O	O	O	O

Pin Name (LSI level)	Signal Name (Module level)	Module	I/O	Reset		Sleep/ Light Sleep	Module Standby	Bus Release
				Power-on	Manual			
DR1/ETH_TXD1	Port A1 (default)	GPIO	IO	PI	K	K	-	K
	DR1	DU	O	-	O	O	O	O
	ETH_TXD1	Ether	O	-	O	O	O	O
DR2/ETH_TXD2	Port A2 (default)	GPIO	IO	PI	K	K	-	K
	DR2	DU	O	-	O	O	O	O
	ETH_TXD2	Ether	O	-	O	O	O	O
DR3/ETH_TXD3	Port A3 (default)	GPIO	IO	PI	K	K	-	K
	DR3	DU	O	-	O	O	O	O
	ETH_TXD3	Ether	O	-	O	O	O	O
DR4/ETH_TX_EN	Port A4 (default)	GPIO	IO	PI	K	K	-	K
	DR4	DU	O	-	O	O	O	O
	ETH_TX_EN	Ether	O	-	O	O	O	O
DR5/ETH_TX_ER	Port A5 (default)	GPIO	IO	PI	K	K	-	K
	DR5	DU	O	-	O	O	O	O
	ETH_TX_ER	Ether	O	-	O	O	O	O
DISP/ETH_LINK	Port A6 (default)	GPIO	IO	PI	K	K	-	K
	DISP	DU	O	-	O	O	O	O
	ETH_LINK	Ether	I	-	I	I	I	I
CDE/ETH_MAGIC	Port A7 (default)	GPIO	IO	PI	K	K	-	K
	CDE	DU	O	-	O	O	O	O
	ETH_MAGIC	Ether	O	-	O	O	O	O
DG0/ETH_CRS	Port B0 (default)	GPIO	IO	PI	K	K	-	K
	DG0	DU	O	-	O	O	O	O
	ETH_CRS	Ether	I	-	I	I	I	I
DG1/ETH_TX_CLK	Port B1 (default)	GPIO	IO	PI	K	K	-	K
	DG1	DU	O	-	O	O	O	O
	ETH_TX_CLK	Ether	I	-	I	I	I	I
DG2/ETH_COL	Port B2 (default)	GPIO	IO	PI	K	K	-	K
	DG2	DU	O	-	O	O	O	O
	ETH_COL	Ether	I	-	I	I	I	I
DG3/ETH_MDC	Port B3 (default)	GPIO	IO	PI	K	K	-	K
	DG3	DU	O	-	O	O	O	O
	ETH_MDC	Ether	O	-	O	O	O	O
DG4/ETH_RX_CLK	Port B4 (default)	GPIO	IO	PI	K	K	-	K
	DG4	DU	O	-	O	O	O	O
	ETH_RX_CLK	Ether	I	-	I	I	I	I
DG5/ETH_MDIO	Port B5 (default)	GPIO	IO	PI	K	K	-	K
	DG5	DU	O	-	O	O	O	O
	ETH_MDIO	Ether	IO	-	K	K	K	K
ODDF/HSPI_CS#	Port B6 (default)	GPIO	IO	PI	K	K	-	K
	ODDF	DU	IO	-	K	K	K	K
	HSPI_CS#	HSPI	IO	-	Z	K	K	K
VSYNC#/HSPI_CLK	Port B7 (default)	GPIO	IO	PI	K	K	-	K
	VSYNC#	DU	IO	-	K	K	K	K
	HSPI_CLK	HSPI	IO	-	Z	K	K	K
DB0/ETH_RX_ER	Port C0 (default)	GPIO	IO	PI	K	K	-	K
	DB0	DU	O	-	O	O	O	O
	ETH_RX_ER	Ether	I	-	I	I	I	I

Pin Name (LSI level)	Signal Name (Module level)	Module	I/O	Reset		Sleep/ Light Sleep	Module Standby	Bus Release
				Power-on	Manual			
DB1/ETH_RX_DV	Port C1 (default)	GPIO	IO	PI	K	K	-	K
	DB1	DU	O	-	O	O	O	O
	ETH_RX_DV	Ether	I	-	I	I	I	I
DB2/ETH_RXD0	Port C2 (default)	GPIO	IO	PI	K	K	-	K
	DB2	DU	O	-	O	O	O	O
	ETH_RXD0	Ether	I	-	I	I	I	I
DB3/ETH_RXD1	Port C3 (default)	GPIO	IO	PI	K	K	-	K
	DB3	DU	O	-	O	O	O	O
	ETH_RXD1	Ether	I	-	I	I	I	I
DB4/ETH_RXD2	Port C4 (default)	GPIO	IO	PI	K	K	-	K
	DB4	DU	O	-	O	O	O	O
	ETH_RXD2	Ether	I	-	I	I	I	I
DB5/ETH_RXD3	Port C5 (default)	GPIO	IO	PI	K	K	-	K
	DB5	DU	O	-	O	O	O	O
	ETH_RXD3	Ether	I	-	I	I	I	I
HSYNC#/HSPI_TX	Port C6 (default)	GPIO	IO	PI	K	K	-	K
	HSYNC#	DU	IO	-	K	K	K	K
	HSPI_TX	HSPI	O	-	O	O	O	O
DCLKIN/HSPI_RX	Port C7 (default)	GPIO	IO	PI	K	K	-	K
	DCLKIN	DU	I	-	I	I	I	I
	HSPI_RX	HSPI	I	-	I	I	I	I
DREQ0#/USB_OVC0	Port D0	GPIO	IO	-	K	K	-	K
	DREQ0#	DMAC	I	-	K	K	K	K
	USB_OVC0 (default)	USB	I	PI	K	K	K	K
DREQ1#/BREQ#/USB_OVC1	Port D1	GPIO	IO	-	K	K	-	K
	DREQ1#	DMAC	I	-	K	K	K	K
	BREQ#	LBSC	I	-	K	K	-	K
	USB_OVC1 (default)	USB	I	PI	K	K	K	K
DACK0#/FCLE	Port D2	GPIO	IO	-	K	K	-	K
	DACK0#	DMAC	O	-	O	O	O	O
	FCLE (default)	FLCTL	O	PZ	K	K	-	K
DACK1#/BACK#/FALE	Port D3	GPIO	IO	-	K	K	-	K
	DACK1#	DMAC	O	-	O	O	O	O
	BACK#	LBSC	O	-	K	K	-	K
	FALE (default)	FLCTL	O	PZ	K	K	-	K
SCIF1_TXD	Port D4 (default)	GPIO	IO	PI	K	K	-	K
	SCIF1_TXD	SCIF	O	-	O	O	O	O
SCIF1_RXD	Port D5 (default)	GPIO	IO	PI	K	K	-	K
	SCIF1_RXD	SCIF	I	-	I	I	I	I
SCIF1_SCK	Port D6 (default)	GPIO	IO	PI	K	K	-	K
	SCIF1_SCK	SCIF	IO	-	K	K	K	K
DCLKOUT	Port D7 (default)	GPIO	IO	PI	K	K	-	K
	DCLKOUT	DU	O	-	O	O	O	O
USB_PENC0	Port E6	GPIO	IO	-	K	K	-	K
	USB_PENC0 (default)	USB	O	L	O	O	O	O
USB_PENC1	Port E7	GPIO	IO	-	K	K	-	K
	USB_PENC1 (default)	USB	O	L	O	O	O	O

Pin Name (LSI level)	Signal Name (Module level)	Module	I/O	Reset		Sleep/ Light Sleep	Module Standby	Bus Release
				Power-on	Manual			
HAC0_BITCLK/SSI0_CLK/SDIF1D0	Port F0 (default)	GPIO	IO	PI	K	K	-	K
	HAC0_BITCLK	HAC	I	-	I	I	I	I
	SSI0_CLK	SSI	I	-	I	I	I	I
	SDIF1D0	SDIF	IO	-	K	K	K	K
HAC0_SYNC/SSI0_WS/SDIF1D1	Port F1 (default)	GPIO	IO	PI	K	K	-	K
	HAC0_SYNC	HAC	O	-	O	O	O	O
	SSI0_WS	SSI	IO	-	K	K	K	K
	SDIF1D1	SDIF	IO	-	K	K	K	K
HAC0_SDIN/SSI0_SCK/SDIF1D2	Port F2 (default)	GPIO	IO	PI	K	K	-	K
	HAC0_SDIN	HAC	I	-	I	I	I	I
	SSI0_SCK	SSI	IO	-	K	K	K	K
	SDIF1D2	SDIF	IO	-	K	K	K	K
HAC0_SDOUT/SSI0_SDATA/SDIF1D3	Port F3 (default)	GPIO	IO	PI	K	K	-	K
	HAC0_SDOUT	HAC	O	-	O	O	O	O
	SSI0_SDATA	SSI	IO	-	K	K	K	K
	SDIF1D3	SDIF	IO	-	K	K	K	K
HAC1_BITCLK/SSI1_CLK/SDIF1CLK	Port F4 (default)	GPIO	IO	PI	K	K	-	K
	HAC1_BITCLK	HAC	I	-	I	I	I	I
	SSI1_CLK	SSI	I	-	I	I	I	I
	SDIF1CLK	SDIF	O	-	O	O	O	O
HAC1_SYNC/SSI1_WS/SDIF1WP	Port F5 (default)	GPIO	IO	PI	K	K	-	K
	HAC1_SYNC	HAC	O	-	O	O	O	O
	SSI1_WS	SSI	IO	-	K	K	K	K
	SDIF1WP	SDIF	I	-	I	I	I	I
HAC1_SDIN/SSI1_SCK/SDIF1CD#	Port F6 (default)	GPIO	IO	PI	K	K	-	K
	HAC1_SDIN	HAC	I	-	I	I	I	I
	SSI1_SCK	SSI	IO	-	K	K	K	K
	SDIF1CD#	SDIF	I	-	I	I	I	I
HAC1_SDOUT/SSI1_SDATA/SDIF1CMD	Port F7 (default)	GPIO	IO	PI	K	K	-	K
	HAC1_SDOUT	HAC	O	-	O	O	O	O
	SSI1_SDATA	SSI	IO	-	K	K	K	K
	SDIF1CMD	SDIF	IO	-	K	K	K	K
SCIF3_TXD/HAC_RES#/SSI2_WS	Port G5 (default)	GPIO	IO	PI	K	K	-	K
	SCIF3_TXD	SCIF	O	-	O	O	O	O
	HAC_RES#	HAC	O	-	O	O	O	O
	SSI2_WS	SSI	IO	-	K	K	K	K
SCIF3_RXD/TCLK/SSI2_SCK	Port G6 (default)	GPIO	IO	PI	K	K	-	K
	SCIF3_RXD	SCIF	I	-	I	I	I	I
	TCLK	TMU	I	-	I	I	I	I
	SSI2_SCK	SSI	IO	-	K	K	K	K
SCIF3_SCK/SSI2_SDATA	Port G7 (default)	GPIO	IO	PI	K	K	-	K
	SCIF3_SCK	SCIF	IO	-	K	K	K	K
	SSI2_SDATA	SSI	IO	-	K	K	K	K
MODE0/SCIF0_TXD/IRL4#/SDIF0D0	MODE0 (power-on reset)	RESET	I	I	-	-	-	-
	Port H0 (default)	GPIO	IO	-	K	K	-	K
	SCIF0_TXD	SCIF	O	-	O	O	O	O
	IRL4#	INTC	I	-	K	K	-	K
	SDIF0D0	SDIF	IO	-	K	K	K	K

Pin Name (LSI level)	Signal Name (Module level)	Module	I/O	Reset		Sleep/ Light Sleep	Module Standby	Bus Release
				Power-on	Manual			
MODE1/SCIF0_RXD/IRL5#/SDIF0D1	MODE1 (power-on reset)	RESET	I	I	-	-	-	-
	Port H1 (default)	GPIO	IO	-	K	K	-	K
	SCIF0_RXD	SCIF	I	-	I	I	I	I
	IRL5#	INTC	I	-	K	K	-	K
	SDIF0D1	SDIF	IO	-	K	K	K	K
MODE2/SCIF0_SCK/IRL6#/SDIF0D2	MODE2 (power-on reset)	RESET	I	I	-	-	-	-
	Port H2 (default)	GPIO	IO	-	K	K	-	K
	SCIF0_SCK	SCIF	IO	-	K	K	K	K
	IRL6#	INTC	I	-	K	K	-	K
	SDIF0D2	SDIF	IO	-	K	K	K	K
MODE3/SCIF0_RTS#/IRL7#/SDIF0D3	MODE3 (power-on reset)	RESET	I	I	-	-	-	-
	Port H3 (default)	GPIO	IO	-	K	K	-	K
	SCIF0_RTS#	SCIF	IO	-	K	K	K	K
	IRL7#	INTC	I	-	K	K	-	K
	SDIF0D3	SDIF	IO	-	K	K	K	K
MODE4/SCIF0_CTS#/DREQ2#/SDIF 0CLK	MODE4 (power-on reset)	RESET	I	I	-	-	-	-
	Port H4 (default)	GPIO	IO	-	K	K	-	K
	SCIF0_CTS#	SCIF	IO	-	K	K	K	K
	DREQ2#	DMAC	I	-	K	K	K	K
	SDIF0CLK	SDIF	O	-	O	O	O	O
MODE5/DREQ3#/SDIF0WP	MODE5 (power-on reset)	RESET	I	I	-	-	-	-
	Port H5 (default)	GPIO	IO	-	K	K	-	K
	DREQ3#	DMAC	I	-	K	K	K	K
	SDIF0WP	SDIF	I	-	I	I	I	I
MODE6/DACK2#/SDIF0CD#	MODE6 (power-on reset)	RESET	I	I	-	-	-	-
	Port H6 (default)	GPIO	IO	-	K	K	-	K
	DACK2#	DMAC	O	-	O	O	O	O
	SDIF0CD#	SDIF	I	-	I	I	I	I
MODE7/DACK3#/SDIF0CMD	MODE7 (power-on reset)	RESET	I	I	-	-	-	-
	Port H7 (default)	GPIO	IO	-	K	K	-	K
	DACK3#	DMAC	O	-	O	O	O	O
	SDIF0CMD	SDIF	IO	-	K	K	K	K
MODE8/SCIF4_TXD/DRAK0#/SSI3_SCK/FSE#	MODE8 (power-on reset)	RESET	I	I	-	-	-	-
	Port J1 (default)	GPIO	IO	-	K	K	-	K
	SCIF4_TXD	SCIF	O	-	O	O	O	O
	DRAK0#	DMAC	O	-	O	O	O	O
	SSI3_SCK	SSI	IO	-	K	K	K	K
	FSE#	FLCTL	O	-	O	K	K	K
MODE9/SCIF4_RXD/DRAK1#/SSI3_SDATA	MODE9 (power-on reset)	RESET	I	I	-	-	-	-
	Port J2	GPIO	IO	-	K	K	-	K
	SCIF4_RXD	SCIF	I	-	I	I	I	I
	DRAK1#	DMAC	O	-	O	O	O	O
	SSI3_SDATA	SSI	IO	-	K	K	K	K

Pin Name (LSI level)	Signal Name (Module level)	Module	I/O	Reset		Sleep/ Light Sleep	Module Standby	Bus Release
				Power-on	Manual			
MODE10/SCIF4_SCK/DRAK2#/SSI3_WS	MODE10 (power-on reset)	RESET	I	I	-	-	-	-
	Port J3 (default)	GPIO	IO	-	K	K	-	K
	SCIF4_SCK	SCIF	IO	-	K	K	K	K
	DRAK2#	DMAC	O	-	O	O	O	O
	SSI3_WS	SSI	IO	-	K	K	K	K
MODE11/DRAK3#/CE2A#	MODE11 (power-on reset)	RESET	I	I	-	-	-	-
	Port J4 (default)	GPIO	IO	-	K	K	-	K
	DRAK3#	DMAC	O	-	O	O	O	O
	CE2A#	LBSC	O	-	K	K	-	K
MODE12/SCIF5_TXD/CE2B#	MODE12 (power-on reset)	RESET	I	I	-	-	-	-
	Port J5 (default)	GPIO	IO	-	K	K	-	K
	SCIF5_TXD	SCIF	O	-	O	O	O	O
	CE2B#	LBSC	O	-	K	K	-	K
MODE13/SCIF5_RXD/IOIS16#	MODE13 (power-on reset)	RESET	I	I	-	-	-	-
	Port J6 (default)	GPIO	IO	-	K	K	-	K
	SCIF5_RXD	SCIF	I	-	I	I	I	I
	IOIS16#	LBSC	I	-	K	K	K	K
MODE14/SCIF5_SCK/FRB#	MODE14 (power-on reset)	RESET	I	I	-	-	-	-
	Port J7 (default)	GPIO	IO	-	K	K	-	K
	SCIF5_SCK	SCIF	IO	-	K	K	K	K
	FRB#	FLCTL	I	-	K	K	K	K
I2C_SCL0/SCIF2_RXD	I2C_SCL0 (default)	I2C	IO	PZ	K	K	K	K
	SCIF2_RXD	SCIF	I	-	I	I	I	I
I2C_SDA0/SCIF2_TXD	I2C_SDA0 (default)	I2C	IO	PZ	K	K	K	K
	SCIF2_TXD	SCIF	O	-	O	O	O	O
I2C_SCL1/SCIF2_SCK	I2C_SCL1 (default)	I2C	IO	PZ	K	K	K	K
	SCIF2_SCK	SCIF	IO	-	K	K	K	K
I2C_SDA1/IRQOUT#	I2C_SDA1 (default)	I2C	IO	PZ	K	K	K	K
	IRQOUT#	RESET	O	-	K	K	-	K
STATUS0/SSI2_CLK	STATUS0	RESET	O	H	H	L	L	L
	SSI2_CLK	SSI	I	-	I	I	I	I
STATUS1/SSI3_CLK	STATUS1	RESET	O	H	H	H	L	L
	SSI3_CLK	SSI	I	-	I	I	I	I
EXTAL	EXTAL	CPG	I	I	I	I	-	I
XTAL	XTAL	CPG	O	O	O	O	-	O
USB_EXTAL	USB_EXTAL	USB	I	I	I	I	I	I
USB_XTAL	USB_XTAL	USB	O	O	K	K	K	K
MPMD	MPMD	H-UDI	I	I	I	I	-	I
ASEBRK#/BRKACK	ASEBRK#/BRKACK	H-UDI	IO	PI	PI	PI	-	PI
TRST#	TRST#	H-UDI	I	PI	PI	PI	-	PI
TDO	TDO	H-UDI	O	O	O	O	-	O
TDI	TDI	H-UDI	I	PI	PI	PI	-	PI
TMS	TMS	H-UDI	I	PI	PI	PI	-	PI
TCK	TCK	H-UDI	I	PI	PI	PI	-	PI
AUDCK	AUDCK	H-UDI	O	L	L	L	-	L
AUDSYNC	AUDSYNC	H-UDI	O	H	H	H	-	H

Pin Name (LSI level)	Signal Name (Module level)	Module	I/O	Reset		Sleep/ Light Sleep	Module Standby	Bus Release
				Power-on	Manual			
AUDATA[3:0]	AUDATA[3:0]	H-UDI	O	L	L	L	-	L
MBA[2:0]	MBA[2:0]	DBSC3	O	L	K	K	-	K
MA[15:0]	MA[15:0]	DBSC3	O	L	K	K	-	K
MDQ[31:0]	MDQ[31:0]	DBSC3	IO	Z	K	K	-	K
MDM[3:0]	MDM[3:0]	DBSC3	O	H	K	K	-	K
MDQS[3:0]	MDQS[3:0]	DBSC3	IO	Z	K	K	-	K
MDQS[3:0]#	MDQS[3:0]#	DBSC3	IO	Z	K	K	-	K
MCS[1:0]#	MCS[1:0]#	DBSC3	O	L	K	K	-	K
MRAS#	MRAS#	DBSC3	O	L	K	K	-	K
MCAS#	MCAS#	DBSC3	O	L	K	K	-	K
MWE#	MWE#	DBSC3	O	L	K	K	-	K
MCKE[1:0]	MCKE[1:0]	DBSC3	O	O	O	O	-	O
MODT[1:0]	MODT[1:0]	DBSC3	O	L	K	K	-	K
MCK[1:0]	MCK[1:0]	DBSC3	O	L	K	K	-	K
MCK[1:0]#	MCK[1:0]#	DBSC3	O	L	K	K	-	K
MRESET#	MRESET#	DBSC3	O	O	O	O	-	O
SDBUP	SDBUP	DBSC3	I	I	I	I	-	I
MBKPRST#	MBKPRST#	DBSC3	I	I	I	I	-	I
MVREF[1:0]	MVREF[1:0]	DBSC3	-	-	-	-	-	-
MZQ	MZQ	DBSC3	-	-	-	-	-	-
USB_DP0	USB_DP0	USB	IO	L	K	K	K	K
USB_DM0	USB_DM0	USB	IO	L	K	K	K	K
USB_OVC0	USB_OVC0	USB	I	Z	K	K	K	K
USB_DP1	USB_DP1	USB	IO	L	K	K	K	K
USB_DM1	USB_DM1	USB	IO	L	K	K	K	K
USB_VBUS1_OVC1	USB_VBUS1_OVC1	USB	I	Z	K	K	K	K
USB_REXT	USB_REXT	USB	-	-	-	-	-	-
PCIE_RX1_0#	PCIE_RX1#	PCIEC	I	Z	I	I	I	I
PCIE_RX1_0	PCIE_RX1	PCIEC	I	Z	I	I	I	I
PCIE_TX1_0#	PCIE_TX1#	PCIEC	O	Z	K	K	K	K
PCIE_TX1_0	PCIE_TX1	PCIEC	O	Z	K	K	K	K
PCIE_RX0_[3:0]#	PCIE_RX0_[3:0]#	PCIEC	I	Z	K	K	K	K
PCIE_RX0_[3:0]	PCIE_RX0_[3:0]	PCIEC	I	Z	K	K	K	K
PCIE_TX0_[3:0]#	PCIE_TX0_[3:0]#	PCIEC	O	Z	K	K	K	K
PCIE_TX0_[3:0]	PCIE_TX0_[3:0]	PCIEC	O	Z	K	K	K	K
GCLK	GCLK	PCIEC	I	Z	K	K	K	K
GCLK#	GCLK#	PCIEC	I	Z	K	K	K	K
VTHREF	PA_VTHREF	Thermal sensor	O	O	O	O	O	O
VTHSENSE	PA_VTHSENSE	Thermal sensor	O	O	O	O	O	O

Legend:

-: Not selected or not supported
I: Input
O: Output
H: High level output
L: Low level output
Z: High impedance state
PI: Input and pulled up with a built-in pull-up resistance.
PZ: High impedance and pulled up with a built-in pull-up resistance.
K: Retain the previous pin state.

- End of Text -