Date: September. 12, 2012

RENESAS TECHNICAL UPDATE

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Product Category	MPU/MCU		Document No.	TN-SH7-A848A/E	Rev.	1.00
Title	SH7786 Exception Handling and Register States Manual Correction		Information Category	Technical Notification		
Applicable Product	SH7786 Group	Lot No. All lots	Reference Document	SH7786 Group User's Manual: Hardware Rev.1.00 Nov 30, 2010 (REJ09B0501-0100)		

There are some corrections about the SH7786 exception handling and register states in manual reset description in user's manual.

Cancelation line parts (~~abc~~) are deleted and gray parts (abc) are newly added.

[Correction]

1. Section 5, Exception Handling 5.3.2 Exception Handling Vector Addresses

Reference document page 97, Section 5.3.2: 1st line

The reset vector address is fixed at H'A0000000 for a power-on reset or H-UDI reset. For a manual reset, instruction TLB multiple hit exception and data TLB multiple hit exception, the reset vector address are the address set in the CnRESETVEC register. Exception and interrupt vector addresses are determined by adding the offset for the specific ...

2. Section 5, Exception Handling 5.4 Exception Types and Priorities Table 5.3 Exceptions

1) Reference document page 98, Table 5.3: Exception Transition Direction, Vector Address; Manual reset, Instruction TLB multiple-hit exception, Data TLB multiple-hit exception Register name: ~~CPUn~~ CnRESETVEC

2) Reference document page 99, Table 5.3: Notes 3

Control passes to H'A000 0000 in a ~~reset~~ power-on reset and H-UDI reset, to address set in the CnRESETVEC register in manual reset, instruction TLB multiple hit exception and data TLB multiple hit exception and to [VBR + offset] in other cases.

3. Section 5, Exception Handling 5.6.1 Resets (2) Manual Reset

Reference document page 104, Operations: 1st line; 4th line and following note are newly added

• Operations:

Exception code H'020 is set in EXPEVT, initialization of the CPUn (n=0, 1) ~~and on-chip peripheral modules~~ is carried out, and then a branch is made to the reset vector (the address set in the ~~CPUn~~ CnRESETVEC register). The registers initialized by a power-on reset and manual reset are different. Note that, initialization by the Manual Reset of the SH7786 is carried out only for the CPUn registers* and on-chip peripheral module registers are retained. For details, see the register descriptions in the relevant sections.

Note. *: The CPUn registers are registers described in table 2.1 in reference document page 26, and the CPU0 and CPU1 has these registers respectively. For details of these registers, see sections 2 and 6. For the remaining CPUn

registers, see the register description in sections 5, 7, 8, 9 and appendix A.

4. Section 5, Exception Handling 5.6.1 Resets (4) Instruction TLB Multiple Hit Exception

Reference document page 105, Transition address and transition operations

- Transition address: ~~H'A0000000~~ Address set in the CnRESETVEC register
- Transition operations:

The virtual address (32 bits) at which this exception occurred is set in TEA, and the corresponding virtual page number (22 bits) is set in PTEH [31:10]. ASID in PTEH indicates the ASID when this exception occurred.

Exception code H'140 is set in EXPEVT. After VBR and SR are initialized, a branch is made to the reset vector (the address set in the ~~CPUn~~ CnRESETVEC register).

CPUn (n=0, 1) ~~and on-chip peripheral module~~ initialization is performed in the same way as in a manual reset. For details, see the register descriptions in the relevant sections.

5. Section 5, Exception Handling 5.6.1 Resets (5) Data TLB Multiple Hit Exception

Reference document page 105, Transition address and transition operations

- Transition address: ~~H'A0000000~~ Address set in the CnRESETVEC register
- Transition operations:

The virtual address (32 bits) at which this exception occurred is set in TEA, and the corresponding virtual page number (22 bits) is set in PTEH [31:10]. ASID in PTEH indicates the ASID when this exception occurred.

Exception code H'140 is set in EXPEVT. After VBR and SR are initialized, a branch is made to the reset vector (the address set in the ~~CPUn~~ CnRESETVEC register).

CPUn (n=0, 1) ~~and on-chip peripheral module~~ initialization is performed in the same way as in a manual reset. For details, see the register descriptions in the relevant sections.

6. Section 5, Exception Handling 5.6.3 Interrupts (1) NMI (Nonmaskable Interrupt)

Reference document page 122, following note is newly added

- Source: NMI pin edge detection*

Note. *: Detected NMI input is only provided to the CPU0. To input NMI to the CPU1, set the NMI interrupt to the CPU1 by using NMI set register. For details, refer to section 10, Interrupt Controller: 10.3.1 (12) NMI Set control Register (NMISET).

7. Section 10, Interrupt Controller (INTC) 10.3 Register Descriptions Table 10.4 Register States in Each Operating Mode

Reference document pages 276 to 281, Table 10.4 header: Manual Reset condition, registers state: Manual Reset

(#: Low active, the followings are the same)

Name	Abbreviation	Power-on Reset by PRESET# Pin//WDT/H-UDI	Manual Reset by ~~WDT~~ CnWDTCNT(n=0, 1) Overflow/Multiple Exception	Sleep/Light Sleep by SLEEP Instruction
Interrupt control register 0	ICR0	H'x000 0000	~~H'x000 0000 etc.~~ ~~(Initialized)~~ Retained (all registers)	Retained
:	:	:		:
Thermal Sensor Interrupt register	INT2THSC	H'0000 0000		Retained

8. Section 11, Local Bus State Controller (LBSC) 11.4 Register Descriptions Table 11.6 Register Configuration (2)

Reference document page 390, Table 11.6 header: Manual Reset condition, MMSELR register state: manual Reset

Register Name	Abbrev.	Power-on Reset by PRESET# Pin/ WDT/H-UDI	Manual Reset by ~~WDT~~ CnWDTCNT (n=0, 1) Overflow/Multiple Exception	Sleep/Light Sleep by SLEEP Instruction
Memory Address Map Select Register	MMSELR	H'0000 0000	~~H'00000000~~ Retained	Retained
:	:	:	:	:

9. Section 12, DDR3-SDRAM Interface (DBSC3) 12.4 Register Descriptions Table 12.7 Register Status in each Processing Mode

Reference document pages 487 to 489, Table 12.7 header: Manual Reset condition

		Power-On Reset	Manual Reset	Sleep/Light Sleep
Register Name	Abbreviation	By PRESET# pin/ WDT/H-UDI	By ~~WDT~~ CnWDTCNT (n=0, 1) Overflow/Multiple Exception	By SLEEP Instruction

10. Section 14.1, USB 14.1.4 Register Descriptions Table 14.2 List of Registers

Reference document page 853, after Table 14.2: following List of Registers (2) is newly added

Register Name	Abbreviation	Power-on Reset By PRESET# Pin/WDT/ H-UDI	Manual Reset By CnWDTCNT (n=0, 1) Overflow/ Multiple Exception	Sleep/ Light Sleep By SLEEP Instruction	Module Standby
Port Control 0	USBPCTRL0	Initialized*	Retained	Retained	Retained
Port Control 1	USBPCTRL1	Initialized*	Retained	Retained	Retained
Port Status	USBST	Initialized*	Retained	Retained	Retained
EHCI Control 0	USBEH0	Initialized*	Retained	Retained	Retained
OHCI Control 0	USBOH0	Initialized*	Retained	Retained	Retained
USB Control 0	USBCTL0	Initialized*	Retained	Retained	Retained

Note. *: For details on the initial value, see the descriptions of the individual registers. Note that, for the initialization of the USB module, follow the description of the register and execute after a power-on reset.

11. Section 14.2 USB2.0-HOST Controller 14.2.2 Register Descriptions Table 14.4 Host Controller Operational Registers

Reference document page 864, after Table 14.4: following List of Registers is newly added

Register Name	Power-on Reset By PRESET# Pin/WDT/ H-UDI	Manual Reset By CnWDTCNT (n=0, 1) Overflow/ Multiple Exception	Sleep/ Light Sleep By SLEEP Instruction	Module Standby
HCIVERSION/CAPLENGTH	Initialized*	Retained	Retained	Retained
HCSPARAMS	Initialized*	Retained	Retained	Retained
HCCPARAMS	Initialized*	Retained	Retained	Retained
HCSP-PORTROUTE	Initialized*	Retained	Retained	Retained

Register Name	Power-on Reset By PRESET# Pin/WDT/ H-UDI	Manual Reset By CnWDTCNT (n=0, 1) Overflow/ Multiple Exception	Sleep/ Light Sleep By SLEEP Instruction	Module Standby
USBCMD	Initialized*	Retained	Retained	Retained
USBSTS	Initialized*	Retained	Retained	Retained
USBINTR	Initialized*	Retained	Retained	Retained
FRINDEX	Initialized*	Retained	Retained	Retained
CTRLDSSEGMENT	Initialized*	Retained	Retained	Retained
PERIODICLISTBASE	Initialized*	Retained	Retained	Retained
ASYNCLISTADDR	Initialized*	Retained	Retained	Retained
CONFIGFLAG	Initialized*	Retained	Retained	Retained
PORTSC (1 – N_PORT)	Initialized*	Retained	Retained	Retained

Note. *: For details on the initial value, see the descriptions of the individual registers. Note that, for the initialization of the USB module, follow the description of the register and execute after a power-on reset.

12. Section 14.3 USB1.1-HOST Controller 14.3.2 Register Descriptions table 14.5 List of Open HCI Registers

Reference document pages 896 and 897, after Table 14.5: following List of Open HCI Registers (2) is newly added

Register Name	Power-on Reset By PRESET# Pin/WDT/ H-UDI	Manual Reset By CnWDTCNT (n=0, 1) Overflow/ Multiple Exception	Sleep/ Light Sleep By SLEEP Instruction	Module Standby
HcRevision register	Initialized*	Retained	Retained	Retained
HcControl register	Initialized*	Retained	Retained	Retained
HcCommandStatus register	Initialized*	Retained	Retained	Retained
HcInterruptStatus register	Initialized*	Retained	Retained	Retained
HcInterruptEnable register	Initialized*	Retained	Retained	Retained
HcInterruptDisable register	Initialized*	Retained	Retained	Retained
HcHCCA register	Initialized*	Retained	Retained	Retained
HcPeriodCurrentED register	Initialized*	Retained	Retained	Retained
HcControlHeadED register	Initialized*	Retained	Retained	Retained
HcControlCurrentED register	Initialized*	Retained	Retained	Retained
HcBulkHeadED register	Initialized*	Retained	Retained	Retained
HcBulkCurrentED register	Initialized*	Retained	Retained	Retained
HcDoneHead register	Initialized*	Retained	Retained	Retained
HcFmInterval register	Initialized*	Retained	Retained	Retained
HcFmRemaining register	Initialized*	Retained	Retained	Retained
HcFmNumber register	Initialized*	Retained	Retained	Retained
HcPeriodicStart register	Initialized*	Retained	Retained	Retained

Register Name	Power-on Reset By PRESET# Pin/WDT/ H-UDI	Manual Reset By CnWDTCNT (n=0, 1) Overflow/ Multiple Exception	Sleep/ Light Sleep By SLEEP Instruction	Module Standby
HcLSThreshold register	Initialized*	Retained	Retained	Retained
HcRhDescriptorA register	Initialized*	Retained	Retained	Retained
HcRhDescriptorB register	Initialized*	Retained	Retained	Retained
HcRhStatus register	Initialized*	Retained	Retained	Retained
HcRhPortStatus1 register	Initialized*	Retained	Retained	Retained
HcRhPortStatus2 register	Initialized*	Retained	Retained	Retained

Note. *: For details on the initial value, see the descriptions of the individual registers. Note that, for the initialization of the USB module, follow the description of the register and execute after a power-on reset.

13. Section 14.4 USB2.0-Function Controller 14.4.4 Register Specifications Table 14.6 List of Registers

Reference document pages 924 to 926, after Table 14.6: following List of Registers (2) is newly added

Symbol	Name	Power-on Reset By PRESET# Pin/WDT/ H-UDI	Manual Reset By CnWDTCNT (n=0, 1) Overflow/ Multiple Exception	Sleep/ Light Sleep By SLEEP Instruction	Module Standby
SYSCFG0	System configuration control register	Initialized*	Retained	Retained	Retained
BUSWAIT	CPU bus wait register	Initialized*	Retained	Retained	Retained
SYSSTS0	System configuration status register	Initialized*	Retained	Retained	Retained
DVSTCTR0	Device state control register	Initialized*	Retained	Retained	Retained
TESTMODE	Test mode register	Initialized*	Retained	Retained	Retained
D0FBCFG	DMA0-FIFO bus configuration register	Initialized*	Retained	Retained	Retained
D1FBCFG	DMA1-FIFO bus configuration register	Initialized*	Retained	Retained	Retained
CFIFO	CFIFO port register	Initialized*	Retained	Retained	Retained
D0FIFO	D0FIFO port register	Initialized*	Retained	Retained	Retained
D1FIFO	D1FIFO port register	Initialized*	Retained	Retained	Retained
CFIFOSEL	CFIFO port select register	Initialized*	Retained	Retained	Retained
CFIFOCTR	CFIFO port control register	Initialized*	Retained	Retained	Retained
D0FIFOSEL	D0FIFO port select register	Initialized*	Retained	Retained	Retained
D0FIFOCTR	D0FIFO port control register	Initialized*	Retained	Retained	Retained
D1FIFOSEL	D1FIFO port select register	Initialized*	Retained	Retained	Retained
D1FIFOCTR	D1FIFO port control register	Initialized*	Retained	Retained	Retained

Symbol	Name	Power-on Reset By PRESET# Pin/WDT/ H-UDI	Manual Reset By CnWDTCNT (n=0, 1) Overflow/ Multiple Exception	Sleep/ Light Sleep By SLEEP Instruction	Module Standby
INTENB0	Interrupt enable register 0	Initialized*	Retained	Retained	Retained
INTENB1	Interrupt enable register 1	Initialized*	Retained	Retained	Retained
BRDYENB	BRDY Interrupt enable register	Initialized*	Retained	Retained	Retained
NRDYENB	NRDY Interrupt enable register	Initialized*	Retained	Retained	Retained
BEMPENB	BEMP Interrupt enable register	Initialized*	Retained	Retained	Retained
SOFCFG	SOF output configuration register	Initialized*	Retained	Retained	Retained
INTSTS0	Interrupt status register 0	Initialized*	Retained	Retained	Retained
INTSTS1	Interrupt status register 1	Initialized*	Retained	Retained	Retained
BRDYSTS	BRDY Interrupt status register	Initialized*	Retained	Retained	Retained
NRDYSTS	NRDY Interrupt status register	Initialized*	Retained	Retained	Retained
BEMPSTS	BEMP Interrupt status register	Initialized*	Retained	Retained	Retained
FRMNUM	Frame number register	Initialized*	Retained	Retained	Retained
UFRMNUM	µFrame number register	Initialized*	Retained	Retained	Retained
USBADDR	USB address register	Initialized*	Retained	Retained	Retained
USBREQ	USB request type register	Initialized*	Retained	Retained	Retained
USBVAL	USB request value register	Initialized*	Retained	Retained	Retained
USBINDX	USB request index register	Initialized*	Retained	Retained	Retained
USBLENG	USB request length register	Initialized*	Retained	Retained	Retained
DCPCFG	DCP configuration register	Initialized*	Retained	Retained	Retained
DCPMAXP	DCP maximum packet size register	Initialized*	Retained	Retained	Retained
DCPCTR	DCP control register	Initialized*	Retained	Retained	Retained
PIPESEL	Pipe window select register	Initialized*	Retained	Retained	Retained
PIPECFG	Pipe configuration register	Initialized*	Retained	Retained	Retained
PIPEBUF	Pipe buffer setting register	Initialized*	Retained	Retained	Retained
PIPEMAXP	Pipe maximum packet size register	Initialized*	Retained	Retained	Retained
PIPEPERI	Pipe cycle control register	Initialized*	Retained	Retained	Retained
PIPE1 to PIPE9 CTR	PIPE1 to PIPE9 control register	Initialized*	Retained	Retained	Retained

Symbol	Name	Power-on Reset By PRESET# Pin/WDT/ H-UDI	Manual Reset By CnWDTCNT (n=0, 1) Overflow/ Multiple Exception	Sleep/ Light Sleep By SLEEP Instruction	Module Standby
PIPE1 to PIPE5 TRE	PIPE1 to PIPE5 transaction counter enable register	Initialized*	Retained	Retained	Retained
PIPE1 to PIPE5 TRN	PIPE1 to PIPE5 transaction counter register	Initialized*	Retained	Retained	Retained
DEVADD0 to DEVADDA	Device address 0 to Device address A configuration register	Initialized*	Retained	Retained	Retained
SUSPMODE	UTMI suspend mode register	Initialized*	Retained	Retained	Retained

Note. *: For details on the initial value, see the descriptions of the individual registers. Note that, in register description, a power-on reset is called as hardware (H/W) reset. For details of the initialization of the USB module, refer to the description of registers after a power-on reset.

14. Section 15, Direct Memory Access Controller 0 (DMAC0) 15.3 Register Configuration Table 15.2 Register Configuration of DMAC0 (2)

Reference document pages 1053 and 1054, Table 15.2 header: Manual Reset condition

Channel	Name	Abbreviation	Power-on Reset by PRESET# Pin/WDT/ H-UDI	Manual Reset by ~~WDT~~ CnWDTCNT (n=0, 1) Overflow/ Multiple Exception	Sleep/ Light Sleep by SLEEP Instruction	Module Standby

15. Section 17, HPB-DMAC 17.4 Register Configuration Table 17.2 List of HPB-DMAC Registers (2)

Reference document pages 1147 and 1148, Table 17.2 header: Power-On/Manual Reset conditions, registers state: Manual Reset

Address(Bytes)	Name	Abbreviation	Power-On Reset by ~~RESET#~~ PRESET# pin, WDT, or H-UDI	Manual Reset by ~~RESET# pin or~~ ~~WDT~~ CnWDTCNT (n=0, 1) Overflow/ or multiple exception
H'FFC00300	SD mode select register	SDMDR	H'0000_0000	~~H'0000_0000 etc. (Initialized)~~ Retained (all registers)
:	:	:	:	
H'FFC08894	[Common to HPB-DMAC] HPB-DMA SuperHyway priority control register 1	HPB-DMASPR1	H'0088_8888	

16. Section 18, Clock Pulse Generator (CPG) 18.4 Register Descriptions Table 18.5 Register State in Each Processing Mode

Reference document page 1196, Table 18.5 header: Manual Reset condition

Register Name	Abbreviation	Power-on Reset by the PRESET# Pin, WDT, or H-UDI	Manual Reset by ~~WDT~~ CnWDTCNT (n=0, 1) Overflow or Multiple Exception	Sleep or Light Sleep by SLEEP Instruction

17. Section 19, Watchdog Timer and Reset (WDT) 19.3 Register Descriptions Table 19.3 Register States in Each Operating Mode

Reference document page 1213, Table 19.3 header: Manual Reset condition

Register Name	Abbreviation	Power-on Reset by PRESET# Pin	Power-on Reset by WDT/H-UDI	Manual Reset by ~~WDT~~ CnWDTCNT (n=0, 1) Overflow/ Multiple Exception	Sleep/Light Sleep Mode by SLEEP Instruction

18. Section 20, Power-Down Mode 20.3 Register Descriptions Table 20.4 Register States in Each Processing Mode

Reference document page 1242, Table 20.4 header: Manual Reset condition

		Power-On Reset	Manual Reset	Sleep/ Light Sleep
Register Name	Abbreviation	By PRESET# pin/WDT/H-UDI	By ~~WDT~~ CnWDTCNT (n=0, 1) Overflow/Multiple Exceptions	By SLEEP Instruction

19. Section 21, Timer Unit (TMU) 21.3 Register Descriptions Table 21.3 Register Configuration (2)

Reference document pages 1263 and 1264, Table 21.3 header: Manual Reset condition

Channel	Register Name	Abbreviation	Power-on Reset by PRESET# Pin/ WDT/H-UDI	Manual Reset by ~~WDT~~ CnWDTCNT (n=0, 1) Overflow/ Multiple Exceptions	Sleep/ Light Sleep by SLEEP Instruction	Module Standby

20. Section 22, Ethernet (Ether) 22.4.2 Register Configuration Table 22.5 HDMAC Register States in Each Operating Mode

Reference document pages 1288 and 1289, Table 22.5 header: Power-On/Manual Reset/Light Sleep conditions, registers state: Manual Reset.

Register Name	Abbreviation	Power-On Reset by ~~RESET#~~ PRESET# Pin/WDT/ H-UDI	Manual Reset by ~~WDT~~ CnWDTCNT (n=0, 1) Overflow/ ~~Multiplex~~ Multiple Exception	Sleep by Sleep Instruction	Module Standby	Light Sleep by SLEEP Instruction
HDMAC operating mode setting register	CXR0	H'0000 0000	~~H'0000 0000 etc. (Initialized)~~ Retained (all registers other than reserved)	Retained	Retained	Retained
:	:	:		:	:	:
Transmit interrupt mode setting register	CXR18	H'0000 0000		Retained	Retained	Retained

21. Section 22, Ethernet (Ether) 22.4.2 Register Configuration Table 22.6 feLic Register States in Each Operating Mode

Reference document pages 1289 and 1290, Table 22.6 header: Power-On/Manual Reset/Light Sleep conditions, registers state: Manual Reset

Register Name	Abbreviation	Power-On Reset by ~~RESET#~~ PRESET# Pin/WDT/ H-UDI	Manual Reset by ~~WDT~~ CnWDTCNT (n=0, 1) Overflow/ ~~Multiplex~~ Multiple Exception	Sleep by Sleep Instruction	Module Standby	Light Sleep by SLEEP Instruction
feLic operating mode setting register	CXR20	H'0000 0000	~~H'0000 0000 etc. (Initialized)~~	Retained	Retained	Retained
:	:	:	Retained (all registers	:	:	:
RINT8 counter register	CXR55	H'0000 0000	other than reserved)	Retained	Retained	Retained

22. Section 24, Serial Communication Interface with FIFO (SCIF) 24.3 Register Descriptions Table 24.2 Register Configuration (2)

Reference document pages 1507 to 1509, Table 24.2 header: Manual Reset condition, registers state: Manual Reset

Ch.	Register Name	Abbreviation	Power-on Reset by PRESET# Pin/ WDT/H-UDI	Manual Reset by ~~WDT~~ CnWDTCNT (n=0, 1) Overflow/ Multiple Exception	Sleep/Light Sleep by SLEEP Instruction	Module Standby
0 to 5	Transmit FIFO data register 0 to 5	SCFTDR0 to SCFTDR5	Undefined	~~Undefined~~ Retained	Retained	Retained
0 to 5	Receive FIFO data register 0 to 5	SCFRDR0 to SCFRDR5	Undefined	~~Undefined~~ Retained	Retained	Retained

23. Section 25, Serial Peripheral Interface (HSPI) 25.3 Register Descriptions Table 25.3 Register Configuration (2)

Reference document page 1568, Table 25.3 header: Manual Reset condition

Register Name	Abbrev.	Power-on Reset by PRESET# Pin/WDT/ H-UDI	Manual Reset by ~~WDT~~ CnWDTCNT (n=0, 1) Overflow/ Multiple Exception	Sleep/Light Sleep by SLEEP Instruction	Module Standby	Software Reset

24. Section 26, NAND Flash Memory Controller (FLCTL) 26.3 Register Descriptions Table 26.3 Register States in Each Processing Mode

Reference document page 1593, Table 26.3 header: Reset/Sleep conditions, registers state: Manual Reset

Register Abbreviation	Power-On Reset by PRESET# Pin/ WDT/H-UDI	Manual Reset by CnWDTCNT (n=0, 1) Overflow/Multiple Exception	Sleep/Light Sleep by SLEEP Instruction	Module Standby
FLCMNCR	H'0000 0000		Retained	Retained
:	:	~~Initialized/Undefined~~ Retained (All registers)	:	:
FLCSLR	H'0000 0000		Retained	Retained

25. Section 27, Audio Codec Interface (HAC) 27.3 Register Descriptions Table 27.3 Register Configuration (2)

Reference document page 1635, Table 27.3 header: Manual Reset/Light Sleep conditions

Channel	Register Name	Abbrev.	Power-on Reset by PRESET# Pin/WDT/ H-UDI	Manual Reset by ~~WDT~~ CnWDTCNT (n=0, 1) Overflow/ Multiple Exceptions	Sleep by SLEEP Instruction	Module Standby	Light Sleep by SLEEP Instruction

26. Section 28, Serial Sound Interface (SSI) Module 28.3 Register Descriptions Table 28.3 Register Configuration (2)

Reference document page 1667, Table 28.3 header: Manual Reset/Light Sleep conditions

Channel	Register Name	Abbr.	Power-on Reset by PRESET# Pin/ WDT/H-UDI	Manual Reset by ~~WDT~~ CnWDTCNT (n=0, 1) Overflow/ Multiple Exceptions	Sleep by SLEEP Instruction	Module Standby	Light Sleep by SLEEP Instruction

27. Section 29, I2C Bus Interface 29.3 Register Descriptions Table 29.2 Register Configuration (2)

Reference document page 1708, Table 29.2 header: Manual Reset condition

Register Name	Abbreviation	Power-on Reset by PRESET# Pin/ WDT/H-UDI	Manual Reset by ~~WDT~~ CnWDTCNT (n=0, 1) Overflow/ Multiple Exception	Sleep/Light Sleep by SLEEP Instruction	Module Standby

28. Section 30, General Purpose I/O Ports (GPIO) 30.2 Register Descriptions Table 30.2 Register Configuration (2)

Reference document page 1744, Table 30.2 header: Power-on/Manual Reset conditions

Register Name	Abbr.	Power-on Reset by ~~RESET#~~ PRESET# Pin/ WDT/H-UDI	Manual Reset by ~~WDT~~ CnWDTCNT (n=0, 1) Overflow/ Multiple Exception	Sleep/Light Sleep by SLEEP Instruction	Module Standby

29. Appendix A.9 Barrier Synchronization Register

Reference document page 1992, after Table: following List of registers is newly added

Register Name	Abbr.	Power-on Reset By PRESET# Pin/WDT/ H-UDI	Manual Reset By CnWDTCNT (n=0, 1) Overflow/ Multiple Exception	Sleep/ Light Sleep By SLEEP Instruction
Barrier write register 0 to 2	BARW0 to BARW2	H'0000 0000	H'0000 0000	Undefined
Barrier read register 0 to 2	BARR0 to BARR2	H'0000 0000	H'0000 0000	Undefined

[Notice]

In manual reset, sleep or light sleep mode, on-chip peripheral modules continue their preceding operations. Therefore, their registers state may be updated by the operation even if described as "Retained" in above tables.

- End of Correction -