To our customers,

Old Company Name in Catalogs and Other Documents

On April 1st, 2010, NEC Electronics Corporation merged with Renesas Technology Corporation, and Renesas Electronics Corporation took over all the business of both companies. Therefore, although the old company name remains in this document, it is a valid Renesas Electronics document. We appreciate your understanding.

Renesas Electronics website: http://www.renesas.com

April 1st, 2010
Renesas Electronics Corporation

Issued by: Renesas Electronics Corporation (http://www.renesas.com)

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RENESAS TECHNICAL UPDATE

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Product Category	MPU&MCU		Document No.	TN-SH7-A650A/E	Rev.	1.00
Title	SH7764 Group Hardware manual Rev.1.00 corrections – 2nd –		Information Category	Technical Notification		
Applicable Product	R5S77640P300BG R5S77640D300BG R5S77640N300BG R5S77641P300BG R5S77641D300BG R5S77641N300BG	Lot No.				
		All lots	Reference Document	SH7764 Group Hardware Manual (REJ09B0360-0100)		

We would like to inform valued customers on hardware manual corrections as described bellow.
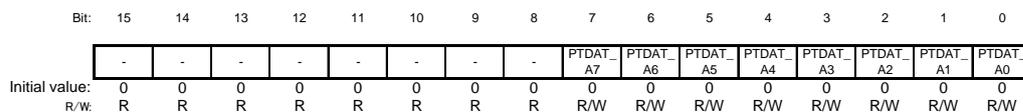
- Note -

1. Additional descriptions to GPIO port A data register
2. Bus timing change

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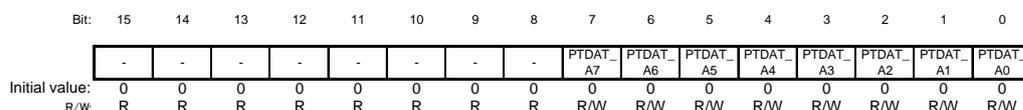1.   Additional descriptions to GPIO port A data register

Original descriptions

> PTDAT_A is a 16-bit readable/writable register that stores port A data.

Bit:	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
	-	-	-	-	-	-	-	-	PTDAT_A7	PTDAT_A6	PTDAT_A5	PTDAT_A4	PTDAT_A3	PTDAT_A2	PTDAT_A1	PTDAT_A0
Initial value:	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
R/W:	R	R	R	R	R	R	R	R	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W

Bit	Bit Name	Initial value	R/W	Description
15 to 8	—	0	R	Reserved The lower 8-bit value is always read from these bits. The write value should always be 0.
7	PTDAT_A7	0	R/W	Each bit stores output data of a pin used as a general output port.
6	PTDAT_A6	0	R/W	
5	PTDAT_A5	0	R/W	When the pin is used as general output port, if the port is read, the value of the corresponding bit in this register will be read.
4	PTDAT_A4	0	R/W	
3	PTDAT_A3	0	R/W	When the pin is used as a general input port, if this register is read, the status of the corresponding pin will be read.
2	PTDAT_A2	0	R/W	
1	PTDAT_A1	0	R/W	
0	PTDAT_A0	0	R/W	

Corrected descriptions

> PTDAT_A is a 16-bit readable/writable register that stores port A data.

Bit:	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
	-	-	-	-	-	-	-	-	PTDAT_A7	PTDAT_A6	PTDAT_A5	PTDAT_A4	PTDAT_A3	PTDAT_A2	PTDAT_A1	PTDAT_A0
Initial value:	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
R/W:	R	R	R	R	R	R	R	R	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W

Bit	Bit Name	Initial value	R/W	Description
15 to 8	—	0	R	Reserved The lower 8-bit value is always read from these bits. The write value should always be 0.
7	PTDAT_A7	0	R/W	Each bit stores output data of a pin used as a general output port.
6	PTDAT_A6	0	R/W	
5	PTDAT_A5	0	R/W	When the pin is used as general output port, if the port is read, the value of the corresponding bit in this register will be read.
4	PTDAT_A4	0	R/W	
3	PTDAT_A3	0	R/W	When the pin is used as a general input port, if this register is read, the status of the corresponding pin will be read.
2	PTDAT_A2	0	R/W	<u>When the pin is set to a function other than the general port, if it is used as an input pin, the pin status will be read from the corresponding bit in this register and writing to the bit is ignored; for an output pin, an undefined value will be read from the bit and writing to the bit is ignored.</u>
1	PTDAT_A1	0	R/W	
0	PTDAT_A0	0	R/W	

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2.   Bus timing change

33.4.3 Bus Timing

Table 33.14 Bus Timing

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Original bus timing table

Item	Symbol	Min.	Max.	Unit	figure
DQM delay time	t_{DQMD}	1.0	7.0	ns	33.12 to 33.23

Corrected bus timing table

Item	Symbol	Min.	Max.	Unit	figure
DQM delay time	t_{DQMD}	1.0	<u>7.4</u>	ns	33.12 to 33.23

- End of report -