To our customers,

Old Company Name in Catalogs and Other Documents

On April 1st, 2010, NEC Electronics Corporation merged with Renesas Technology Corporation, and Renesas Electronics Corporation took over all the business of both companies. Therefore, although the old company name remains in this document, it is a valid Renesas Electronics document. We appreciate your understanding.

Renesas Electronics website: http://www.renesas.com

April 1st, 2010
Renesas Electronics Corporation

Issued by: Renesas Electronics Corporation (http://www.renesas.com)

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RENESAS

Date: Jun.19.2009

RENESAS TECHNICAL UPDATE

Nippon Bldg., 2-6-2, Ohte-machi, Chiyoda-ku, Tokyo 100-0004, Japan
Renesas Technology Corp.

Product Category	MPU&MCU		Document No.	TN-SH7-A726A/E	Rev.	1.00
Title	SH7763 Hardware manual Rev.2.00 corrections		Information Category	Technical Notification		
Applicable Product	SH7763 Group	Lot No. All Lots	Reference Document	SH7763 Hardware Manual Rev.2.00 (REJ09B0256-0200)		

We would like to inform valued customers on hardware manual corrections as described bellow.

- Note -

1. Description correction of Compare Match Timer Control/Status Register (CMCSR) (Page 754)

- Original description

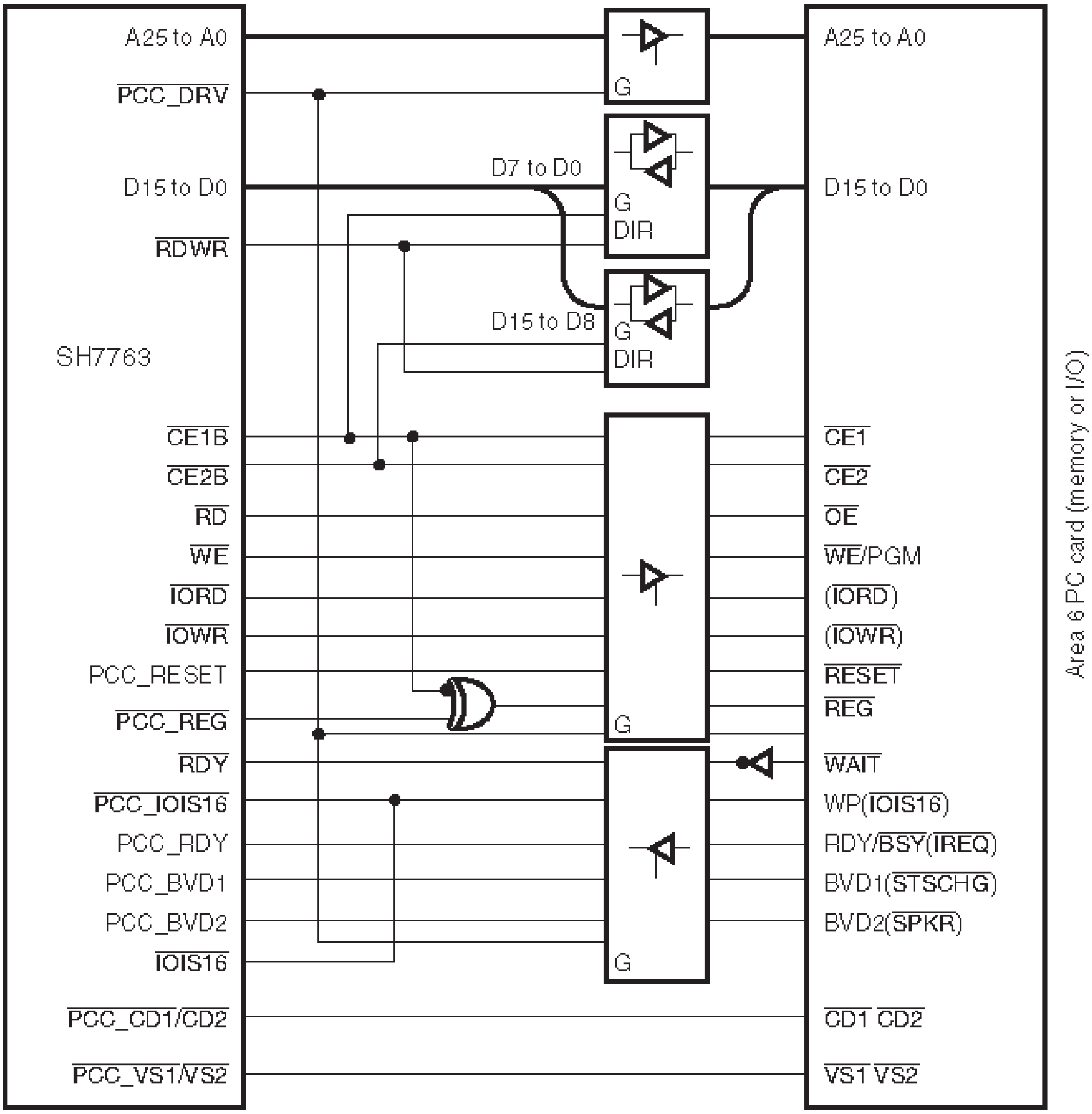
Bit	Bit Name	Initial Value	R/W	Description
15	CMF	0	R/(W)*1	Compare Match Flag This flag indicates whether or not values of the compare match timer counter (CMCNT) and compare match timer constant register (CMCOR) have matched. Software cannot write 1 to the bit. When one-shot is selected for the counter operation, counting resumes by clearing this bit. 0: CMCNT and CMCOR values have not matched [Clearing condition] · Write 0 to CMF after reading CMF=1 1: CMCNT and CMCOR values have matched
14	OVF	0	R/(W)*1	Overflow Flag This flag indicates whether or not the compare match timer counter (CMCNT) has overflowed and been cleared to 0. Software cannot write 1 to this bit. 0: CMCNT has not overflowed [Clearing condition] · Write 0 to OVF after reading OVF=1 1: CMCNT has overflowed

- Corrected description

Bit	Bit Name	Initial Value	R/W	Description
15	CMF	0	R/(W)*1	Compare Match Flag This flag indicates whether or not values of the compare match timer counter (CMCNT) and compare match timer constant register (CMCOR) have matched. Software cannot write 1 to the bit. When one-shot is selected for the counter operation, counting resumes by clearing this bit. 0: CMCNT and CMCOR values have not matched [Clearing condition] · Write 0 to CMF 1: CMCNT and CMCOR values have matched
14	OVF	0	R/(W)*1	Overflow Flag This flag indicates whether or not the compare match timer counter (CMCNT) has overflowed and been cleared to 0. Software cannot write 1 to this bit. 0: CMCNT has not overflowed [Clearing condition] · Write 0 to OVF 1: CMCNT has overflowed

2. PC card Connection Specification (Interface Diagram, Pin Correspondence) (Page 1382)

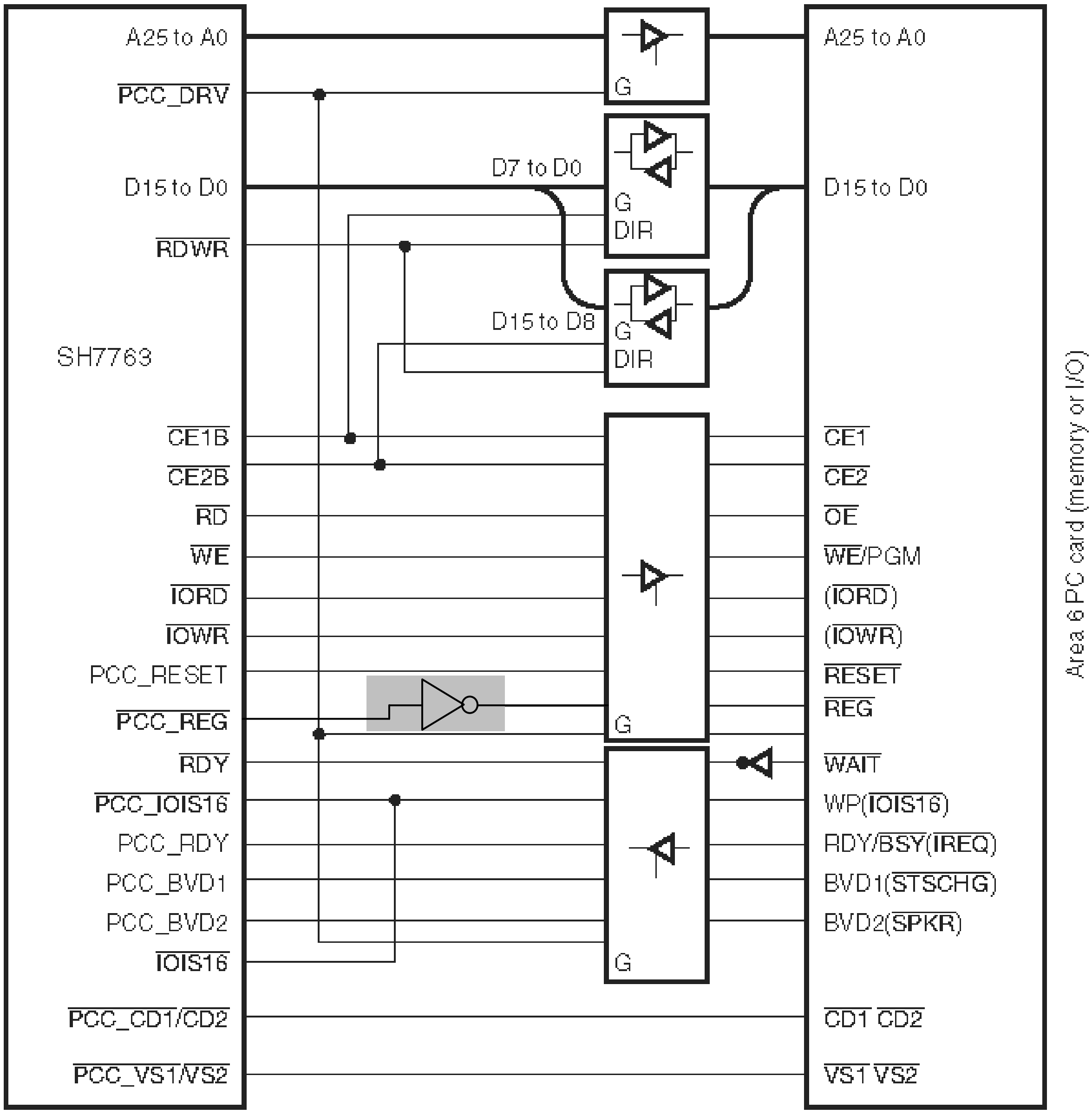
- Original figure



Note: Refer to section 11, Local Bus State Controller (LBSC), for $\overline{IOIS16}$.

Figure 32.4 SH7763 Interface

- Corrected figure



Note: Refer to section 11, Local Bus State Controller (LBSC), for IOIS16.

Figure 32.4 SH7763 Interface (When PCC0GCR.P0USE=1)

3. GETHER Module Signal Timing (Page 1874)

- Original table

Table 43.20 Ethernet Controller Signal Timing (GMII)

Conditions: V_{CCQ} = VDD_RTC = AV_{CC} = 3.0 to 3.6 V, $V_{CCQ\text{-}DDR}$ = 2.3 to 2.7 V, VDD = 1.15 to 1.35 V, Ta = –20 to 75°C

Item	Symbol	Min.	Typ.	Max.	Unit	Figure
GETn_GTX-CLK cycle time	t_{Gtcyc}	8	—	—	ns	43.45
Etn_TX-EN output delay time	t_{GTEND}	0.5	—	5.5	ns	43.45
GETn_ETXD[7:4], ETn_ETXD[3:0] output delay time	t_{GETDD}	0.5	—	5.5	ns	43.45
ETn_RX-CLK cycle time	t_{GRcyc}	8	—	—	ns	43.46
ETn_RX-DV setup time	t_{GRDVS}	2.5	—	—	ns	43.46
ETn_RX-DV hold time	t_{GRDVH}	0.5	—	—	ns	43.46
GETn_ERXD[7:4], ETn_ERXD[3:0] setup time	t_{GERDS}	2.5	—	—	ns	43.46
GETn_ERXD[7:4], ETn_ERXD[3:0] hold time	t_{GERDH}	0.5	—	—	ns	43.46
ETn_RX-ER setup time	t_{GRERS}	2.5	—	—	ns	43.47
ETn_RX-ER hold time	t_{GRERH}	0.5	—	—	ns	43.47
ETn_WOL output delay time	t_{GWOLD}	0	—	18	ns	43.48

- Corrected table

Table 43.20 Ethernet Controller Signal Timing (GMII)

Conditions: V_{CCQ} = VDD_RTC = AV_{CC} = 3.0 to 3.6 V, $V_{CCQ\text{-}DDR}$ = 2.3 to 2.7 V, VDD = 1.15 to 1.35 V, Ta = –20 to 75°C

Item	Symbol	Min.	Typ.	Max.	Unit	Figure
REF125CK clock input frequency	$f_{REF125CK}$	125 – 100ppm	—	125 + 100ppm	MHz	
GETn_GTX-CLK cycle time	t_{Gtcyc}	8	—	—	ns	43.45
Etn_TX-EN output delay time	t_{GTEND}	0.5	—	5.5	ns	43.45
GETn_ETXD[7:4], ETn_ETXD[3:0] output delay time	t_{GETDD}	0.5	—	5.5	ns	43.45
ETn_RX-CLK cycle time	t_{GRcyc}	8	—	—	ns	43.46
ETn_RX-DV setup time	t_{GRDVS}	2.5	—	—	ns	43.46
ETn_RX-DV hold time	t_{GRDVH}	0.5	—	—	ns	43.46
GETn_ERXD[7:4], ETn_ERXD[3:0] setup time	t_{GERDS}	2.5	—	—	ns	43.46
GETn_ERXD[7:4], ETn_ERXD[3:0] hold time	t_{GERDH}	0.5	—	—	ns	43.46
ETn_RX-ER setup time	t_{GRERS}	2.5	—	—	ns	43.47
ETn_RX-ER hold time	t_{GRERH}	0.5	—	—	ns	43.47
ETn_WOL output delay time	t_{GWOLD}	0	—	18	ns	43.48

- Original table

Table 43.21 Ethernet Controller Signal Timing (RMII)

Conditions: V_{CCQ} = VDD_RTC = AV_{CC} = 3.0 to 3.6 V, $V_{CCQ-DDR}$ = 2.3 to 2.7 V, V_{DD} = 1.15 to 1.35 V, Ta = –20 to 75°C

Item	Symbol	Min.	Typ.	Max.	Unit	Figure
REF50CK cycle time	t_{Rtcyc}	20	—	—	ns	43.49
RMIIn_TXD-EN, RMII1M_TXD-EN output delay time	t_{RTEND}	2.5	—	10	ns	43.49
RMIIn_TXD1, RMIIn_TXD0, RMII1M_TXD1, RMII1M_TXD0 output delay time	t_{RETDD}	2.5	—	10	ns	43.49
RMIIn_CRS_DV, RMII1M_CRS_DV setup time	t_{RRDVS}	4	—	—	ns	43.50
RMIIn_CRS_DV, RMII1M_CRS_DV hold time	t_{RRDVH}	2.5	—	—	ns	43.50
RMIIn_RXD1, RMIIn_RXD0, RMII1M_RXD1, RMII1M_RXD0 setup time	t_{RERDS}	4	—	—	ns	43.50
RMIIn_RXD1, RMIIn_RXD0, RMII1M_RXD1, RMII1M_RXD0 hold time	t_{RERDH}	2.5	—	—	ns	43.50
RMIIn_RX_ER setup time	t_{RRERS}	4	—	—	ns	43.51
RMIIn_RX_ER hold time	t_{RRERH}	2.5	—	—	ns	43.51

- Corrected table

Table 43.21 Ethernet Controller Signal Timing (RMII)

Conditions: V_{CCQ} = VDD_RTC = AV_{CC} = 3.0 to 3.6 V, $V_{CCQ-DDR}$ = 2.3 to 2.7 V, V_{DD} = 1.15 to 1.35 V, Ta = –20 to 75°C

Item	Symbol	Min.	Typ.	Max.	Unit	Figure
REF50CK clock input frequency	f_{RTcyc}	50 – 50ppm	—	50 + 50ppm	MHz	43.49
RMIIn_TXD-EN, RMII1M_TXD-EN output delay time	t_{RTEND}	2.5	—	10	ns	43.49
RMIIn_TXD1, RMIIn_TXD0, RMII1M_TXD1, RMII1M_TXD0 output delay time	t_{RETDD}	2.5	—	10	ns	43.49
RMIIn_CRS_DV, RMII1M_CRS_DV setup time	t_{RRDVS}	4	—	—	ns	43.50
RMIIn_CRS_DV, RMII1M_CRS_DV hold time	t_{RRDVH}	2.5	—	—	ns	43.50
RMIIn_RXD1, RMIIn_RXD0, RMII1M_RXD1, RMII1M_RXD0 setup time	t_{RERDS}	4	—	—	ns	43.50
RMIIn_RXD1, RMIIn_RXD0, RMII1M_RXD1, RMII1M_RXD0 hold time	t_{RERDH}	2.5	—	—	ns	43.50
RMIIn_RX_ER setup time	t_{RRERS}	4	—	—	ns	43.51
RMIIn_RX_ER hold time	t_{RRERH}	2.5	—	—	ns	43.51

4. Correction of Package Dimensions (Page 1914)

- Original description

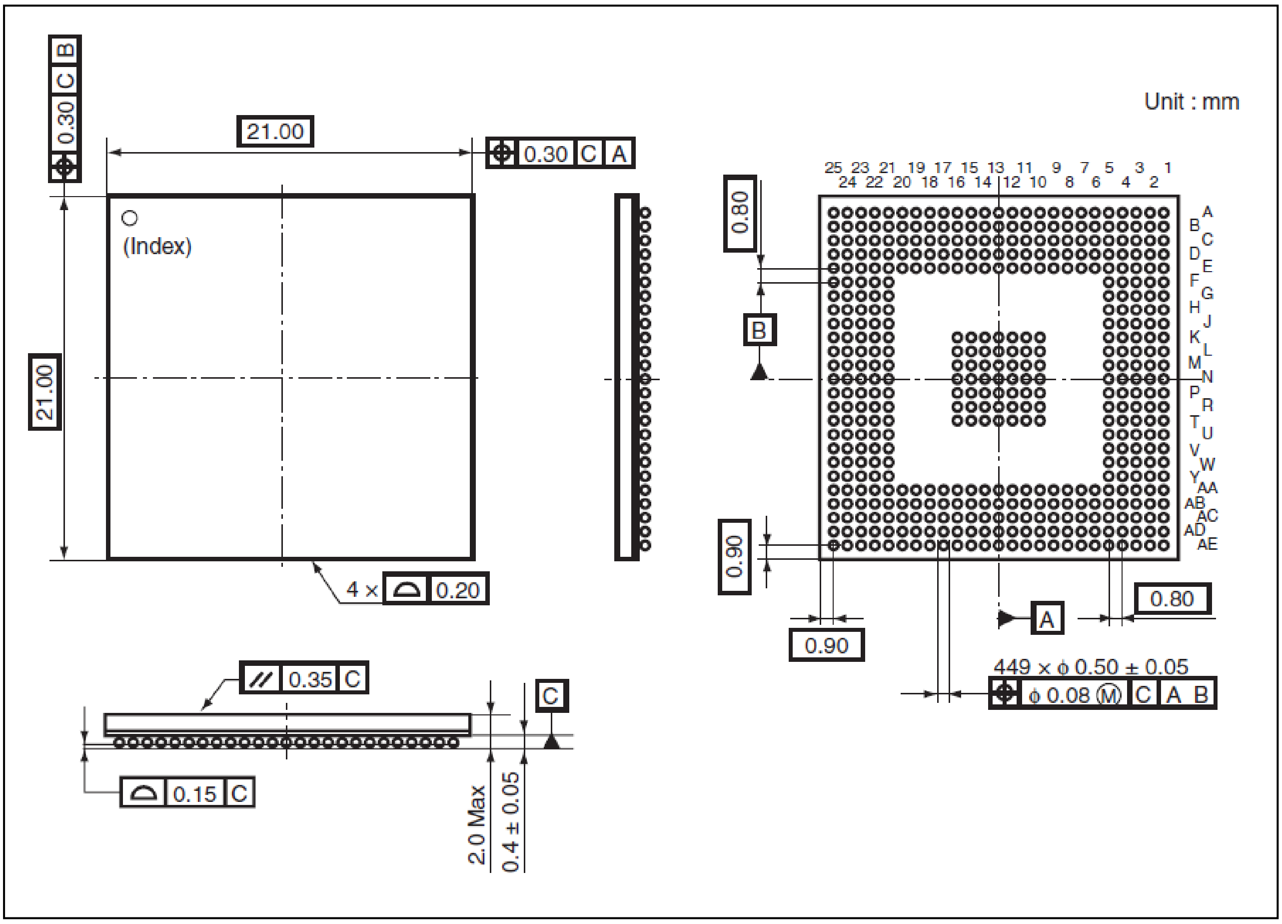


Figure F.1 Package Dimensions (449-Pin)

- Corrected description

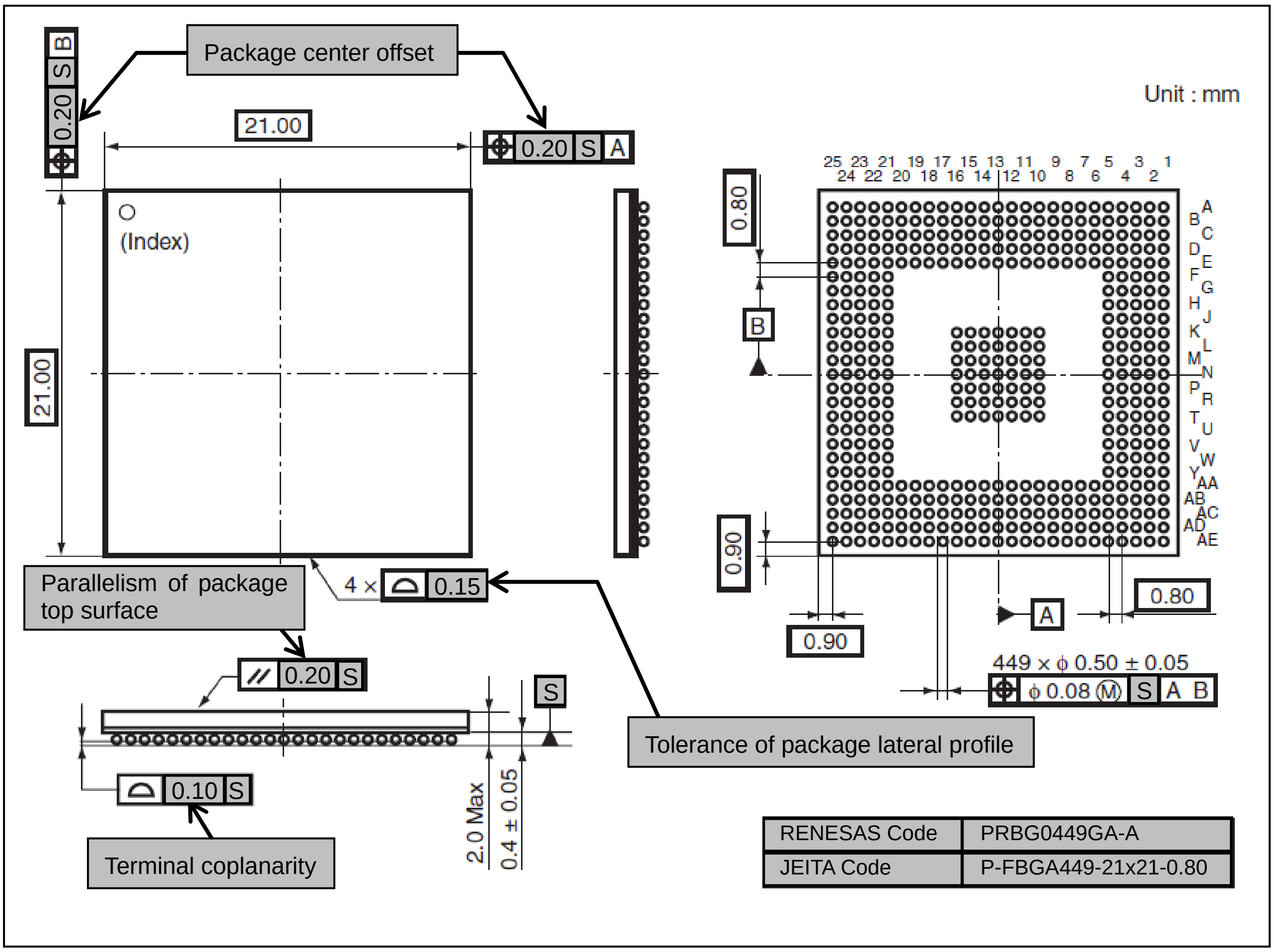


Figure F.1 Package Dimensions (449-Pin)

Table Correction summary

Name	Reference symbol	Symbol	Datum 1st Before correction	Datum 1st After correction	Datum 2nd	Before correction	After correction	Unit
Package center offset	w	⊕	C	S	A	0.30	0.20	mm
			C	S	B	0.30	0.20	mm
Parallelism of package top surface	y1	//	C	S	—	0.35	0.20	mm
Tolerance of package lateral profile	v	⌓	—	—	—	0.20	0.15	mm
Terminal coplanarity	y		C	S	—	0.15	0.10	mm

Note. For the package information, also refer to the “Package Data Book” of Renesas web site.

- End of report -