To our customers,

Old Company Name in Catalogs and Other Documents

On April 1st, 2010, NEC Electronics Corporation merged with Renesas Technology Corporation, and Renesas Electronics Corporation took over all the business of both companies. Therefore, although the old company name remains in this document, it is a valid Renesas Electronics document. We appreciate your understanding.

Renesas Electronics website: http://www.renesas.com

April 1st, 2010
Renesas Electronics Corporation

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RENESAS TECHNICAL UPDATE

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Product Category	MPU&MCU		Document No.	TN-SH7-A538A/E	Rev.	1.0
Title	SH7760 The revision about power-on and power-off procedure.		Information Category	Technical Notification		
Applicable Product	SH7760	Lot No. ALL	Reference Document	SH7760 Hardware Manual (ADE-602-291 Rev.1.0)		

SH7760 Power-On and Power-Off Procedures.

1. Power-on Procedure

(1)Please turn on the power supply of I/O, and CPG to the same timing as a power supply VDDQ.

(2)After turning on a power supply to VDDQ or simultaneously, the input of a signal line (RESET, MRESET, MD0-MD10 , external clock, and etc) must be input. If the signal lines are entered first, the LSI may be damaged.

(i)Please make a RESET signal into a Low level at the power supply VDDQ.

(3) Please turn on the power supply so that the voltage of a power supply VDD may become VDD < 1.2V until the voltage of a power supply VDDQ reaches 2V to avoid the unusual frequency of the PLL1/2/3 circuit.

(4)It recommends that a power supply to VDDQ is in advance, and a power supply to VDD is behind.

(5)In addition to the above (1), (2), (3) and following (i)(ii), please follow “3. The ratings for power-on and power-off”.

(i) In the case of this LSI simple substance, the power supply sequence of a power supply to VDDQ and VDD does not have time restrictions. Please refer to Figure F {Fig. F1}. In addition, it recommends performing a power-on procedure at the shortest possible time.

(ii)When this LSI is connected with other elements on the mounting board, please keep that

-0.3V < Vin < VDDQ+0.3V.

Moreover, as shown in figure F {Fig. F2}, restrictions time until it goes up from the following condition (A) to a operation voltage value {VDDQ (min), VDD (min)} is 100ms (max). It is exceeded, a product may be damaged.

In addition, it recommends performing a power-on procedure at the shortest possible time.

Condition (A) : VDDQ > 1.0V or VDD > 0.5V

2 . Power-off Procedure

(1) Please turn off the power supply of I/O and CPG to the same timing as a power supply VDDQ.
(2) There is no timing regulation of a signal line (RESET and MRESET).
(3) The input level to the pin must be lowered in compliance with the I/O, RTC, CPG power supply voltage.
(4) It recommends that turning off the I/O, RTC, CPG power supply voltage after (or at the same time as) turning off the internal power supply voltage (VDD}.
(5) In addition to the above (1), (2), (3), (4) and following (i)(ii), please follow “3. The ratings for power-on and power-off”.
(i) In the case of this LSI simple substance, the power supply sequence of a power supply to VDDQ and VDD does not have time restrictions. Please refer to Figure F {Fig. F1}. In addition, it recommends performing a power off at the shortest possible time.
(ii) When this LSI is connected with other elements on the mounting board, please keep that
-0.3V < Vin < VDDQ+0.3V.
Moreover, as shown in figure F {Fig. F2}, restrictions time until it goes down from a operation voltage value {VDDQ (min), VDD (min)} to the following condition (B) is 150ms (max).
It is exceeded, a product may be damaged.
In addition, it recommends performing a power off at the shortest possible time.

Condition (B) : VDDQ < 1.0V and VDD < 0.5V

3. The ratings for power-on and power-off

A product may be damaged when not satisfying the conditions of (1), (2), (3) and (4) below.
(1) VDDQ = VDD-CPG = AVCC-ADC
(2) VDD = VDD-PLL1=VDD-PLL2
(3) -0.3V < VDD < VDDQ+0.3V.
-0.3V < VDD-PLL1 < VDDQ+0.3V.
-0.3V < VDD-PLL2 < VDDQ+0.3V.
-0.3V < VDD-PLL3 < VDDQ+0.3V.
(4)VSS = VSSQ = VSS-PLL1=VSS-PLL2 = VSS-PLL3 = VSS-CPG = AVSS-ADC = GND [0V].

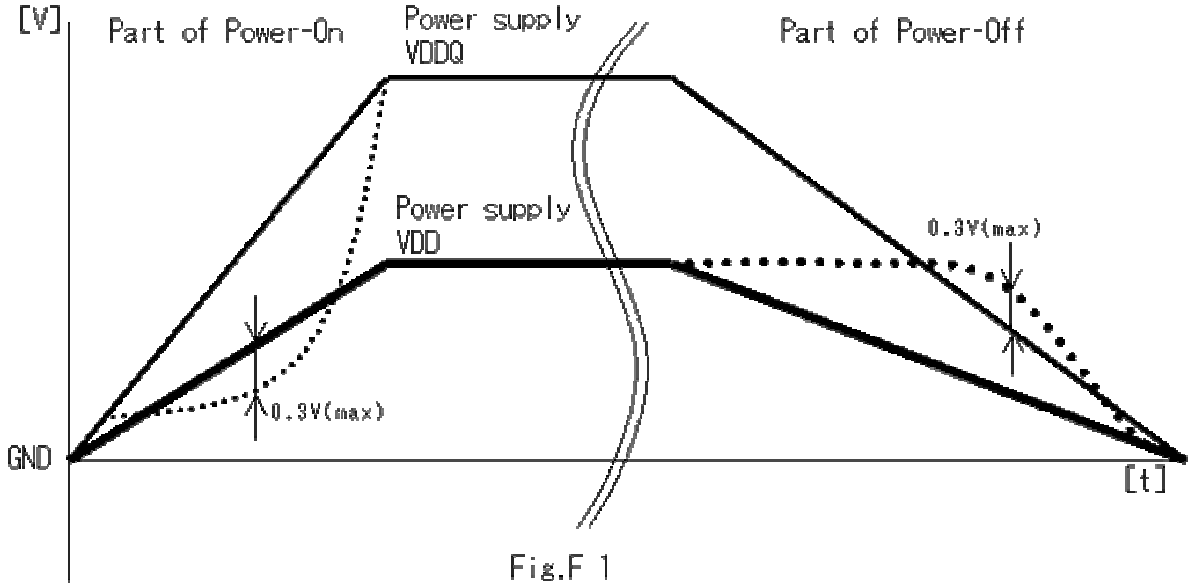

Fig.F 1

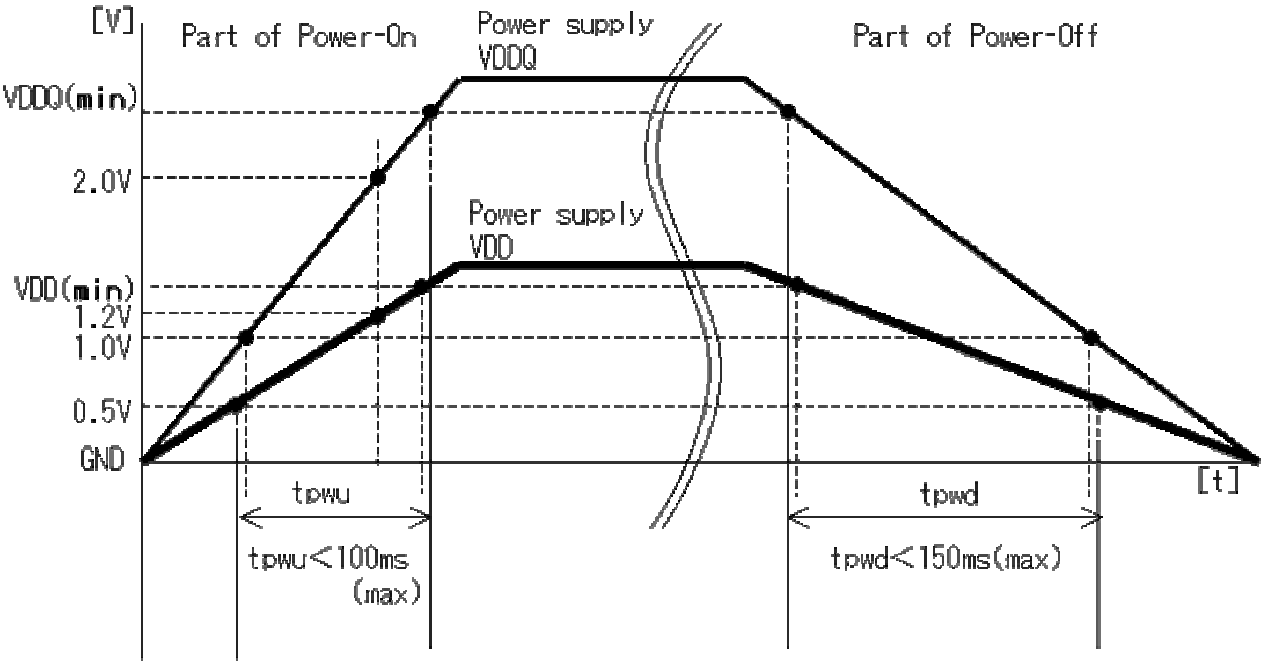

Fig.F 2

Fig.F Power-On and Power-Off procedure