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Renesas Electronics Corporation

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RENESAS TECHNICAL UPD

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Product Category	MPU&MCU		Document No.	TN-SH7-A548A/E	Rev.	1.0
Title	SH7760 New Package Product name		Information Category	Technical Notification		
Applicable Product	SH7760	Lot No. All	Reference Document	SH7760 hardware manual (ADE-602-291 Rev.1.0)		

The followings are the information of a new package product of SH7760(HD6417760) .

1. new product names / specification

(1) New products' pin arrangement refer to Appendix 1, 2.

(2) Package dimensions is 17mm×17mm. Please refer to Appendix 3.

(3) Mark example refer to Appendix 4.

(3) DC characteristics and AC characteristics are as same as that of the current product(HD6417760BP200AD).

(4) The following shows new products' "Operating temperature" and "Solder ball".

New product name	Operating temperature	Solder ball
HD6417760BL200A	-20°C ~ 75°C	include lead (Sn-Pb)
HD6417760BL200AV	-20°C ~ 75°C	Pb-free
HD6417760BL200AD	-40°C ~ 85°C	include lead (Sn-Pb)
HD6417760BL200ADV	-40°C ~ 85°C	Pb-free

Appendix 1 Pin arrangement of BP-256B(17mm X 17mm) version

shows the difference between BP-256F package version and BP-256B(V) package version.

	1	2	3	4	5	6	7	8	9	10	11	12	13	14	15	16	17	18	19	20	
A	EXTAL	XTAL	VDD-CPG	VDD-PLL1	SSID_SCK/HAC_SD_IN0/BS2#	HSPI_TX/SIM_D/MCDAT	HSPI_CLK/SIM_CLK/MCCLK	CMT_CTR1	CMT_CTR3	SCIF2_CLK	SCIF2_TXD	SCIF2_RXD	SCIF2_CTS#	SCIF2_RTS#	SCIF0_CLK	SCIF0_TXD	MD4/CE2B#	DACK0	VDD-PLL3	UCLK	A
B	RESET#	VSS-CPG	VDD-PLL2	VSS-PLL1	SSID_WS/HAC_SYNC0	HSPI_RX	HSPI_CS#/SIM_RST/MCMD	CMT_CTR0/TCLK	CMT_CTR2	NMI	SCIF1_CLK	SCIF1_TXD	SCIF1_RXD	SCIF1_CTS#	SCIF1_RTS#	SCIF0_RXD	MD3/CE2A#	VSS-PLL3	USB_DM	VDDQ	B
C	RDY#	HAC_BIT_CLK0	VSS-PLL2	HAC_RES#	SSID_SDATA/HAC_SD_OUT0	SSII_SDATA/HAC_SD_OUT1	VDD	ASEBRK#/BRKACK	VDDQ	TMS	VDDQ	TDO	VDDQ	VDD	TCK	MD2	DRAK0	USB_PENC	VSSQ	USB_DP	C
D	DCK	SSII_SCK/HAC_SD_IN1	SSII_WS/HAC_SYNC1	HAC_BIT_CLK1	MRESET#	STATUS0	VSS	STATUS1	VSSQ	TRST#	VSSQ	TDI	VSSQ	VSS	VSSQ	MD0	MD1	DRAK1	DACK1	USB_OVC#	D
E	MFI-D8/LCD_DATA8	VEPWC/IRQ5#	CA	BREQ#													VSSQ	VDDQ	DREQ0#	DREQ1#	E
F	MFI-D9/LCD_DATA9	MFI-D0/LCD_DATA0	CS0#	VCPWC/IRQ4#													I2C1_SCL	I2C1_SDA	I2C0_SCL	I2C0_SDA	F
G	MFI-D10/LCD_DATA10	MFI-D1/LCD_DATA1	VDD	VSS													VSS	VDD	MD6/DIS16#	MD5	G
H	CS1#	MFI-D2/LCD_DATA2/IRQ6#	VDDQ	VSSQ				TOP									MD7	MD8	Reserved/AUDCK	Reserved/AUDSYNC	H
J	MFI-D11/LCD_DATA11	MFI-D3/LCD_DATA3/IRQ7#	CS2#	BACK#													VSSQ	VDDQ	Reserved/AUDATA[2]	Reserved/AUDATA[3]	J
K	MFI-D12/LCD_DATA12	CS4#	MFI-D4/LCD_DATA4/DREQ2#	VSSQ													Avss_ADC	Avcc_ADC	ADTRG#/AUDATA[0]	Reserved/AUDATA[1]	K
L	MFI-D13/LCD_DATA13	MFI-D6/LCD_DATA6/DREQ3#	MFI-D5/LCD_DATA5/DRAK2/DACK2	A20													AN3	AN2	AN1	AN0	L
M	MFI-D14/LCD_DATA14	MFI-D7/LCD_DATA7/DRAK3/DACK3	A21	VDDQ													VSSQ	VDDQ	IRL3#	IRL2#	M
N	CS5#	MFI-INT#/LCD_CLK	MFI-CS#/LCD_DON	VSSQ													VSSQ	VDDQ	IRL1#	IRL0#	N
P	MFI-D15/LCD_DATA15	CS6#	VSS	VDD													VSS	VDD	CAN0_NERR/AUDCK	CAN1_NERR/AUDSYNC	P
R	A1	BS#	MFI-E/LCD_CL1	A0													A24	A25	CAN0_RX/AUDATA[2]	CAN1_RX/AUDATA[3]	R
T	MFI-RW/LCD_FLM	MFI-RS/LCD_M_DISP	D11	MFI-MD/LCD_CL2													A22	A23	CAN0_TX/AUDATA[0]	CAN1_TX/AUDATA[1]	T
U	D15	D0	D3	VDDQ	VSSQ	CKE	VSS	VSSQ	A17	VSSQ	VSSQ	VSSQ	A18	VSS	A19	VSSQ	D20	D28	D16	D31	U
V	D14	D1	VDDQ	D10	VDDQ	A2	VDD	VDDQ	A7	VDDQ	VDDQ	VDDQ	A15	VDD	A16	VDDQ	D21	VDDQ	D17	D30	V
W	D2	VSSQ	D4	D6	D7	RD/WR#	WE0#/DQM0/REG#	A4	A6	A8	A10	A12	A14	WE2#/DQM2/ICIORD#	RAS#	D24	D25	D27	VSSQ	D29	W
Y	D13	D12	D5	D9	D8	RD#/CASS#/FRAME#	WE1#/DQM1	A3	A5	CKD	A9	A11	A13	WE3#/DQM3/ICIOWR#	CS3#	D23	D22	D26	D19	D18	Y
	1	2	3	4	5	6	7	8	9	10	11	12	13	14	15	16	17	18	19	20	

Appendix 2 17mm x 17mm (BP-256B) Pin arrangement

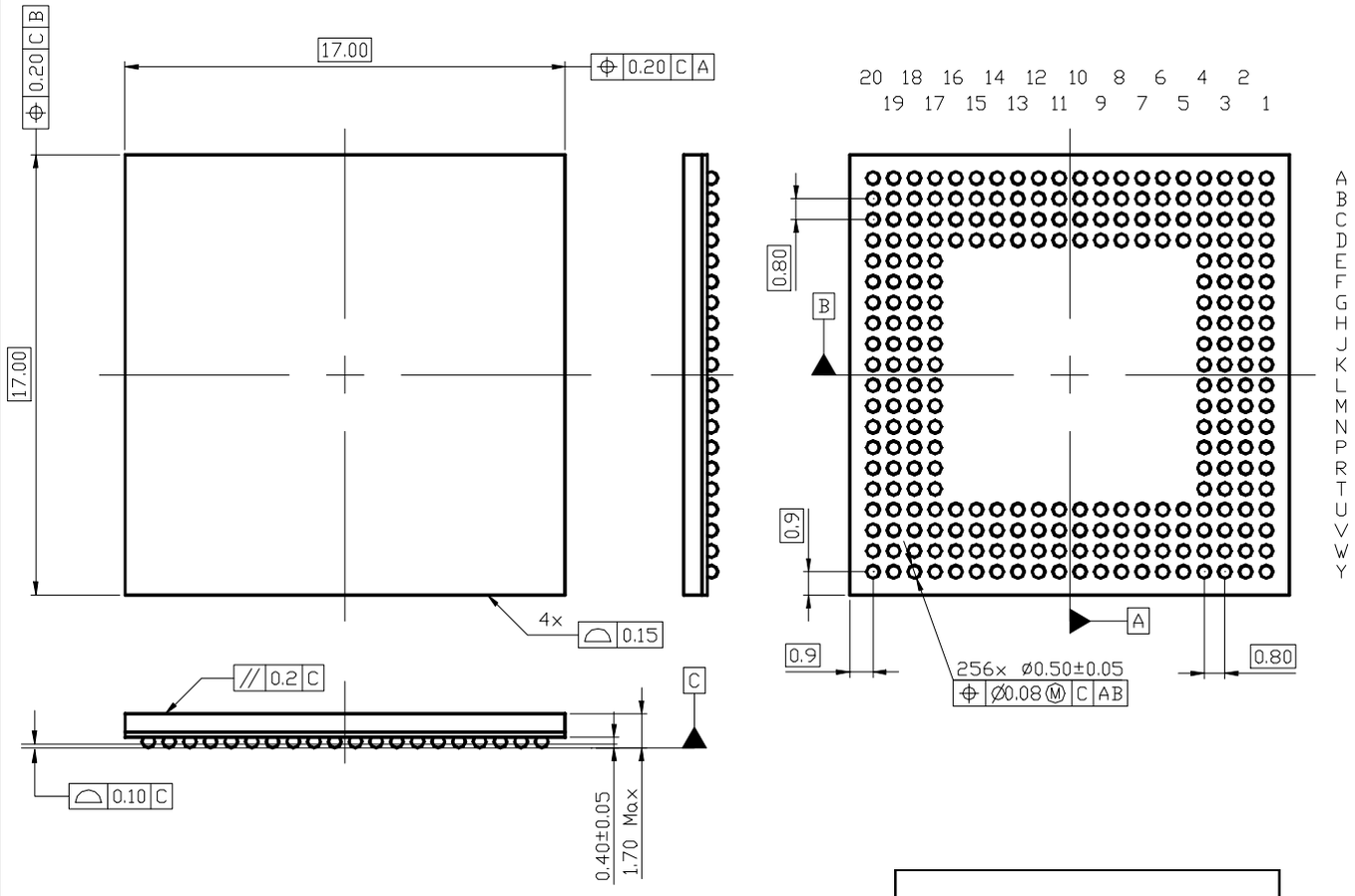
Pin No.	Pin Name
A1	EXTAL
A2	XTAL
A3	VDD-CPG
A4	VDD-PLL1
A5	SSI0_SCK/HAC_SD_IN0/BS2#
A6	HSPI_TX/SIM_D/MCDAT
A7	HSPI_CLK/SIM_CLK/MCCLK
A8	CMT_CTR1
A9	CMT_CTR3
A10	SCIF2_CLK
A11	SCIF2_TXD
A12	SCIF2_RXD
A13	SCIF2_CTS#
A14	SCIF2_RTS#
A15	SCIF0_CLK
A16	SCIF0_TXD
A17	MD4/CE2B#
A18	DACK0
A19	VDD-PLL3
A20	UCLK
B1	RESET#
B2	VSS-CPG
B3	VDD-PLL2
B4	VSS-PLL1
B5	SSI0_WS/HAC_SYNC0
B6	HSPI_RX
B7	HSPI_CS#/SIM_RST/MCCMD
B8	CMT_CTR0/TCLK
B9	CMT_CTR2
B10	NMI
B11	SCIF1_CLK
B12	SCIF1_TXD
B13	SCIF1_RXD
B14	SCIF1_CTS#
B15	SCIF1_RTS#
B16	SCIF0_RXD
B17	MD3/CE2A#
B18	VSS-PLL3
B19	USB_DM
B20	VDDQ
C1	RDY#
C2	HAC_BIT_CLK0
C3	VSS-PLL2
C4	HAC_RES#
C5	SSI0_SDATA/HAC_SD_OUT0
C6	SSI1_SDATA/HAC_SD_OUT1
C7	VDD
C8	ASEBRK#/BRKACK
C9	VDDQ
C10	TMS
C11	VDDQ
C12	TDO
C13	VDDQ
C14	VDD
C15	TCK
C16	MD2
C17	DRAK0
C18	USB_PENC
C19	VSSQ
C20	USB_DP
D1	DCK
D2	SSI1_SCK/HAC_SD_IN1
D3	SSI1_WS/HAC_SYNC1
D4	HAC_BIT_CLK1

Pin No.	Pin Name
D5	MRESET#
D6	STATUS0
D7	VSS
D8	STATUS1
D9	VSSQ
D10	TRST#
D11	VSSQ
D12	TDI
D13	VSSQ
D14	VSS
D15	VSSQ
D16	MD0
D17	MD1
D18	DRAK1
D19	DACK1
D20	USB_OVC#
E1	MFI-D8/LCD_DATA8
E2	VEPWC/IRQ5#
E3	CA
E4	BREQ#
E17	VSSQ
E18	VDDQ
E19	DREQ0#
E20	DREQ1#
F1	MFI-D9/LCD_DATA9
F2	MFI-D0/LCD_DATA0
F3	CS0#
F4	VCPWC/IRQ4#
F17	I2C1_SCL
F18	I2C1_SDA
F19	I2C0_SCL
F20	I2C0_SDA
G1	MFI-D10/LCD_DATA10
G2	MFI-D1/LCD_DATA1
G3	VDD
G4	VSS
G17	VSS
G18	VDD
G19	MD6/IOIS16#
G20	MD5
H1	CS1#
H2	MFI-D2/LCD_DATA2/IRQ6#
H3	VDDQ
H4	VSSQ
H17	MD7
H18	MD8
H19	Reserved/AUDCK
H20	Reserved/AUDSYNC
J1	MFI-D11/LCD_DATA11
J2	MFI-D3/LCD_DATA3/IRQ7#
J3	CS2#
J4	BACK#
J17	VSSQ
J18	VDDQ
J19	Reserved/AUDATA[2]
J20	Reserved/AUDATA[3]
K1	MFI-D12/LCD_DATA12
K2	CS4#
K3	MFI-D4/LCD_DATA4/DREQ2#
K4	VSSQ
K17	Avss_ADC
K18	Avcc_ADC
K19	ADTRG#/AUDATA[0]
K20	Reserved/AUDATA[1]

Pin No.	Pin Name
L1	MFI-D13/LCD_DATA13
L2	MFI-D6/LCD_DATA6/DREQ3#
L3	MFI-D5/LCD_DATA5/DRAK2/DACK2
L4	A20
L17	AN3
L18	AN2
L19	AN1
L20	AN0
M1	MFI-D14/LCD_DATA14
M2	MFI-D7/LCD_DATA7/DRAK3/DACK3
M3	A21
M4	VDDQ
M17	VSSQ
M18	VDDQ
M19	IRL3#
M20	IRL2#
N1	CS5#
N2	MFI-INT#/LCD_CLK
N3	MFI-CS#/LCD_DON
N4	VSSQ
N17	VSSQ
N18	VDDQ
N19	IRL1#
N20	IRL0#
P1	MFI-D15/LCD_DATA15
P2	CS6#
P3	VSS
P4	VDD
P17	VSS
P18	VDD
P19	CAN0_NERR/AUDCK
P20	CAN1_NERR/AUDSYNC
R1	A1
R2	BS#
R3	MFI-E/LCD_CL1
R4	A0
R17	A24
R18	A25
R19	CAN0_RX/AUDATA[2]
R20	CAN1_RX/AUDATA[3]
T1	MFI-RW/LCD_FLM
T2	MFI-RS/LCD_M_DISP
T3	D11
T4	MFI-MD/LCD_CL2
T17	A22
T18	A23
T19	CAN0_TX/AUDATA[0]
T20	CAN1_TX/AUDATA[1]
U1	D15
U2	D0
U3	D3
U4	VDDQ
U5	VSSQ
U6	CKE
U7	VSS
U8	VSSQ
U9	A17
U10	VSSQ
U11	VSSQ
U12	VSSQ
U13	A18
U14	VSS
U15	A19
U16	VSSQ

Pin No.	Pin Name
U17	D20
U18	D28
U19	D16
U20	D31
V1	D14
V2	D1
V3	VDDQ
V4	D10
V5	VDDQ
V6	A2
V7	VDD
V8	VDDQ
V9	A7
V10	VDDQ
V11	VDDQ
V12	VDDQ
V13	A15
V14	VDD
V15	A16
V16	VDDQ
V17	D21
V18	VDDQ
V19	D17
V20	D30
W1	D2
W2	VSSQ
W3	D4
W4	D6
W5	D7
W6	RD/WR#
W7	WE0#/DQM0/REG#
W8	A4
W9	A6
W10	A8
W11	A10
W12	A12
W13	A14
W14	WE2#/DQM2/ICIORD#
W15	RAS#
W16	D24
W17	D25
W18	D27
W19	VSSQ
W20	D29
Y1	D13
Y2	D12
Y3	D5
Y4	D9
Y5	D8
Y6	RD#/CASS#/FRAME#
Y7	WE1#/DQM1
Y8	A3
Y9	A5
Y10	CKIO
Y11	A9
Y12	A11
Y13	A13
Y14	WE3#/DQM3/ICIOWR#
Y15	CS3#
Y16	D23
Y17	D22
Y18	D26
Y19	D19
Y20	D18

Appendix 3 17mm x 17mm (BP-256B/BP-256BV) Package dimension



Package code:

BP-256B (include lead (Sn-Pb))

BP-256BV (Pb-free)

Appendix 4 Mark example

The letter surrounded in ☐ is the difference in the mark example.

HD6417760BL200A Mark example

HD6417760BL200AV Mark example

HD6417760BL200AD Mark example

HD6417760BL200ADV Mark example