HITACHI MICROCOMPUTER TECHNICAL UPDATE

DATE	11 October 2000	No.	TN-SH7-262A/E
THEME	SH7729/SH7709A usage notice when using DMAC		
CLASSIFICATION	☐ Spec. change ☐ Supplement of Documents	☐ Limitation on Use	
PRODUCT NAME	HD6417709A, SH7729		
REFERENCE DOCUMENTS	SH7709A Hardware manual SH7729 Hardware manual	Effective From	Eternity

HD6417729 and HD6417709A have followed usage notice

1. Conditions and phenomenon

The register value may not correct if reading or writing to registers which connected to I bus during DMA transfer. The problem will not happen if clock ratio of internal clock (I clock) to external clock (B clock) is 1 or 2. And the write access problem may happen only on the Bus State Controller registers.

The summary of problem conditions are shown in Table 1,2 and 3.

Table 1.The relationship between the clock ratio and problem

Ratio of Internal clock (I clock) / External clock (B clock)	Problem
x1, x2	Problem will not happen
x3, x4, x6, x8	Problem may happen

Table 2.The relationship between the DMA transfer mode and the possibilities of occurring problem during data transfer

		request mode	
		auto request mode	other request mode
DMA transfer mode	cycle steal mode	only first data of transfer	every data of
	burst mode	only first data of transfer	only first data of transfer

Table 3.The modules connected to I bus and access limitation when problem occurs

	Module
Only read	INTC,CPG,H-UDI,X/Y memory (SH7729 only)
Read and write	BSC

The registers of modules connected I bus are shown below.

Interrupt Controller (INTC):
INTEVT2, IRR0, IRR1, IRR2, ICR0, ICR1, ICR2, PINTER, IPRC, IPRA, IPRB, IPRC, IPRD, IPRE

Clock Pulse Generator (CPG):
FRQCR, STBCR, STBCR2, WTCNT, WTCSR

Bus State Controller (BSC):
BCR1, BCR2, WCR1, WCR2, MCR, DCR, PCR, TCSR, RTCNT, RTCOR, RFCR, BCR3, MCSCR0, MCSCR1, MCSCR2, MCSCR3, MCSCR4, MCSCR5, MCSCR6, MCSCR7

Hitachi-User Debug Interface (H-UDI):
SDIR, SDSR, SDDR/SDDRH, SDDRL, SDAR, SDARE

X/Y memory (only SH7729)
CPU access from X/Y memory as P0,P3 or U0 space.

2. Note on usage

Please stop DMA data transfer when accessing to I bus registers.
Or please make software modification shown below.

2.1 When ratio of internal clock (I clock) to external clock (B clock) is 3.
Please follow instruction (1),(2) and (3). Figure 1 in page 3 shows the software example which satisfies (1),(2) and (3).

(1) The command (a) which is reading from h'A0000000 and the command (b) which is reading from I bus registers should be executed continuously.
(2) The command (a) and (b) should be placed in cacheable area, and the command (a) should be placed in the address 4n+2. And the commands (a) and (b) must be in same 16 byte boundary.
[Example of reading INTEVT2]

```
                Address     Mnemonic
Command(a)      0xxxxxxA    mov.l   @r0,r2   ; The value of R0 is h'A0000000
Command(b)      0xxxxxxC    mov.l   @r1,r4   ; The value of R1 is h'A4000000 (Address of INTEVT2)
```

(3) No interrupts or exceptions should not be occurred between the commands (a) and (b). The settings of prohibiting interrupts are shown in Table 4.

2.2 When ratio of internal clock (I clock) to external clock (B clock) is 4,6 or 8.
Please follow instruction (1),(2) and (3). Figure 2 in page 4 shows the software example which satisfies (1),(2) and (3).

(1) The command (a) which is from h'A0000000 and the command (b) which is reading from I bus registers should be executed continuously.
(2) The command (a) should be placed in the address 4n.
[Example of reading INTEVT2]

```
                Address     Mnemonic
Command(a)      xxxxxxx8    mov.l   @r0,r2   ; The value of R0 is h'A0000000
Command(b)      xxxxxxxA    mov.l   @r1,r4   ; The value of R1 is h'A4000000 (Address of INTEVT2)
```

(3) No interrupts or exceptions should not be occurred between commands (a) and (b). The settings of prohibiting interrupts are shown in Table 4.

Table 4.The register settings and interrupt acceptance

CPU/SR.BL bit	INTC/ICR1.BLMASK bit	Interrupt acceptance
BL=0	—	Do not occur interrupt between command(a) and (b)
BL=1	BLMASK=0	All interrupts are not accepted
	BLMASK=1	Do not occur NMI interrupt between command(a) and (b)

```
 1 AC400000                      1           .org    h'ac400000
 2                               2
 3                               3    ; set ccr = 1
 4 AC400000 E1EC                 4           mov.b   #h'ec,r1
 5 AC400002 E001                 5           mov.b   #h'01,r0
 6 AC400004 2102                 6           mov.l   r0,@r1
 7                               7
 8                               8    ; set sr.bl=1
 9 AC400006 0002                 9           stc     sr,r0
10 AC400008 D106                10           mov.l   #h'10000000,r1
11 AC40000A 201B                11           or      r1,r0
12 AC40000C 403E                12           ldc     r0,ssr
13                              13
14                              14    ; set spc
15 AC40000E D006                15           mov.l   #h'0c400102,r0
16 AC400010 404E                16           ldc     r0,spc
17                              17
18                              18    ; set intc/icr1.blmask = 0
19 AC400012 D106                19           mov.l   #h'a4000010,r1
20 AC400014 9004                20           mov.w   #h'1000,r0
21 AC400016 2101                21           mov.w   r0,@r1
22                              22
23 AC400018 D205                23           mov.l   #h'a4000000,r2
24 AC40001A D306                24           mov.l   #h'a0000000,r3
25                              25
26 AC40001C 002B                26           rte
27 AC40001E 0009                27           nop
28                              28
29                                   ***** BEGIN-POOL *****
30 AC400020 1000                     DATA FOR SOURCE-LINE 20
31 AC400022 0000                     ALIGNMENT CODE
32 AC400024 10000000                 DATA FOR SOURCE-LINE 10
33 AC400028 0C400102                 DATA FOR SOURCE-LINE 15
34 AC40002C A4000010                 DATA FOR SOURCE-LINE 19
35 AC400030 A4000000                 DATA FOR SOURCE-LINE 23
36 AC400034 A0000000                 DATA FOR SOURCE-LINE 24
37                                   ***** END-POOL *****
38 0C400102                     29           .org    h'0c400102
39 0C400102 6432                30           mov.l   @r3,r4  ; dummy read
40 0C400104 6022                31           mov.l   @r2,r0  ; read from intc
41                              32
42                              33
43                              34           .pool
44                              35           .end
```

Figure 1 : Software example(when ratio of internal clock (I clock) to external clock (B clock) is 3)

```
 1 AC400000                      1           .org    h'ac400000
 2                               2
 3                               3    ; set sr.bl=1
 4 AC400000 0002                 4           stc     sr,r0
 5 AC400002 D10A                 5           mov.l   #h'10000000,r1
 6 AC400004 201B                 6           or      r1,r0
 7 AC400006 403E                 7           ldc     r0,ssr
 8                               8
 9                               9    ; set spc
10 AC400008 D009                10           mov.l   #h'ac400020,r0
11 AC40000A 404E                11           ldc     r0,spc
12                              12
13                              13    ; set intc/icr1.blmask = 0
14 AC40000C D109                14           mov.l   #h'a4000010,r1
15 AC40000E 900B                15           mov.w   #h'1000,r0
16 AC400010 2101                16           mov.w   r0,@r1
17                              17
18 AC400012 D209                18           mov.l   #h'a4000000,r2
19 AC400014 D309                19           mov.l   #h'a0000000,r3
20                              20
21 AC400016 002B                21           rte
22 AC400018 0009                22           nop
23                              23           .nopool
24                              24
25 AC400020                     25           .org    h'ac400020
26 AC400020                     26    label
27 AC400020 6432                27           mov.l   @r3,r4  ; dummy read
28 AC400022 6022                28           mov.l   @r2,r0  ;read from intc
29                              29
30                              30
31                              31           .pool
32                                    ***** BEGIN-POOL *****
33 AC400024 A00C                      BRA TO END-POOL
34 AC400026 0009                      NOP
35 AC400028 1000                      DATA FOR SOURCE-LINE 15
36 AC40002A 0000                      ALIGNMENT CODE
37 AC40002C 10000000                  DATA FOR SOURCE-LINE 5
38 AC400030 AC400020                  DATA FOR SOURCE-LINE 10
39 AC400034 A4000010                  DATA FOR SOURCE-LINE 14
40 AC400038 A4000000                  DATA FOR SOURCE-LINE 18
41 AC40003C A0000000                  DATA FOR SOURCE-LINE 19
42                                    ***** END-POOL *****
43                              32           .end
```

Figure 2 : Software example(when ratio of internal clock (I clock) to external clock (B clock) is 4,6 or 8)