

HITACHI SEMICONDUCTOR TECHNICAL UPDATE

DATE	1 December 2000	No.	TN-SH7-280A /E
THEME	SH7729/SH7709A usage notice about DACK when usingDMAC(No.2)		
CLASSIFICATION	<input type="checkbox"/> Spec. change <input type="checkbox"/> Supplement of Documents <input checked="" type="checkbox"/> Limitation on Use		
PRODUCT NAME	HD6417709A, SH7729		
REFERENCE DOCUMENTS	SH7709A Hardware manual SH7729 Hardware manual	Effective Date	Eternity
		From	

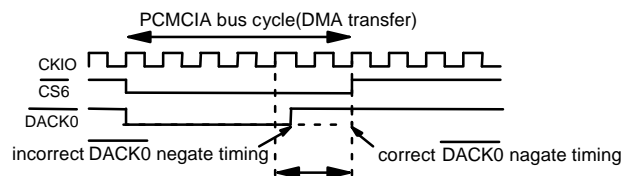
HD6417729 and HD6417709A have followed usage notice

1. condition and phenomenon

- Using PCMCIA (A5(6)PCM in BCR is set to 1)
- A5(6)TEH[2:0] in PCR is set to other than 3'b000

On above conditions,

- (A) When source or destination of DMA transfer is PCMCIA and DACK is set to be output at PCMCIA cycle, negate timing of DACK0/1 may be incorrect. DACK negate timing depends on A5(6)TEH[2:0]. DACK is nagated at most A5(6)TEH[2:0] cycles shorter than the correct timing.

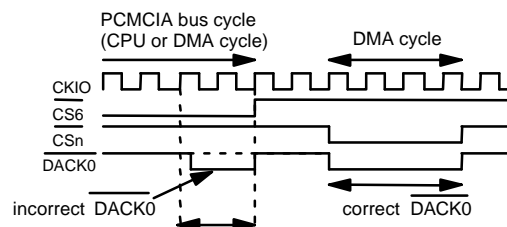


In the case that A6TEH is 3'b010, DACK is nagated at most 2 cycles shorter than the correct case.

figure 1. An example of timing diagram that DACK is nagated faster (the case that A6TEH is 3'b010)

- (B) (Same as TN-SH7-254B/E)

When a PCMCIA bus cycle is followed by a bus cycle with asserting DACK0/1, DACK0/1 may be incorrectly asserted in the PCMCIA bus cycle. The width of incorrect DACK0/1 depends on A5(6)TEH[2:0]. The max width of incorrect DACK0/1 cycle is value of A5(6)TEH[2:0]. This incorrect DACK is independant from whether DACK0/1 is asserted in the PCMCIA bus cycle or not.



In the case that A6TEH is 3'b010, DACK is asserted at most 2cycles.

figure 2. An example of the timing diagram that DACK is incorrectly asserted (the case that A6TEH is 3'b010)

2. work around

Work around of (A) and (B)

- Please don't use PCMCIA and DMAC at the same time.
- When you use PCMCIA and DMAC at the same time, please set A5(6)TEH[2:0] to 3'b000.

Work around of (A)

- Please set AM bit in CHCRn to the setting that DACK is asserted in PCMCIA cycle.

Work around of (B)

- Please fix DACK to high during PCMCIA bus cycle.

3. Notes

Even if the DACK is negated incorrectly, other signals for DMA are generated correctly.

Even if the DACK is asserted incorrectly, DMA bus cycle never be generated while the incorrect DACK signal is asserted.