To our customers,

Old Company Name in Catalogs and Other Documents

On April 1st, 2010, NEC Electronics Corporation merged with Renesas Technology Corporation, and Renesas Electronics Corporation took over all the business of both companies. Therefore, although the old company name remains in this document, it is a valid Renesas Electronics document. We appreciate your understanding.

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April 1st, 2010
Renesas Electronics Corporation

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Date: Jun.23.2005

RENESAS TECHNICAL UPDATE

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RenesasTechnology Corp.

Product Category	MPU&MCU		Document No.	TN-SH7-A556A/E	Rev.	1.00
Title	SH7720 hardware manual revision up		Information Category	Technical Notification		
Applicable Product	SH3-DSP SH7700 Series SH7720 Group	Lot No. All	Reference Document	SH7720 hardware manual (REJ09B0033-0100 Rev.1.00) (REJ09B0033-0200 Rev.2.00)		

SH7720 Hardware Manual is revised from Rev.1.00. to Rev.2.00

Please refer to main revisions and additions in Rev. 2.00 as shown in the following.

Item	Page	Revision (See Manual for Details)
Section 1 Overview 1.1 Features Table 1.1 SH7720 Features	4, 8	Amended **Item** / **Features** Clock pulse generator (CPG): • Generates three types of clocks — CPU clock: Maximum 133.34 MHz — Bus clock: Maximum 66.67 MHz — Peripheral clock: Maximum 33.34 MHz Product lineup: **Abb.** / **Operating Frequency** / **Product Code** / **Package** SH7720 / 133.34 MHz / HD6417720BP133C / 256-pin CSP (PLBG0256GA-A (BP-256H)) HD6417720BP133CV / 256-pin CSP (PLBG0256GA-A (BP-256HV)) HD6417720BL133C / 256-pin CSP (PLBG0256KA-A (BP-256C)) HD6417720BL133CV / 256-pin CSP (PLBG0256KA-A (BP-256CV))
1.3 Pin Assignments 1.3.1 Pin Assignments Figure 1.2 Pin Assignments (PLBG0256GA-A (BP-256H/HV))	10	Added PLBG0256GA-A BP-256HV BP-256H C18 → USB1d_TXDPLS/AFE_SCLK/IOIS16/PCC_IOIS16/PTG4 Amended J17 → MMC_CMD/SIOF1_RxD/TPU_TI2B/PTU1

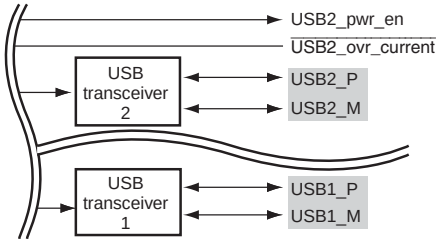
<table>
<tr><th>Item</th><th>Page</th><th>Revision (See Manual for Details)</th></tr>
<tr><td>Figure 1.3 Pin Assignments (PLBG0256KA-A (BP-256C/CV))</td><td>11</td><td>Added
PLBG0256KA-A
BP-256CV
BP-256C
E18 → USB1d_TXDPLS/AFE_SCLK/IOIS16/PCC_IOIS16/PTG4
Amended
K17 → MMC_CMD/SIOF1_RxD/TPU_TI2B/PTU1</td></tr>
<tr><td>Table 1.2 List of Pin Assignments</td><td>12 to 23</td><td>Headings of pin number columns amended
BP-256H → PLBG0256GA-A
BP-256C → PLBG0256KA-A</td></tr>
<tr><td></td><td>14 to 18</td><td>Amended
<table>
<tr><th>Pin No. (PLBG0256GA-A)</th><th>Pin No. (PLBG0256KA-A)</th><th>Pin Name</th><th>Function</th><th>I/O</th><th>I/O Buffer Power Supply</th></tr>
<tr><td>C18</td><td>E18</td><td>USB1d_TXDPLS/ AFE_SCLK/ IOIS16/ PCC_IOIS16/ PTG4</td><td>D+ transmit output/shift clock/16-bit IO/write protection/general-purpose port</td><td>O/I/I/I/IO</td><td>VccQ</td></tr>
<tr><td>G20</td><td>J20</td><td>SIM_CLK/SCIF1_ SCK/PTV0</td><td>Clock output/serial clock/ general-purpose port</td><td>O/IO/IO</td><td>VccQ</td></tr>
<tr><td>J17</td><td>K17</td><td>MMC_CMD/ SIOF1_RxD/ TPU_TI2B/ PTU1</td><td>MMC command output/response input/receive data/ clock input/general-purpose port</td><td>IO/I/I/IO</td><td>VccQ</td></tr>
<tr><td>J20</td><td>L17</td><td>SCIF0_RTS/TPU_ TO0/PTT3</td><td>Transmit request/timer output/general-purpose port</td><td>O/O/IO</td><td>VccQ</td></tr>
<tr><td>L19</td><td>N17</td><td>SCIF0_SCK/PTT0</td><td>Serial clock/general-purpose port</td><td>IO/IO</td><td>VccQ</td></tr>
</table></td></tr>
</table>

Item	Page	Revision (See Manual for Details)
1.3.2 Pin Functions Table 1.3 SH7720 Pin Functions	29 to 34	Amended

Classification	Symbol	I/O	Name	Function
Realtime clock (RTC)	VccQ_RTC	—	RTC power supply	Power supply pin for the RTC (3.3 V)
	Vcc_RTC	—	RTC power supply	Power supply pin for the RTC (1.5 V)
	Vss_RTC	—	RTC ground	Ground pin for the RTC.
	EXTAL_RTC	I	RTC external clock	Connects crystal resonator for the RTC. Also used to input external clock for the RTC.
	XTAL_RTC	O	RTC crystal	Connects crystal resonator for the RTC
USB	EXTAL_USB	I	USB external clock	Connects crystal resonator for USB. Also used to input external clock for USB (48 MHz)

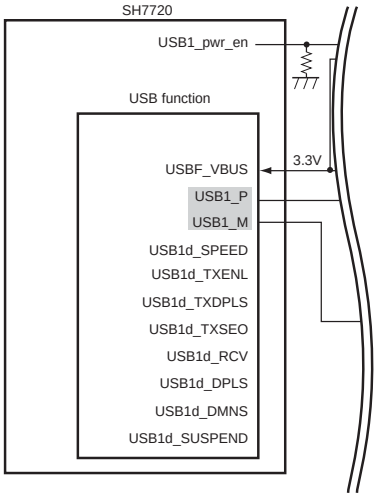
Notes:
1. All Vcc/Vss/VccQ/VssQ/VccQ1/VssQ1/Avcc/Avss/Avcc_USB/Avss_USB/VccQ_RTC/Vcc_RTC/Vss_RTC/Vcc_PLL1/Vss_PLL1/Vcc_PLL2/Vss_PLL2 should be connected to the system power supply (so that power is supplied at all times.) In hardware standby mode, the power supply to other than Vcc_RTC and VccQ_RTC can be turned off (section 13.8).
2. Always supply power to the Vcc_RTC and VccQ_RTC, even if the RTC is not being used.
3. Always supply power to the Vcc_PLL1 and Vcc_PLL2, even if the PLL is not being used.
4. Drive ASEMD0 high when using the user system alone, and not using an emulator or the H-UDI. When this pin is low or open, RESETP may be masked.
5. Drivability can be switched by the register settings of the pin function controller (PFC). When 3.3 V is applied to VccQ1, set the drivability low. When 1.8 V is applied to VccQ1, set the drivability high.

<table>
<tr><th>Item</th><th>Page</th><th>Revision (See Manual for Details)</th></tr>
<tr><td>Section 11 Clock Pulse Generator (CPG)
11.4 Register Description
11.4.2 USBH/USBF Clock Control Register (UCLKCR)</td><td>447</td><td>Amended
…… is an 8-bit readable/writable register. UCLKCR is initialized to H′60 by a power-on reset. ……</td></tr>
<tr><td>Section 13 Power-Down Modes
13.8 Hardware Standby Mode
13.8.3 Hardware Standby Mode Timing</td><td>481</td><td>Added
……timings in hardware standby mode. Since the signal on the CA pin is sampled at the timing of EXTAL-RTC, clock should be input to the EXTAL-RTC pin when hardware standby mode is entered. In hardware standby mode, the CA pin……</td></tr>
<tr><td>Figure 13.12 Timing When Power of Pins other than VCC-RTC and VCCQ_RTC is Off</td><td>482</td><td>Added
Note * VCC, VCCQ, VccQ1, AVCC_USB, AVCC, VCC_PLL1, and VCC_PLL2</td></tr>
<tr><td>Section 15 16-Bit Timer Pulse Unit (TPU)
15.3 Register Description
15.3.3 Timer I/O Control Registers (TIOR)</td><td>506</td><td>Added
……Care is required since TIOR is affected by the TMDR setting.
If the counting operation is halted, the initial value set by this register is output from the TPU_TO pin.</td></tr>
<tr><td>Section 17 Realtime Clock (RTC)
17.2 Input/Output Pin
Table 17.1 Pin Configuration</td><td>541</td><td>Amended
<table>
<tr><th>Name</th><th>Abbreviation</th><th>Description</th></tr>
<tr><td>RTC external clock</td><td>EXTAL_RTC</td><td>Connects crystal resonator for RTC. Also used to input external clock for RTC.</td></tr>
<tr><td>RTC crystal</td><td>XTAL_RTC</td><td>Connects crystal resonator for RTC.</td></tr>
<tr><td>RTC power supply</td><td>V_{CC}_RTC</td><td>Power-supply pin for RTC (1.5 V)*</td></tr>
<tr><td>RTC GND</td><td>V_{SS}_RTC</td><td>GND pin for RTC *</td></tr>
<tr><td>RTC power supply</td><td>V_{CC}Q_RTC</td><td>Power-supply pin for RTC (3.3 V)*</td></tr>
</table>
Note: * Power-supply pins for RTC should be power supplied even when the RTC is not used.</td></tr>
</table>

<table>
<tr><th>Item</th><th>Page</th><th>Revision (See Manual for Details)</th></tr>
<tr><td>Section 20 I²C Bus Interface (IIC)
20.3 Register Description
20.3.3 I²C Bus Mode Register (ICMR)</td><td>629</td><td>Amended
<table>
<tr><th>Bit</th><th>Bit Name</th><th>Initial Value</th><th>R/W</th><th>Description</th></tr>
<tr><td>6</td><td>—</td><td>0</td><td>—</td><td>Reserved
This bit is always read as 0. The write value should always be 0.</td></tr>
</table></td></tr>
<tr><td>20.4 Operation
20.4.2 Master Transmit Operation
20.4.4 Slave Transmit Operation
20.4.5 Slave Receive Operation</td><td>640 to 647</td><td>WAIT deleted
1. Set the ICE bit in ICCR1 to 1. Also set up the MLS bit in ICMR and the CKS4 to CKS0 bits in ICCKS. (Initial setting)</td></tr>
<tr><td>20.7 Usage Notes</td><td>656</td><td>Added</td></tr>
<tr><td>Section 23 USB Pin Multiplex Controller
23.1 Features
Figure 23.1 Block Diagram of USB PIN Multiplexer</td><td>733</td><td>Amended

</td></tr>
<tr><td>23.2 Input/Output Pins
Table 23.4 Pin Configuration (Clock Signal)</td><td>735</td><td>Amended
<table>
<tr><th>Name</th><th>Pin Name</th><th>Description</th></tr>
<tr><td>USB external clock</td><td>EXTAL_USB</td><td>Connects a crystal resonator for USB. Also used to input an external clock for USB (48 MHz input).</td></tr>
<tr><td>USB crystal</td><td>XTAL_USB</td><td>Connects a crystal resonator for USB</td></tr>
</table></td></tr>
</table>

Item	Page	Revision (See Manual for Details)
23.3 Register Description 23.3.1 USB Transceiver Control Register (UTRCTL)	736	Amended

Bit	Bit Name	Initial Value	R/W	Description
15 to 9	—	All 0	R/W	Reserved These bits are always read as all 0s. The write values should always be all 0s.
7 to 2	—	All 0	R/W	Reserved These bits are always read as all 0s. The write values should always be all 0s.

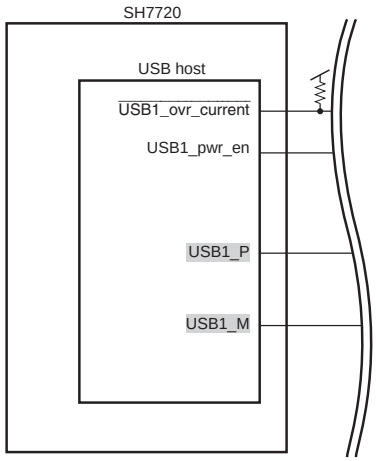
23.4 Examples of External Circuit 23.4.1 Example of the Connection between USB Function Controller and Transceiver Figure 23.2 Example 1 of Transceiver Connection for USB function Controller (On-Chip Transceiver is Used)	737	Amended 
23.4.2 Example of the Connection between USB Host Controller and Transceiver	739	Amended ……using the built-in transceiver 1. By using the USB2_ovr_current, USB2_pwr_en, USB2_P, and USB2_M pins in an external circuit similar to that in figure 23.4, you can……

Item | **Page** | **Revision (See Manual for Details)**

Figure 23.4 Example 1 of Transceiver Connection for USB Host Controller (On-Chip Transceiver is Used)

740

Amended



Section 24 USB Host Controller (USBH)

24.2 Input/Output Pins

Table 24.1 Pin Configuration

744

Amended

Pin name	Pin Name	Function
1P pin	USB1_P	D+ port 1 transceiver pin
1M pin	USB1_M	D– port 1 transceiver pin
2P pin	USB2_P	D+ port 2 transceiver pin
2M pin	USB2_M	D– port 2 transceiver pin

24.7 Usage Note

778

Added

Section 30 SIM Card Module (SIM)

30.3 Register Description

30.3.1 Serial Mode Register (SCSMR)

962

Amended

Bit	Bit Name	Initial Value	R/W	Description
5	—	1	R	Reserved This bit is always read as 1. The write value should always be 1.

Section 34 Pin Function Controller (PFC)

Table 34.1 Multiplex Pins

1143

Amended

Port	Port Function (Related Module)	Other Function (Related Module)
U	PTU1 input/output (port)	MMC_CMD input/output (MMC)/ SIOF1_RxD input (SIOF)/TPU_TI2B input (TPU)

<table>
<tr><th>Item</th><th>Page</th><th>Revision (See Manual for Details)</th></tr>
<tr><td>Section 35 I/O Ports
35.16 Port T
Figure 35.16 Port T</td><td>1205</td><td>Amended
PTT0 (input/output) / SCIF0_SCK (input/output)</td></tr>
<tr><td>35.17 Port U
Figure 35.17 Port U</td><td>1207</td><td>Amended
PTU2 (input/output) / MMC_DAT (input/output) / SIOF1_TxD (output) / TPU_TI3A (input)
PTU1 (input/output) / MMC_CMD (output) / SIOF1_RxD (input) / TPU_TI2B (input)
PTU0 (input/output) / MMC_CLK (output) / SIOF1_SCK (input/output) / TPU_TI2A (input)</td></tr>
<tr><td>35.17 Port V
Figure 35.18 Port V</td><td>1209</td><td>Amended
PTV0 (input/output) / SIM_CLK (output) / SCIF1_SCK (input/output)</td></tr>
<tr><td>Section 36 User Debugging Interface (H-UDI)
36.3 Register Description
36.3.3 Boundary Scan Register (SDBSR)
Table 36.3 Pins and Boundary Scan Register Bits</td><td>1219 to 1222</td><td>Amended
<table>
<tr><th>Bit</th><th>Pin Name</th><th>I/O</th></tr>
<tr><td>189</td><td>MMC_CMD/SIOF1_RxD/TPU_TI2B_PTU1</td><td>IN</td></tr>
<tr><td>176</td><td>USB1d_TXDPLS/AFE_SCLK/IOIS16/PCC_IOIS16/ PTG4</td><td>IN</td></tr>
<tr><td>154</td><td>SCIF0_TxD/PTT2</td><td>OUT</td></tr>
<tr><td>153</td><td>SCIF0_RTS/TPU_TO0/PTT3</td><td>OUT</td></tr>
<tr><td>152</td><td>SCIF0_CTS/TPU_TO1/PTT4</td><td>OUT</td></tr>
<tr><td>151</td><td>MMC_CLK/SIOF1_SCK/TPU_TI2A_PTU0</td><td>OUT</td></tr>
<tr><td>150</td><td>MMC_CMD/SIOF1_RxD/TPU_TI2B_PTU1</td><td>OUT</td></tr>
<tr><td>149</td><td>MMC_DAT/SIOF1_TxD/TPU_TI3A/PTU2</td><td>OUT</td></tr>
<tr><td>137</td><td>USB1d_TXDPLS/AFE_SCLK/IOIS16/PCC_IOIS16/ PTG4</td><td>OUT</td></tr>
<tr><td>112</td><td>MMC_CMD/SIOF1_RxD/TPU_TI2B/PTU1</td><td>Control</td></tr>
<tr><td>111</td><td>MMC_DAT/SIOF1_TxD/TPU_TI3A/PTU2</td><td>Control</td></tr>
<tr><td>99</td><td>USB1d_TXDPLS/AFE_SCLK/IOIS16/PCC_IOIS16/ PTG4</td><td>Control</td></tr>
</table></td></tr>
</table>

Item	Page	Revision (See Manual for Details)
Section 37 List of Registers 37.2 Register Bits	1269, 1279	Amended

Register Abbreviation	Bit 31/23/15/7	Bit 30/22/14/6	Bit 29/21/13/5	Module
ICMR	MLS	□	□	IIC
SCSMR	□	□	□	SIM

Section 38 Electrical Characteristics
38.3 DC Characteristics
Table 38.4 DC Characteristics (1) [Common]

1323, 1324

Amended

Item	Symbol		Test Conditions
Power supply voltage	V_{CC} V_{CC}_PLL1*1 V_{CC}_PLL2*1 V_{CC}_RTC*1		
Analog (A/D, D/A) power supply current	During A/D conversion	AI_{CC}	
	During A/D and D/A conversion		
	Idle		T_a = 25°C
Current consumption*3	Sleep mode	I_{CC}	When sleep mode is entered after a power-on reset: $V_{CC}Q$, $V_{CC}Q1$ = 3.3 V Bϕ = 33 MHz
		$I_{CC}Q$	

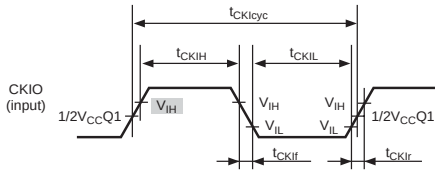
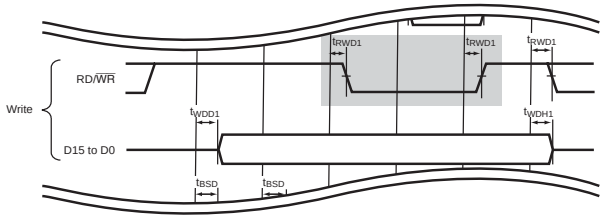
Notes: 1. When the PLL and RTC are not used, the V_{CC}_PLL1, V_{CC}_PLL2, V_{CC}_RTC, $V_{CC}Q$_RTC, V_{SS}_PLL1, V_{SS}_PLL2, and V_{SS}_RTC should be power supplied.

Item	Page	Revision (See Manual for Details)
Table 38.4 DC Characteristics (2-a) [Except USB Transceiver and I^2C Related Pins]	1325	Added

Item		Min.	Typ.	Max.	Unit	Test Conditions
Output high voltage	Group 2 output pins*	$V_{CC}Q1 \times 0.85$	—	—	V	$V_{CC}Q1$ = 1.65 to 1.95 V I_{OH} = –0.2 mA
		2.4	—	—	V	$V_{CC}Q1$ = 3.0 to 3.6 V I_{OH} = –0.2 mA
		2.2	—	—	V	$V_{CC}Q1$ = 2.7 to 3.6 V I_{OH} = –2 mA
	Other input pins	2.2	—	—	V	I_{OH} = –2mA

Table 38.4 DC Characteristics (2-b) [I^2C Related Pins*]	1326	Amended					
Item	**Symbol**	**Min.**	**Typ.**	**Max.**	**Unit**	**Test Conditions**	
Power supply voltage	VCCQ	2.7	3.3	3.6	V		
Input high voltage	VIH	VCCQ × 0.7	—	VCCQ + 0.3	V		
Input low voltage	VIL	–0.3	—	VCCQ × 0.3	V		
		Note: * The IIC_SCL and IIC_SDA pins (open-drain pins).					
38.4 AC Characteristics Table 38.6 Maximum Operating Frequencies	1328	Added Note: * When using the USB host controller, the external bus frequency (B□) should be set to 32 MHz or higher.					
38.4.1 Clock Timing Table 38.7 Clock Timing	1329	Amended					

Item	Symbol	Min.	Max.	Unit	Figure
CKIO clock output frequency	f_{OP}	20	66.67	MHz	38.2
CKIO clock input frequency	f_{CKI}	20	66.67	MHz	38.3

Item	Page	Revision (See Manual for Details)
Figure 38.3 CKIO Clock Input Timing	1330	Amended 
Table 38.8 Control Signal Timing	1333	Amended Notes: 1. RESETP, NMI, and IRQ5 to IRQ0 are asynchronous. Changes are detected at the clock rise when the setup time shown is used. If the setup time cannot be used, detection may be delayed until the next clock rises. 2. The upper limits of the external bus clock are 66.67 MHz (133 MHz version) and 80 MHz (160 MHz).
38.4.4 Basic Timing Figure 38.18 Bus Cycle of SRAM with Byte Selection (SW = 1 Cycle, HW = 1 Cycle, Asynchronous External Wait 1 Input, BAS = 1 (WE in Write Cycle Controlled))	1344	Amended 
38.4.8 Peripheral Module Signal Timing Table 38.10 Peripheral Module Signal Timing	1373	Added Conditions: $V_{CC}Q$ = 2.7 to 3.6 V, $V_{CC}Q1$ = 2.7 to 3.6 V or 1.65 to 1.95 V, V_{CC} = 1.4 to 1.6 V, AV_{CC} = 2.7 to 3.6 V, Ta = –20 to 75°C
38.4.12 I^2C Bus Interface Timing Table 38.14 I^2C Bus Interface Timing	1378	Amended **Item** / **Symbol** / **Test Conditions** SCL, SDA output fall time / t_{Sf} / VccQ=3.0 V
38.4.18 MMCIF Module Signal Timing Table 38.22 MMCIF Module Signal Timing	1389	Amended **Item** / **Symbol** / **Figure** MMC_CLK clock cycle / t_{MMCYC} / 38.69 to 38.70 MMC_CLK clock high level width / t_{MMWH} /

<table>
<tr><th>Item</th><th>Page</th><th>Revision (See Manual for Details)</th></tr>
<tr><td>Figure 38.71 MMCIF Receive Timing (Fall Sampling)</td><td>1390</td><td>Deleted</td></tr>
<tr><td>38.4.19 H-UDI Related Pin Timing
Table 38.23 H-UDI Related Pin Timing</td><td>1390</td><td>Amended
<table>
<tr><th>Item</th><th>Symbol</th><th>Min.</th><th>Max.</th><th>Unit</th><th>Figure</th></tr>
<tr><td>TCK cycle time</td><td>t_{TCKcyc}</td><td>50</td><td></td><td>ns</td><td>38.71</td></tr>
<tr><td>TRST setup time</td><td>t_{TRSTS}</td><td>12</td><td></td><td>ns</td><td>38.72</td></tr>
<tr><td>TDI setup time</td><td>t_{TDIS}</td><td>10</td><td></td><td>ns</td><td>38.73</td></tr>
<tr><td>ASEMD0 setup time</td><td>$t_{ASEMD0S}$</td><td>12</td><td></td><td>ns</td><td>38.74</td></tr>
</table></td></tr>
<tr><td>Figure 38.71 TCK Input Timing
Figure 38.72 TRST Input Timing (Reset Hold)
Figure 38.73 H-UDI Data Transfer Timing
Figure 38.74 ASEMD0 Input Timing
Figure 38.75 Output Load Circuit</td><td>1391s</td><td>Figure numbers amended</td></tr>
</table>

Item: Appendix A. Pin States — Table A.1 SH7720 Pin States

Page: 1395 to 1406

Revision (See Manual for Details): Headings of pin number columns amended

BP-256H → PLBG0256GA-A

BP-256C → PLBG0256KA-A

Page: 1397, 1406

Amended and deleted

Category								
PLBG0256GA-A	PLBG0256KA-A	Pin Name	Manual Reset	Software Standby	Hardware Standby	Bus Release	I/O	Handling of Unused Pins
C18	E18	USB1d_TXDPLS/ AFE_SCLK/ IOIS16/ PCC_IOIS16/ PTG4	O/I/I/I/P	O/Z/Z/Z/K	Z/Z/Z/Z/Z	O/I/I/I/P	O/I/I/I/IO	Pull-up
C20	E21	EXTAL_USB	I	I	I	I	I	Pull-up

Notes: * The conditions for setting USB_1P and USB_M to Z (open) are as follows:
(1) Pull the USB1_ovr_current/USBF_VBUS pin down.
(2) Clear the USB_TRANS bit in UTRCTR to 0 (initial value).
Set the USB_SEL bit in UTRCTR to 1 (initial value).

1. Handlings of unused pins in this table are handling examples with the pin functions set to the initial values of the pin function controller (PFC) and cannot be guaranteed in some cases.
2. Controlled by software when an input buffer (PAD) is not enabled.
3. Normal input pin specification.
4. A schmitt characteristic is provided.
5. A board with which the emulator can be used must be designed according to the emulator specifications.

Item: B. Product Lineup

Page: 1407

Amended

Operating Frequency	Product Code	Package
133.34 MHz	HD6417720BP133C	256-pin CSP (PLBG0256GA-A (BP-256H))
	HD6417720BP133CV	256-pin CSP (PLBG0256GA-A (BP-256HV))
	HD6417720BL133C	256-pin CSP (PLBG0256KA-A (BP-256C))
	HD6417720BL133CV	256-pin CSP (PLBG0256KA-A (BP-256CV))

Item	Page	Revision (See Manual for Details)
C. Package Dimensions Figure C.1 Package Dimensions (PLBG0256GA-A (BP-256H/HV)) Figure C.2 Package Dimensions (PLBG0256KA-A (BP-256C/CV))	1408, 1409	Figures replaced