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April 1st, 2010
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HITACHI MICROCOMPUTER TECHNICAL UPDATE

DATE	12 April 2001	No.	TN-SH7-314A/E
THEME	SH7615 limitation on use of internal direct memory access controller.		
CLASSIFICATION	☐ Spec change ■ Limitation on Use ☐ Supplement of Documents		
PRODUCT NAME	HD6417615ARF	Lot No.etc.	ALL
REFERENCE DOCUMENTS	SH7615 Hardware manual	Effective Date	Permanent

There are two limitations on use of internal Direct Memory Access Controller(DMAC) in SH7615, and their countermeasures are shown below.

<Phenomenon>

1. Data bus collision during a DMA transfer in single address mode

In the system which has SH7615, external devices with DACK and Synchronous DRAM(SDRAM), after SH7615 writes data to SDRAM, there is a case that SH7615 drives data bus wrong without regard to DMA transfer in single address mode from the external device with DACK to SDRAM, and the wrongly driven data collides with the DMA transfer data.

2. DACK Error

On the condition that both channels select external DMA request signals DREQ0/1 for DMA requests, there is a case that DMAC executes DMA channel1 transfer wrong with DACK1 output without regard to DREQ1 inactive.

<Condition>

1. Condition of data bus collision during a DMA transfer in single address mode

When all following conditions are met, the data bus collision occurs on transferring data from the external device with DACK to SDRAM in single address mode.

(1)External clock(Eø) freq. : Internal clock(Iø) freq.=1:1

(2)SDRAM single write mode

(3)Right after SH7615 writes data to SDRAM, DMAC transfers data from the external device with DACK to SDRAM in single address mode.

2. Condition of DACK Error

When all following conditions are met, DMAC executes DMA channel1 transfer with DACK1 output without regard to DREQ1 inactive.

(1)DMAC channel0/1 are enabled.

(2)Both channel0/1 select the external DMA request signals(DREQ0/1) for DMA request sources.

(3)Both channel0/1 is set to Cycle-steal mode.

(4)Round-robin mode is set as priority mode.

<Countermeasures>

1. Countermeasure to data bus collision during a DMA transfer in single address mode

This problem is avoided by any of the following countermeasures.

(1)Use frequency mode except External clock(Eø) freq. : Internal clock(Iø) freq.=1:1

(2)Not execute SDRAM write access from CPU, E-DMAC, or another channel of DMAC, while DMAC transfers data from the external device with DACK to SDRAM in single address mode.

2. Countermeasure to DACK Error

This problem is avoided by any of the following countermeasures.

(1)Set either channel of DMAC to burst mode.

(2)Set to Fixed priority mode.