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RENESAS TECHNICAL UPDATE

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Renesas Technology Corp.

Product Category	MPU&MCU		Document No.	TN-SH7-A643A/E	Rev.	1.00
Title	SH7211 Group: Error correction in the hardware manuals		Information Category	Technical Notification		
Applicable Product	SH7211 Group	Lot No. All	Reference Document	SH7211 Group Hardware Manual Rev. 1.00 (REJ09B0344-0100)		

Thank you for your consistent patronage of Renesas semiconductor products.

We would like to inform you of error corrections in the description of the SH7211 Group Hardware Manual. Please take this information into consideration when using these products.

<Error Corrections>

Section 1. Overviews

Pages 5 and 6, Table 1 SH7211 Features are revised as follows.

[Before change]

Items	Specification
Multi-function timer pulse unit 2 (MTU2)	• Pulse output modes One shot, toggle, PWM, complementary PWM, and reset-synchronized PWM modes
User break controller (UBC)	• Two break channels • Addresses, data values, type of access, and data size can all be set as break conditions
Advanced user debugger II (AUD-II)	• Six input/output pins

[After change]

Items	Specification
Multi-function timer pulse unit 2 (MTU2)	• Pulse output modes Toggle, PWM, complementary PWM, and reset-synchronized PWM modes
User break controller (UBC)	• Four break channels • Addresses, type of access, and data size can all be set as break conditions
Advanced user debugger II (AUD-II)	• Six output pins

Page 9, Table 1.2 Pin Functions

[Before change]

Classification	Symbol	I/O	Name	Function
Clock	CK	I/O	System clock	Inputs an external clock or supplies the system clock to external devices.

[After change]

Classification	Symbol	I/O	Name	Function
Clock	CK	O	System clock	Supplies the system clock to external devices.

Section 3. MCU Operating Modes

Page 55, Table 3.1 Selection of Operating Modes

[Before change]

	Pin Setting					Bus Width of CS0 Space
Mode No.	FWE	MD1	MD0	Mode Name	On-Chip ROM	SH7211F
Mode 6*	1	1	0	User programming mode	Active	Set by CS0BCR in BSC
Mode 7*	1	1	1			—

[After change]

	Pin Setting					Bus Width of CS0 Space
Mode No.	FWE	MD1	MD0	Mode Name	On-Chip ROM	SH7211F
Mode 6*	1	1	0	User program mode	Active	Set by CS0BCR in BSC

Section 4. Clock Pulse Generator (CPG)

Page 61, 4.1 Features

[Before change]

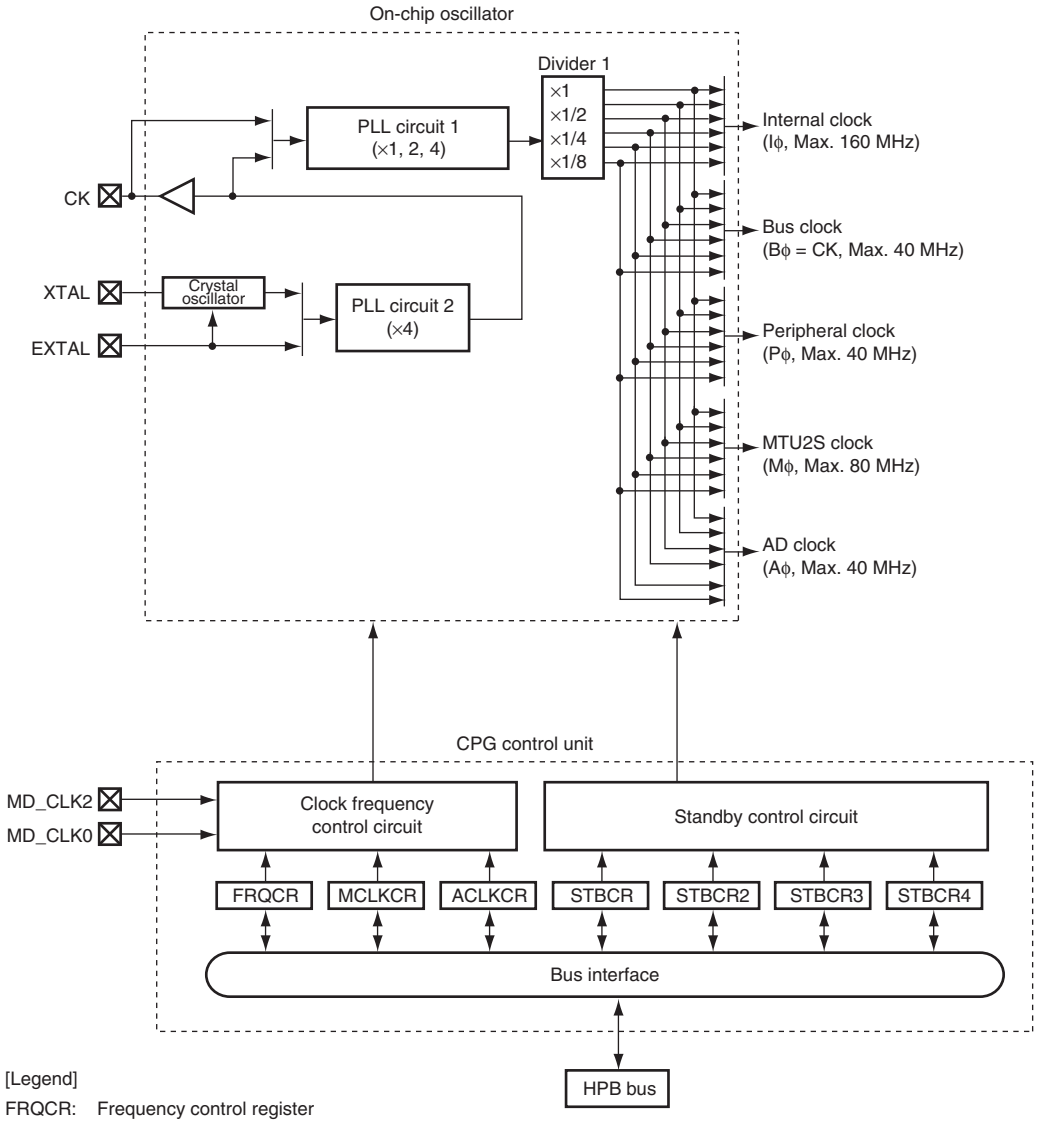
- Two clock operating modes
  The mode is selected from among the one clock operating mode by the selection of the following three conditions: the frequency-divisor in use, whether the PLLs are on or off, and whether the internal crystal resonator or the input on the external clock-signal line is used.

[After change]

- Clock operating modes
  Either the internal crystal resonator or the input on the external clock-signal line can be selected.

Page 62, Figure 4-1 Block Diagram of Clock Pulse Generator

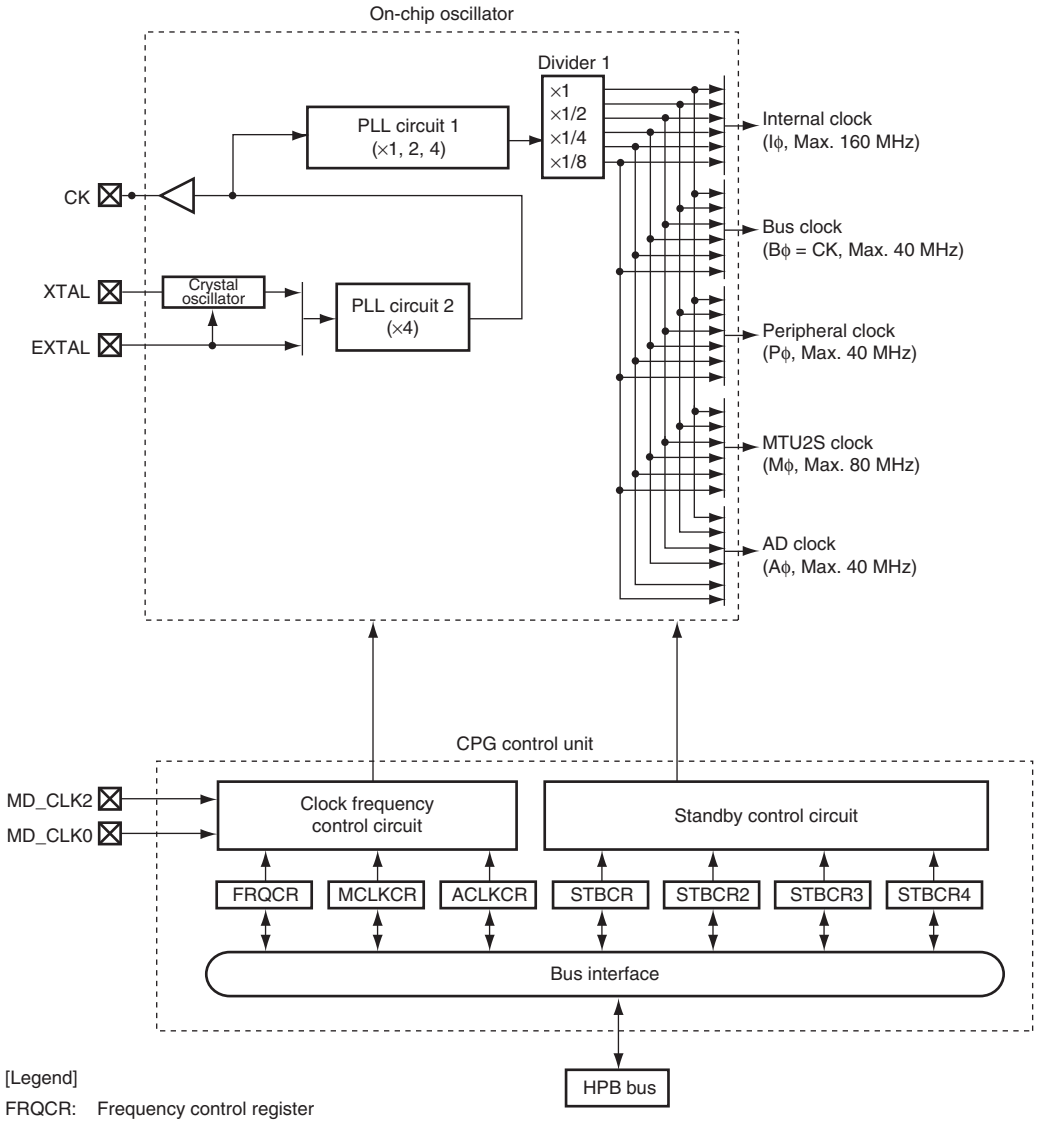
[Before change]



[Legend]

FRQCR: Frequency control register
MCLKCR: MTU2S clock frequency control register
ACLKCR: AD clock frequency control register
STBCR: Standby control register
STBCR2: Standby control register 2
STBCR3: Standby control register 3
STBCR4: Standby control register 4

[After change]



[Legend]

FRQCR: Frequency control register
MCLKCR: MTU2S clock frequency control register
ACLKCR: AD clock frequency control register
STBCR: Standby control register
STBCR2: Standby control register 2
STBCR3: Standby control register 3
STBCR4: Standby control register 4

Page 65, Table 4.1 Pin Configuration and Functions of the Clock Pulse Generator

[Before change]

Pin Name	Symbol	I/O	Function (Clock Operating Mode 6)
Clock input/output pin	CK	I/O	Clock output pin. This pin can be high impedance.

[After change]

Pin Name	Symbol	I/O	Function (Clock Operating Mode 6)
Clock output pin	CK	Output	Clock output pin. This pin can be high impedance.

Page 70, 4.4.1 Frequency Control Register (FRQCR)

[Before change]

Bit	Bit Name	Initial Value	R/W	Description
6 to 4	IFC[2:0]	000	R/W	Internal Clock (Iϕ) Frequency Division Ratio These bits specify the frequency division ratio of the internal clock with respect to the output frequency of PLL circuit 1. 000: × 1 time 001: × 1/2 time 010: Setting prohibited 011: × 1/4 time 100: Setting prohibited 101: × 1/8 time
2 to 0	PFC[2:0]	011	R/W	Peripheral Clock (Pϕ) Frequency Division Ratio These bits specify the frequency division ratio of the peripheral clock with respect to the output frequency of PLL circuit 1. 000: × 1 time 001: × 1/2 time 010: Setting prohibited 011: × 1/4 time 100: Setting prohibited 101: × 1/8 time

[After change]

Bit	Bit Name	Initial Value	R/W	Description
6 to 4	IFC[2:0]	000	R/W	Internal Clock (Iϕ) Frequency Division Ratio These bits specify the frequency division ratio of the internal clock with respect to the output frequency of PLL circuit 1. If a prohibited value is specified, correct operation cannot be guaranteed. 000: × 1 time 001: × 1/2 time 011: × 1/4 time Other than above: Setting prohibited
2 to 0	PFC[2:0]	011	R/W	Peripheral Clock (Pϕ) Frequency Division Ratio These bits specify the frequency division ratio of the peripheral clock with respect to the output frequency of PLL circuit 1. If a prohibited value is specified, correct operation cannot be guaranteed. 000: × 1 time 001: × 1/2 time 011: × 1/4 time 101: × 1/8 time Other than above: Setting prohibited

Page 73, 4.5.1 Changing the Multiplication Rate

[Before change]

For details, see table 23.3 in section 23, Power-Down Modes.

[After change]

For details, see table 23.4 in section 23, Power-Down Modes.

Section 5. Exception Handling

Page 87, 5.3.1 Address Error Sources, Table 5.6 Bus Cycle and Address Errors

[Before change]

Bus Cycle			
Type	**Bus Master**	**Bus Cycle Description**	**Address Errors**
Instruction fetch	CPU	Instruction fetched from even address	None (normal)
		Instruction fetched from odd address	Address error occurs
		Instruction fetched from other than on-chip peripheral module space* or H'F0000000 to H'F5FFFFFF in on-chip RAM space*	None (normal)
		Instruction fetched from on-chip peripheral module space* or H'F0000000 to H'F5FFFFFF in on-chip RAM space*	Address error occurs
Data read/write	CPU or DMAC	Word data accessed from even address	None (normal)
		Word data accessed from odd address	Address error occurs
		Longword data accessed from a longword boundary	None (normal)
		Longword data accessed from other than a long-word boundary	Address error occurs
		Byte or word data accessed in on-chip peripheral module space*	None (normal)
		Longword data accessed in 16-bit on-chip peripheral module space*	None (normal)
		Longword data accessed in 8-bit on-chip peripheral module space*	None (normal)

[After change]

Bus Cycle			
Type	**Bus Master**	**Bus Cycle Description**	**Address Errors**
Instruction fetch	CPU	Instruction fetched from even address	None (normal)
		Instruction fetched from odd address	Address error occurs
		Instruction fetched from other than on-chip peripheral module space* or H'F0000000 to H'F5FFFFFF in on-chip RAM space*	None (normal)
		Instruction fetched from on-chip peripheral module space* or H'F0000000 to H'F5FFFFFF in on-chip RAM space*	Address error occurs
		Instruction fetched from external memory space in single-chip mode	Address error occurs
Data read/write	CPU or DMAC	Word data accessed from even address	None (normal)
		Word data accessed from odd address	Address error occurs
		Longword data accessed from a longword boundary	None (normal)
		Longword data accessed from other than a long-word boundary	Address error occurs
		Byte or word data accessed in on-chip peripheral module space*	None (normal)
		Longword data accessed in 16-bit on-chip peripheral module space*	None (normal)
		Longword data accessed in 8-bit on-chip peripheral module space*	None (normal)
		Instruction fetched from external memory space in single-chip mode	Address error occurs

Page 88, 5.3.2 Address Error Exception Handling

[Before change]

5.3.2 Address Error Exception Handling

When an address error occurs, the bus cycle in which the address error occurred ends. When the executing instruction then finishes, address error exception handling starts. The CPU operates as follows:

1. The exception service routine start address which corresponds to the address error that occurred is fetched from the exception handling vector table.
2. The status register (SR) is saved to the stack.
3. The program counter (PC) is saved to the stack. The PC value saved is the start address of the instruction to be executed after the last executed instruction.
4. After jumping to the address fetched from the exception handling vector table, program execution starts. The jump that occurs is not a delayed branch.

[After change]

5.3.2 Address Error Exception Handling

When an address error occurs, the bus cycle in which the address error occurred ends*. When the executing instruction then finishes, address error exception handling starts. The CPU operates as follows:

1. The exception service routine start address which corresponds to the address error that occurred is fetched from the exception handling vector table.
2. The status register (SR) is saved to the stack.
3. The program counter (PC) is saved to the stack. The PC value saved is the start address of the instruction to be executed after the last executed instruction.
4. After jumping to the address fetched from the exception handling vector table, program execution starts. The jump that occurs is not a delayed branch.

Note: * This is the case in which an address error was caused by data read or write. When an address error is caused by an instruction fetch, and if the bus cycle in which the address error occurred does not end by step 3 above, the CPU restarts the address error exception handling until the bus cycle ends.

Section 6. Interrupt Controller (INTC)

Page 119, Table 6.4 Interrupt Exception Handling Vectors and Priorities

[Before change]

Interrupt Source Number			Interrupt Vector: Vector	Interrupt Vector: Vector Table Address Offset	Interrupt Priority (Initial Value)	Corresponding IPR (Bit)	IPR Setting Unit Internal Priority	Default Priority
DMAC	DMAC0	TEI0	108	H'000001B0 to H'000001B3	0 to 15 (0)	IPR06 (15 to 12)	1	High
		HEI0	109	H'000001B4 to H'000001B7			2	
	DMAC1	TEI1	112	H'000001C0 to H'000001C3	0 to 15 (0)	IPR06 (11 to 8)	1	
		HEI1	113	H'000001C4 to H'000001C7			2	
	DMAC2	TEI2	116	H'000001D0 to H'000001D3	0 to 15 (0)	IPR06 (7 to 4)	1	
		HEI2	117	H'000001D4 to H'000001D7			2	
	DMAC3	TEI3	120	H'000001E0 to H'000001E3	0 to 15 (0)	IPR06 (3 to 0)	1	
		HEI3	121	H'000001E4 to H'000001E7			2	
	DMAC4	TEI4	124	H'000001F0 to H'000001F3	0 to 15 (0)	IPR07 (15 to 12)	1	
		HEI4	125	H'000001F4 to H'000001F7			2	
	DMAC5	TEI5	128	H'00000200 to H'00000203	0 to 15 (0)	IPR07 (11 to 8)	1	
		HEI5	129	H'00000204 to H'00000207			2	
	DMAC6	TEI6	132	H'00000210 to H'00000213	0 to 15 (0)	IPR07 (7 to 4)	1	
		HEI6	133	H'00000214 to H'00000217			2	
	DMAC7	TEI7	136	H'00000220 to H'00000223	0 to 15 (0)	IPR07 (3 to 0)	1	
		HEI7	137	H'00000224 to H'00000227			2	Low

[After change]

Interrupt Source Number			Interrupt Vector: Vector	Interrupt Vector: Vector Table Address Offset	Interrupt Priority (Initial Value)	Corresponding IPR (Bit)	IPR Setting Unit Internal Priority	Default Priority
DMAC	DMAC0	DEI0	108	H'000001B0 to H'000001B3	0 to 15 (0)	IPR06 (15 to 12)	1	High
		HEI0	109	H'000001B4 to H'000001B7			2	
	DMAC1	DEI1	112	H'000001C0 to H'000001C3	0 to 15 (0)	IPR06 (11 to 8)	1	
		HEI1	113	H'000001C4 to H'000001C7			2	
	DMAC2	DEI2	116	H'000001D0 to H'000001D3	0 to 15 (0)	IPR06 (7 to 4)	1	
		HEI2	117	H'000001D4 to H'000001D7			2	
	DMAC3	DEI3	120	H'000001E0 to H'000001E3	0 to 15 (0)	IPR06 (3 to 0)	1	
		HEI3	121	H'000001E4 to H'000001E7			2	
	DMAC4	DEI4	124	H'000001F0 to H'000001F3	0 to 15 (0)	IPR07 (15 to 12)	1	
		HEI4	125	H'000001F4 to H'000001F7			2	
	DMAC5	DEI5	128	H'00000200 to H'00000203	0 to 15 (0)	IPR07 (11 to 8)	1	
		HEI5	129	H'00000204 to H'00000207			2	
	DMAC6	DEI6	132	H'00000210 to H'00000213	0 to 15 (0)	IPR07 (7 to 4)	1	
		HEI6	133	H'00000214 to H'00000217			2	
	DMAC7	DEI7	136	H'00000220 to H'00000223	0 to 15 (0)	IPR07 (3 to 0)	1	
		HEI7	137	H'00000224 to H'00000227			2	Low

Section 8. Bus State Controller (BSC)

Page 177, Figure 8.1 Block Diagram of BSC

[Before change]

CSnWCR: CSn Space Wait Control Register (n = 0 to 8)

CSnBCR: CSn Space Bus Control Register (n = 0 to 8)

[After change]

CSnWCR: CSn space wait control register (n = 0 to 7)

CSnBCR: CSn space bus control register (n = 0 to 7)

Page 181, 8.3.2 Setting Operating Modes

- Initial Settings of Endianness

[Before change]

When an instruction code of the CPU of SH2A is accessed in little-endian order, both longword fetch and word fetch are performed and even byte reading may be performed in some cases. Therefore, select 8-bit bus width for the external memory. For higher access performance, it is recommended that instruction fetches from the external memory be performed in big-endian order.

[After change]

Little endian cannot be selected in area 0. Since both 32-bit and 16-bit accesses are included in instruction fetches, no instructions can be assigned in little endian area. Accordingly, instructions should be executed in big endian area.

Section 10. Multifunction Timer Pulse Unit 2 (MTU2)

Page 353, Table 10.1 MTU2 Functions

[Before change]

Item	Channel 0	Channel 1	Channel 2	Channel 3	Channel 4	Channel 5
DMAC activation	TGR compare match or input capture	TGR compare match or input capture	TGR compare match or input capture	TGR compare match or input capture	TGR compare match or input capture and TCNT overflow or underflow	TGR compare match or input capture

[After change]

Item	Channel 0	Channel 1	Channel 2	Channel 3	Channel 4	Channel 5
DMAC activation	TGR compare match or input capture	TGR compare match or input capture	TGR compare match or input capture	TGR compare match or input capture	TGR compare match or input capture	—

Page 387, Table 10.28 TIORU_5, TIORV_5, and TIORW_5 (Channel 5)

[Before change]

					Description	
Bit 4 IOC4	Bit 3 IOC3	Bit 2 IOC2	Bit 1 IOC1	Bit 0 IOC0	TGRU_5, TGRV_5, and TGRW_5 Function	TIC5U, TIC5V, and TIC5W Pin Function
1	1	0	0	1	Input capture register	Measurement of low pulse width of external input signal Capture at trough
1	1	0	1	0		Measurement of low pulse width of external input signal Capture at crest
1	1	0	1	1		Measurement of low pulse width of external input signal Capture at crest and trough
1	1	1	0	1		Measurement of high pulse width of external input signal Capture at trough
1	1	1	1	0		Measurement of high pulse width of external input signal Capture at crest
1	1	1	1	1		Measurement of high pulse width of external input signal Capture at crest and trough

[After change]

					Description	
Bit 4 IOC4	Bit 3 IOC3	Bit 2 IOC2	Bit 1 IOC1	Bit 0 IOC0	TGRU_5, TGRV_5, and TGRW_5 Function	TIC5U, TIC5V, and TIC5W Pin Function
1	1	0	0	1	Input capture register	Measurement of low pulse width of external input signal Capture at trough in complementary PWM mode
1	1	0	1	0		Measurement of low pulse width of external input signal Capture at crest in complementary PWM mode
1	1	0	1	1		Measurement of low pulse width of external input signal Capture at crest and trough in complementary PWM mode
1	1	1	0	1		Measurement of high pulse width of external input signal Capture at trough in complementary PWM mode
1	1	1	1	0		Measurement of high pulse width of external input signal Capture at crest in complementary PWM mode
1	1	1	1	1		Measurement of high pulse width of external input signal Capture at crest and trough in complementary PWM mode

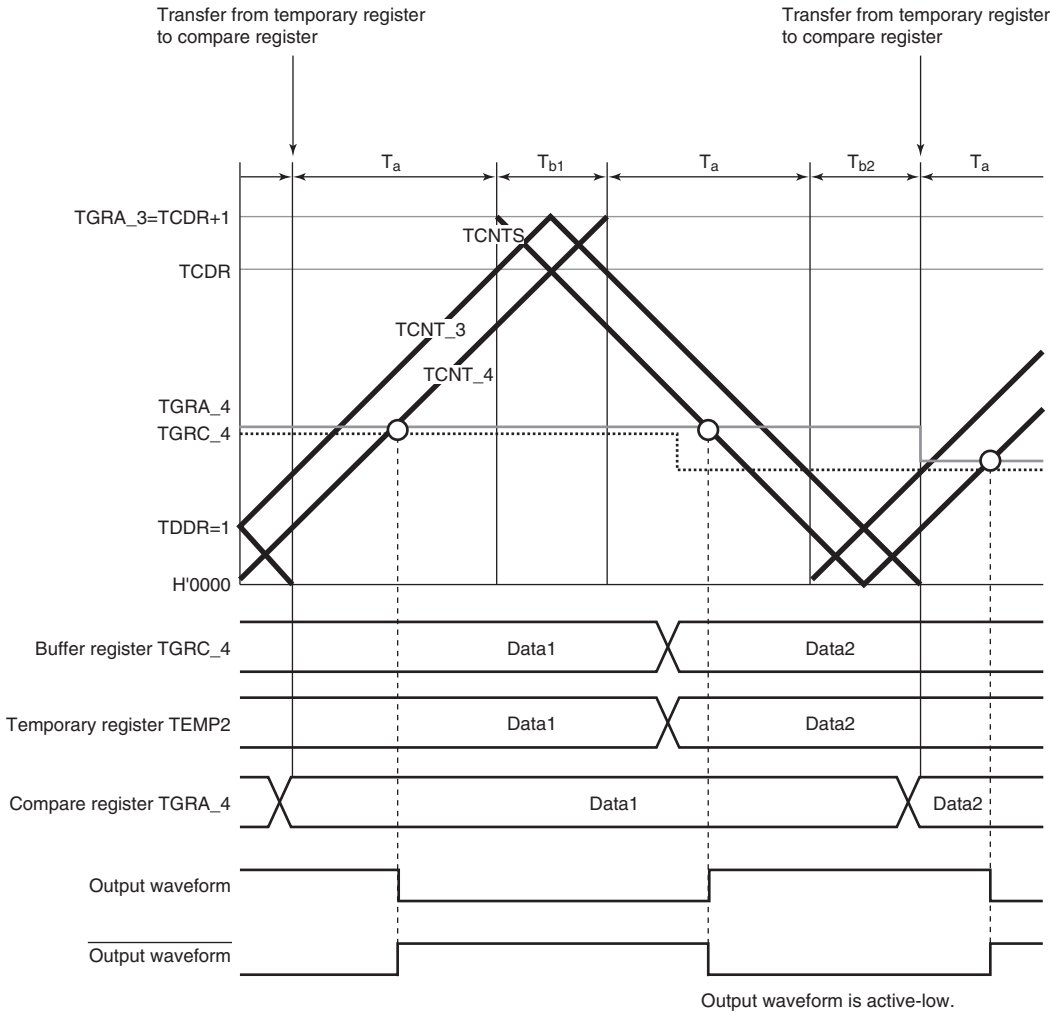
Page 428, 10.3.23 Timer Gate Control Register (TGCR)

[Addition]

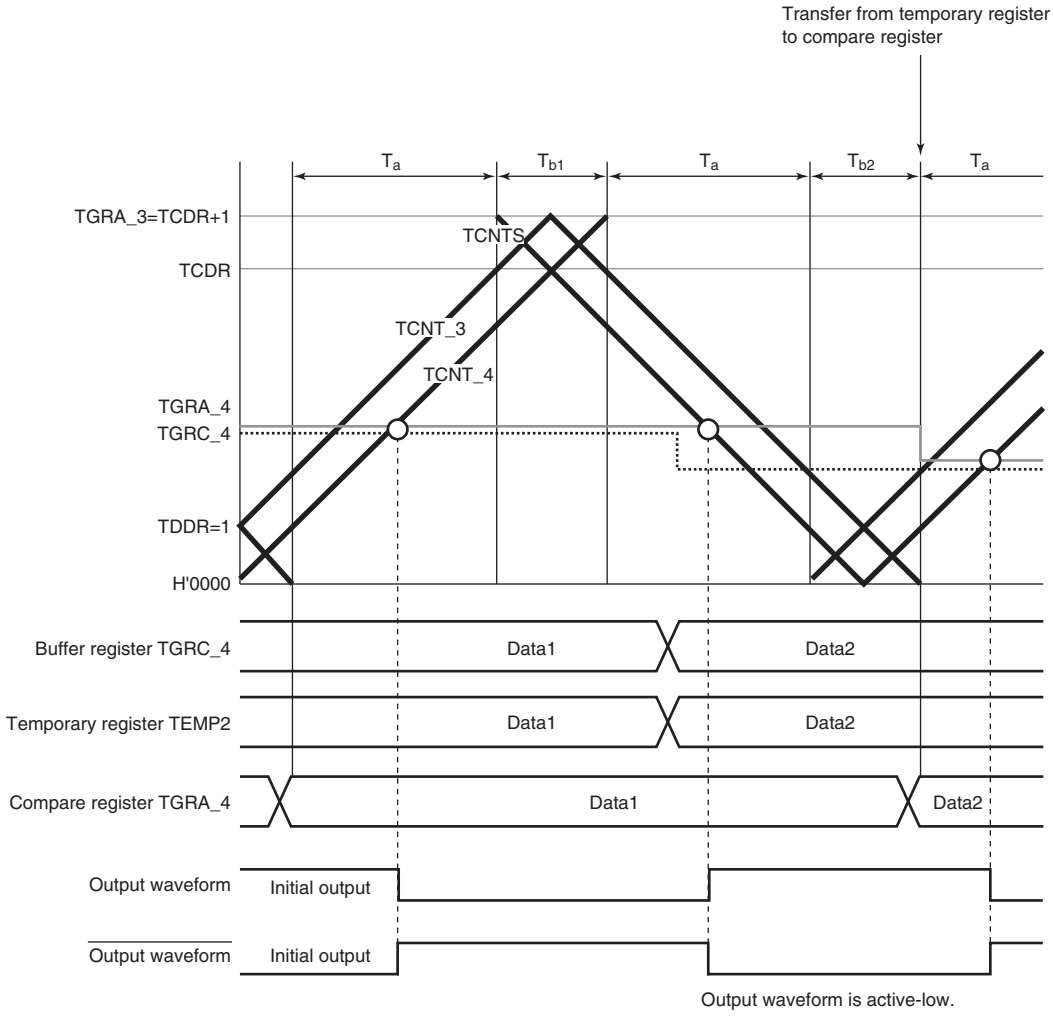
Note: If the BDC bit in the MTU2S is set to 1, the FB bit should not be cleared to 0.

Page 482, Figure 10.41 Example of Operation without Dead Time

[Before Change]



[After Change]



Page 513, (c) Buffer Transfer Control Linked with Interrupt Skipping

[Before Change]

(c) Buffer Transfer Control Linked with Interrupt Skipping

In complementary PWM mode, whether to transfer data from a buffer register to a temporary register and whether to link the transfer with interrupt skipping can be specified with the BTE1 and BTE0 bits in the timer buffer transfer set register (TBTER).

Figure 10.76 shows an example of operation when buffer transfer is suppressed (BTE1 = 0 and BTE0 = 1). While this setting is valid, data is not transferred from the buffer register to the temporary register.

Figure 10.77 shows an example of operation when buffer transfer is linked with interrupt skipping (BTE1 = 1 and BET0 = 0). While this setting is valid, data is not transferred from the buffer register outside the buffer transfer-enabled period.

Note that the buffer transfer-enabled period depends on the T3AEN and T4VEN bit settings in the timer interrupt skipping set register (TITCR). Figure 10.78 shows the relationship between the T3AEN and T4VEN bit settings in TITCR and buffer transfer-enabled period.

[After Change]

(c) Buffer Transfer Control Linked with Interrupt Skipping

In complementary PWM mode, whether to transfer data from a buffer register to a temporary register and whether to link the transfer with interrupt skipping can be specified with the BTE1 and BTE0 bits in the timer buffer transfer set register (TBTER).

Figure 10.76 shows an example of operation when buffer transfer is suppressed (BTE1 = 0 and BTE0 = 1). While this setting is valid, data is not transferred from the buffer register to the temporary register.

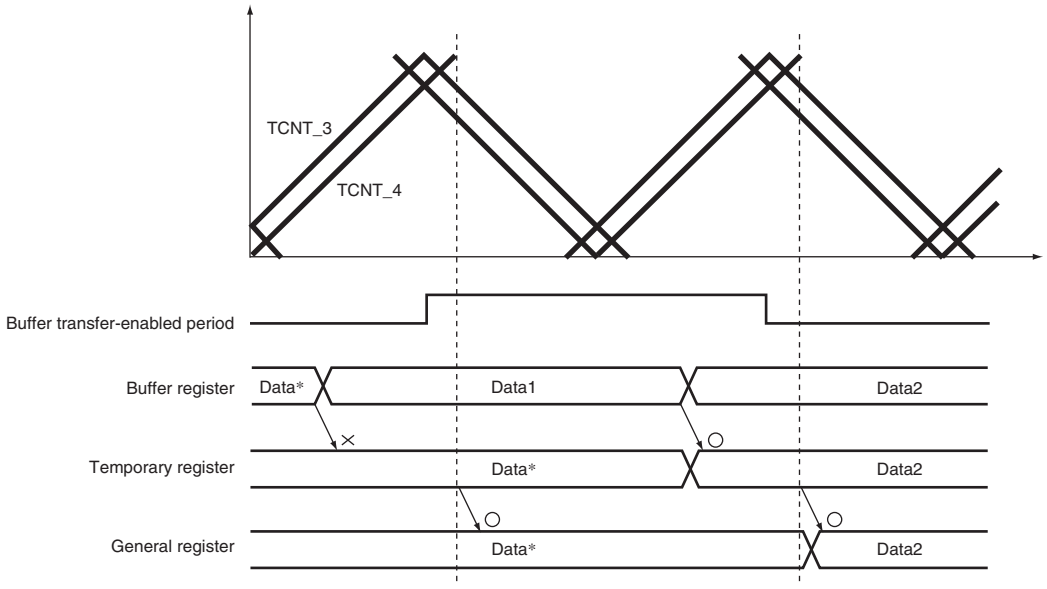
Figure 10.77 shows an example of operation when buffer transfer is linked with interrupt skipping (BTE1 = 1 and BET0 = 0). While this setting is valid, data is not transferred from the buffer register outside the buffer transfer-enabled period.

There are two types of timing in which data is transferred from the buffer register to the temporary register or to general register, depending on the buffer register modification timing after an interrupt occurrence.

Note that the buffer transfer-enabled period depends on the T3AEN and T4VEN bit settings in the timer interrupt skipping set register (TITCR). Figure 10.78 shows the relationship between the T3AEN and T4VEN bit settings in TITCR and buffer transfer-enabled period.

Page 515, Figure 10.77 Example of Operation when Buffer Transfer is Linked with Interrupt Skipping (BTE1 = 1 and BTE0 = 0)

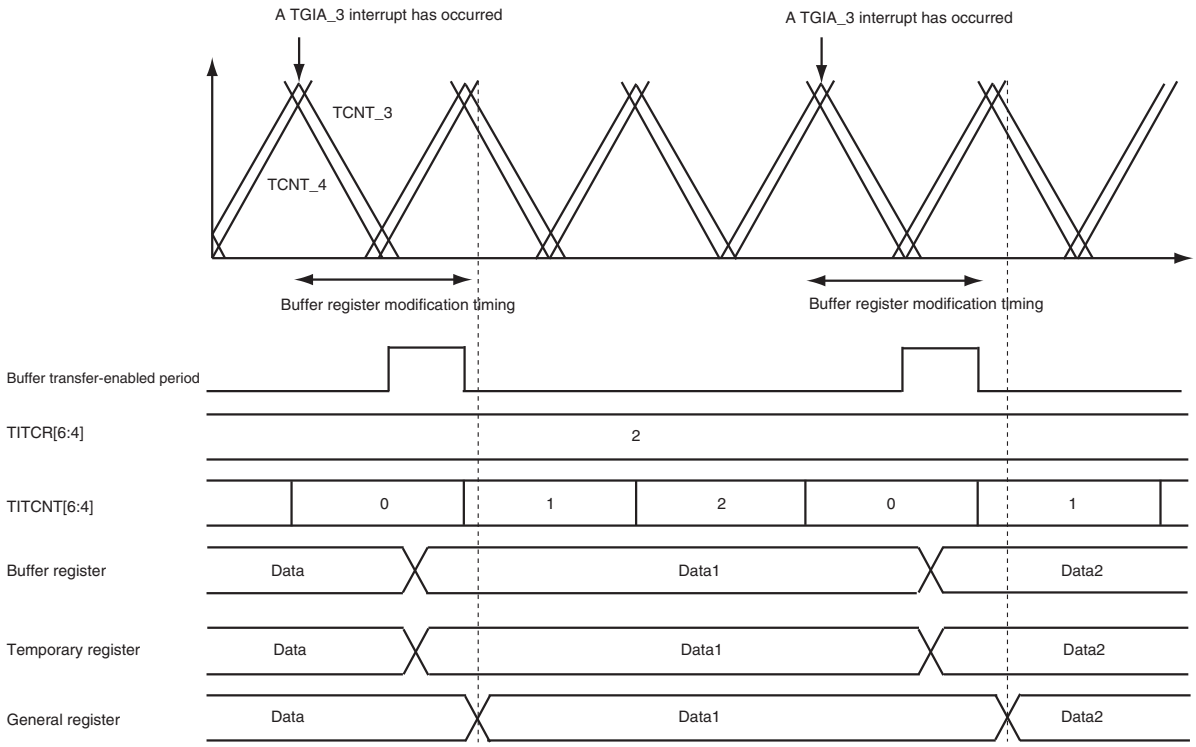
[Before Change]



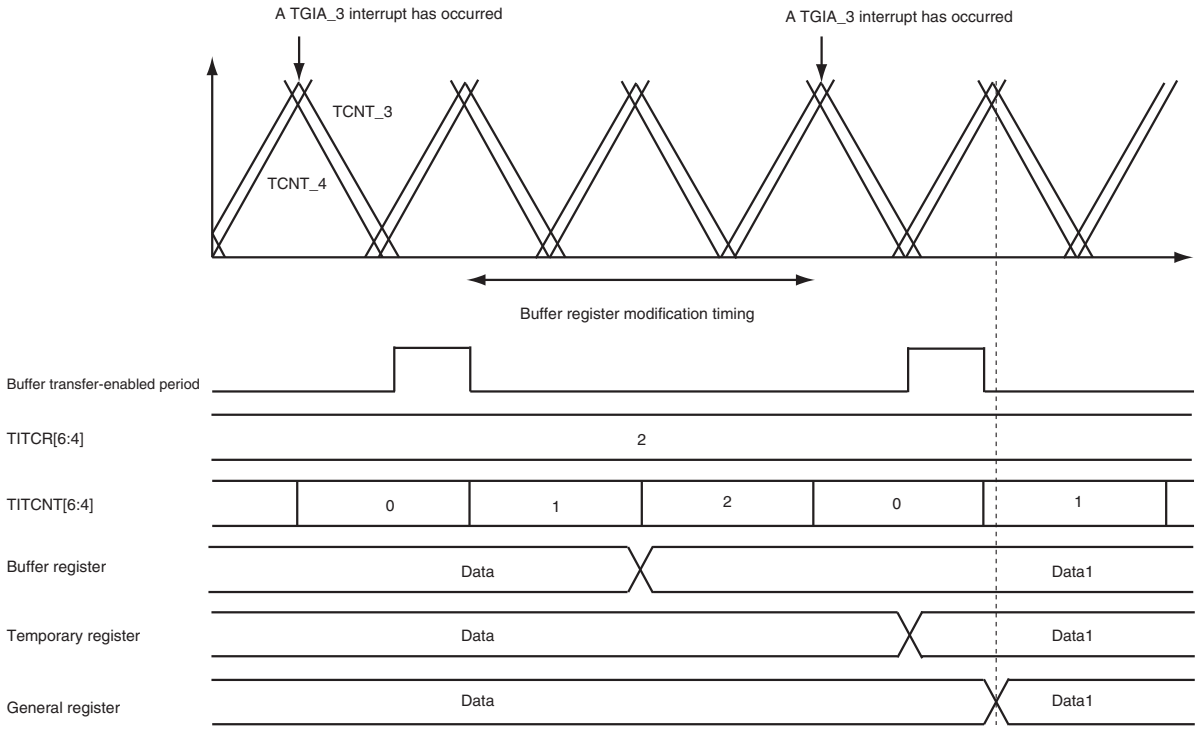
Note: * Buffer transfer at the crest is selected.
The skipping count is set to three.
T3AEN is set to 1.

[After Change]

(1) When the buffer register is modified within one carrier cycle after a TGIA_3 interrupt has occurred



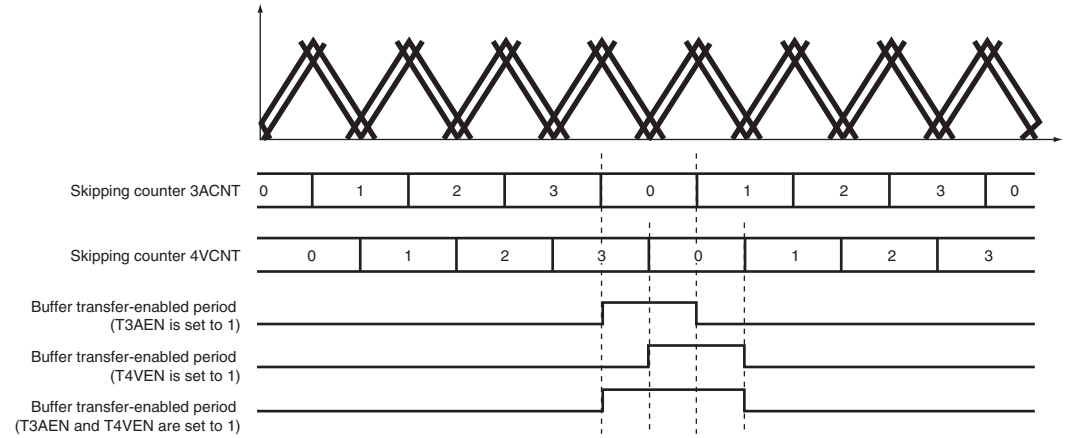
(2) When the buffer register is modified after one carrier cycle has been passed from a TGIA_3 interrupt occurrence



Note: MD[3:0] in TMDR_3 = 1101
Buffer transfer at the crest is selected.
The skipping count is set to two.
T3AEN and T4VEN are set to 1 and cleared to 0, respectively.

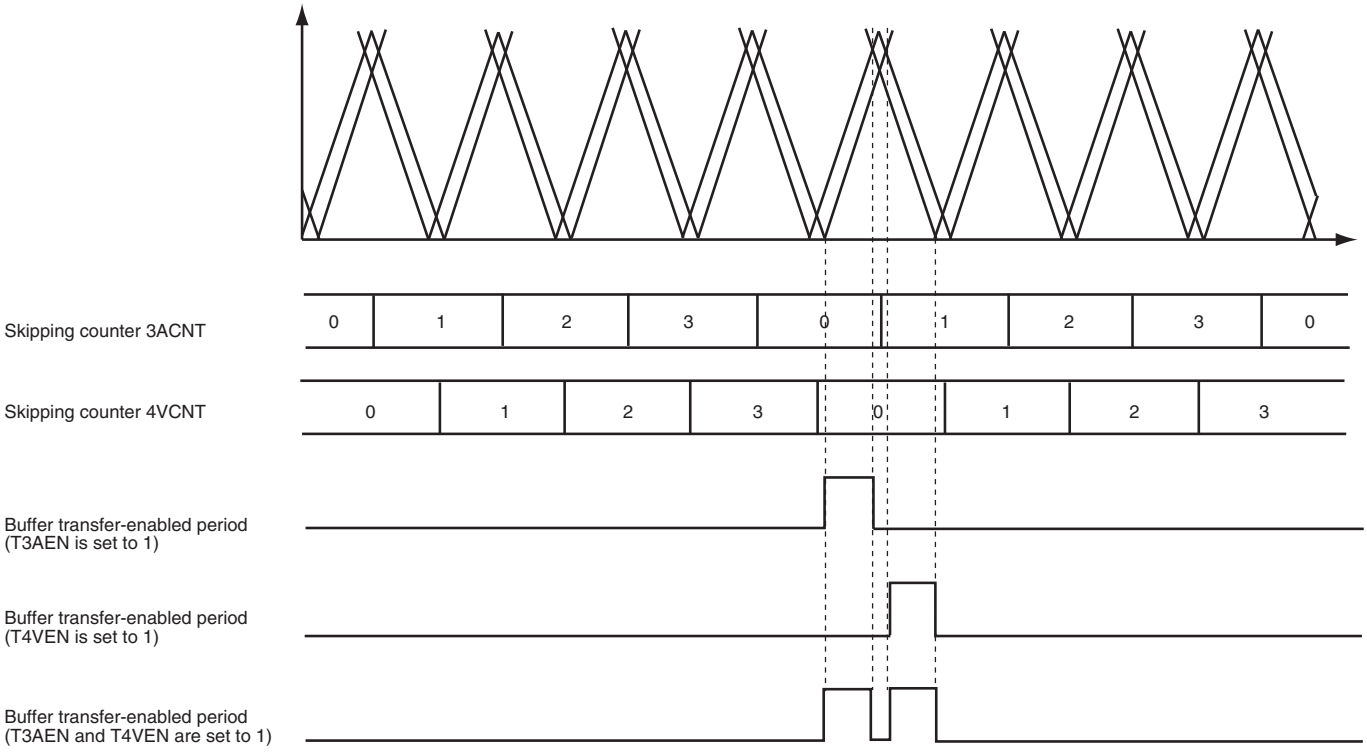
Page 515, Figure 10.78 Relationship between Bits T3AEN and T4VEN in TITCR and Buffer Transfer-Enabled Period

[Before Change]



Note: * The skipping count is set to three.

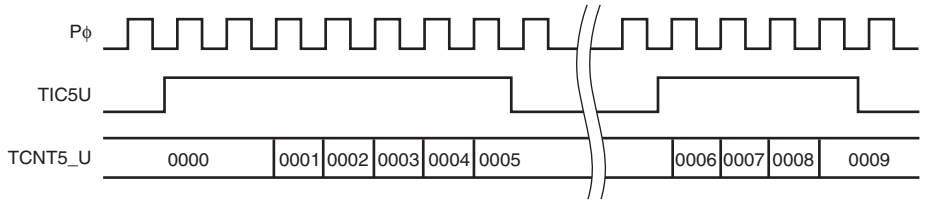
[After Change]



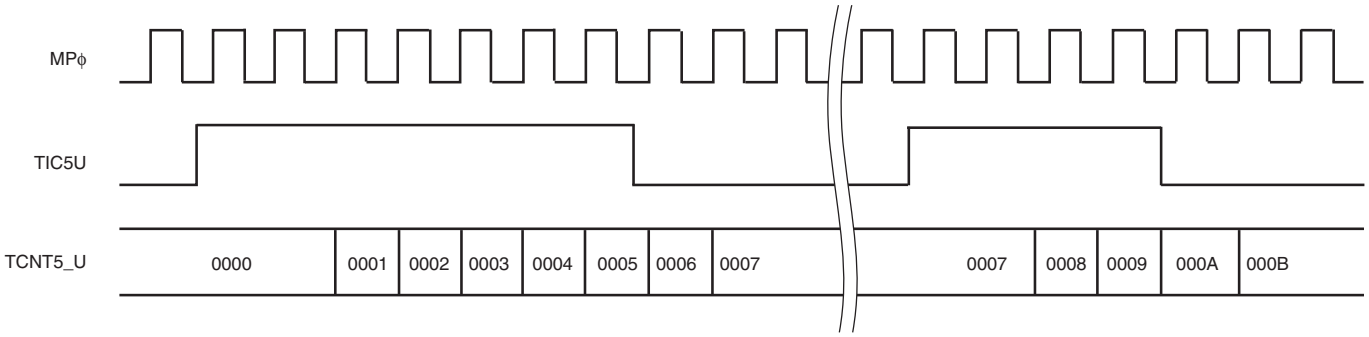
Note: MD[3:0] in TMDR_3 = 1111
Buffer transfer at the crest and trough is selected.
The skipping count is set to three.
T3AEN and T4VEN are set to 1.

Page 527, Figure 10.88 Example of External Pulse Width Measurement (Measuring High Pulse Width)

[Before Change]



[After Change]



Page 564, 10.7.22 Simultaneous Capture of TCNT_1 and TCNT_2 in Cascade Connection

[Addition]

The MTU2 additionally supports the function that can capture TCNT_1 and TCNT_2 simultaneously via a single input capture input. This function allows 32-bit counter fetches without TCNT_1 and TCNT_2 capture timing deviation. For details, see section 10.3.8, Timer Input Capture Control Register (TICCR).

Section 12. Port Output Enable 2 (POE2)

Page 633, 12.6 Usage Note

[Before Change]

12.6.1 Note when the WDT Issues a Power-On Reset

When a power-on reset is issued by the WDT during high-impedance control by the POE signals, the pins are placed in output state for a time period of one cycle of the peripheral clock, Pϕ, until the pin function switches to general input.

[After Change]

12.6.1 Pin Status When the WDT Issues a Power-On Reset

When a power-on reset is issued by the WDT, the pin function controller (PFC) is initialized and the I/O ports function as general inputs (initial value).

If a power-on reset is issued by the WDT during high-impedance processing by the port output enable (POE) signal, the I/O port pins are placed in output state for a time period of one cycle of the peripheral clock, Pϕ, until the pin functions switch to general inputs.

If a power-on reset is issued by the WDT during high-impedance processing by MTU2 or MTU2S short detection, the I/O port pins are placed in the same status as described above.

Figure 12.5 shows the I/O port pin status when a power-on reset is issued by the WDT during high-impedance processing by the POE input while the timer output is selected.

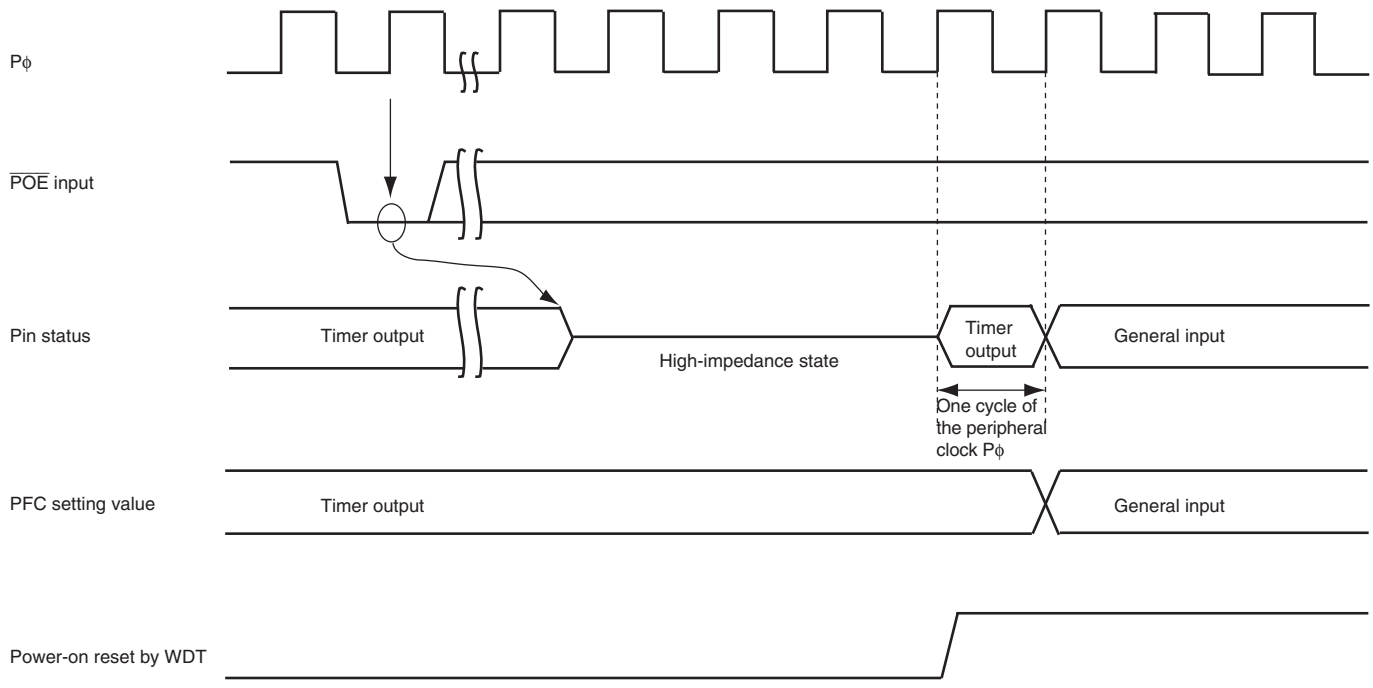


Figure 12.5 Pin Status When Power-on Reset Is Issued from Watchdog Timer

Section 15. Serial Communication Interface with FIFO (SCIF)

Page 664, 15.1 Features

[Before Change]

- In asynchronous mode, on-chip modem control functions (RTS and CTS) (only channel 3).

[After Change]

Deleted

Page 680, 15.3.7 Serial Status Register (SCFSR)

[Before Change]

Bit	Bit Name	Initial Value	R/W	Description
5	TDFE	1	R/(W)*	Transmit FIFO Data Empty Indicates that data has been transferred from the transmit FIFO data register (SCFTDR) to the transmit shift register (SCTSR), the quantity of data in SCFTDR has become less than the transmission trigger number specified by the TTRG1 and TTRG0 bits in the FIFO control register (SCFCR), and writing of transmit data to SCFTDR is enabled. 0: The quantity of transmit data written to SCFTDR is greater than the specified transmission trigger number [Clearing conditions] • TDFE is cleared to 0 when data exceeding the specified transmission trigger number is written to SCFTDR after 1 is read from TDFE and then 0 is written • TDFE is cleared to 0 when data exceeding the specified transmission trigger number is written to SCFTDR by the DMAC. 1: The quantity of transmit data in SCFTDR is less than the specified transmission trigger number* [Setting conditions] • TDFE is set to 1 by a power-on reset • TDFE is set to 1 when the quantity of transmit data in SCFTDR becomes less than the specified transmission trigger number as a result of transmission. Note: * Since SCFTDR is a 16-byte FIFO register, the maximum quantity of data that can be written when TDFE is 1 is "16 minus the specified transmission trigger number". If an attempt is made to write additional data, the data is ignored. The quantity of data in SCFTDR is indicated by the upper 8 bits of SCFDR.

[After Change]

Bit	Bit Name	Initial Value	R/W	Description
5	TDFE	1	R/(W)*	Transmit FIFO Data Empty Indicates that data has been transferred from the transmit FIFO data register (SCFTDR) to the transmit shift register (SCTSR), the quantity of data in SCFTDR has become less than the transmission trigger number specified by the TTRG1 and TTRG0 bits in the FIFO control register (SCFCR), and writing of transmit data to SCFTDR is enabled. 0: The quantity of transmit data written to SCFTDR is greater than the specified transmission trigger number [Clearing conditions] • TDFE is cleared to 0 when data exceeding the specified transmission trigger number is written to SCFTDR after 1 is read from TDFE and then 0 is written • TDFE is cleared to 0 when data exceeding the specified transmission trigger number is written to SCFTDR by the DMAC. 1: The quantity of transmit data in SCFTDR is equal to or less than the specified transmission trigger number* [Setting conditions] • TDFE is set to 1 by a power-on reset • TDFE is set to 1 when the quantity of transmit data in SCFTDR becomes equal to or less than the specified transmission trigger number as a result of transmission. Note: * Since SCFTDR is a 16-byte FIFO register, the maximum quantity of data that can be written when TDFE is 1 is "16 minus the specified transmission trigger number". If an attempt is made to write additional data, the data is ignored. The quantity of data in SCFTDR is indicated by the upper 8 bits of SCFDR.

Page 685, 15.3.8 Bit Rate Register (SCBRR)

[Before Change]

Each channel has independent baud rate generator control, so different values can be set in three channels.

[After Change]

Each channel has independent baud rate generator control, so different values can be set in four channels.

Pages 687 to 689, Table 15.4 Bit Rates and SCBRR Settings (Asynchronous Mode)

[Before Change]

Table 15.4 Bit Rates and SCBRR Settings (Asynchronous Mode)

Bit Rate (bit/s)	Pϕ (MHz) 5			6			6.144			7.37288		
	n	N	Error (%)	n	N	Error (%)	n	N	Error (%)	n	N	Error (%)
110	2	88	–0.25	2	106	–0.44	2	108	0.08	2	130	–0.07
150	2	64	0.16	2	77	0.16	2	79	0.00	2	95	0.00
300	1	129	0.16	1	155	0.16	1	159	0.00	1	191	0.00
600	1	64	0.16	1	77	0.16	1	79	0.00	1	95	0.00
1200	0	129	0.16	0	155	0.16	0	159	0.00	0	191	0.00
2400	0	64	0.16	0	77	0.16	0	79	0.00	0	95	0.00
4800	0	32	–1.36	0	38	0.16	0	39	0.00	0	47	0.00
9600	0	15	1.73	0	19	–2.34	0	19	0.00	0	23	0.00
19200	0	7	1.73	0	9	–2.34	0	9	0.00	0	11	0.00
31250	0	4	0.00	0	5	0.00	0	5	2.40	0	6	5.33
38400	0	3	1.73	0	4	–2.34	0	4	0.00	0	5	0.00

Bit Rate (bit/s)	Pϕ (MHz) 8			9.8304			10			12		
	n	N	Error (%)	n	N	Error (%)	n	N	Error (%)	n	N	Error (%)
110	2	141	0.03	2	174	–0.26	2	177	–0.25	2	212	0.03
150	2	103	0.16	2	127	0.00	2	129	0.16	2	155	0.16
300	1	207	0.16	1	255	0.00	2	64	0.16	2	77	0.16
600	1	103	0.16	1	127	0.00	1	129	0.16	1	155	0.16
1200	0	207	0.16	0	255	0.00	1	64	0.16	1	77	0.16
2400	0	103	0.16	0	127	0.00	0	129	0.16	0	155	0.16
4800	0	51	0.16	0	63	0.00	0	64	0.16	0	77	0.16
9600	0	25	0.16	0	31	0.00	0	32	–1.36	0	38	0.16
19200	0	12	0.16	0	15	0.00	0	15	1.73	0	19	0.16
31250	0	7	0.00	0	9	–1.70	0	9	0.00	0	11	0.00
38400	0	6	–6.99	0	7	0.00	0	7	1.73	0	9	–2.34

Bit Rate (bit/s)	Pϕ (MHz) 12.288 n	N	Error (%)	14.7456 n	N	Error (%)	16 n	N	Error (%)	19.6608 n	N	Error (%)
110	2	217	0.08	3	64	0.70	3	70	0.03	3	86	0.31
150	2	159	0.00	2	191	0.00	2	207	0.16	2	255	0.00
300	2	79	0.00	2	95	0.00	2	103	0.16	2	127	0.00
600	1	159	0.00	1	191	0.00	1	207	0.16	1	255	0.00
1200	1	79	0.00	1	95	0.00	1	103	0.16	1	127	0.00
2400	0	159	0.00	0	191	0.00	0	207	0.16	0	255	0.00
4800	0	79	0.00	0	95	0.00	0	103	0.16	0	127	0.00
9600	0	39	0.00	0	47	0.00	0	51	0.16	0	63	0.00
19200	0	19	0.00	0	23	0.00	0	25	0.16	0	31	0.00
31250	0	11	2.40	0	14	–1.70	0	15	0.00	0	19	–1.70
38400	0	9	0.00	0	11	0.00	0	12	0.16	0	15	0.00

Note: This is an example when ABCS in SCSEMR is 0. When ABCS = 1, the bit rate is doubled.

Bit Rate (bit/s)	Pϕ (MHz) 20 n	N	Error (%)	24 n	N	Error (%)	24.576 n	N	Error (%)	28.7 n	N	Error (%)
110	3	88	–0.25	3	106	–0.44	3	108	0.08	3	126	0.31
150	3	64	0.16	3	77	0.16	3	79	0.00	3	92	0.46
300	2	129	0.16	2	155	0.16	2	159	0.00	2	186	–0.08
600	2	64	0.16	2	77	0.16	2	79	0.00	2	92	0.46
1200	1	129	0.16	1	155	0.16	1	159	0.00	1	186	–0.08
2400	1	64	0.16	1	77	0.16	1	79	0.00	1	92	0.46
4800	0	129	0.16	0	155	0.16	0	159	0.00	0	186	–0.08
9600	0	64	0.16	0	77	0.16	0	79	0.00	0	92	0.46
19200	0	32	–1.36	0	38	0.16	0	39	0.00	0	46	–0.61
31250	0	19	0.00	0	23	0.00	0	24	–1.70	0	28	–1.03
38400	0	15	1.73	0	19	–2.34	0	19	0.00	0	22	1.55

Bit Rate (bit/s)	Pϕ (MHz) 30 n	N	Error (%)	33 n	N	Error (%)	40 n	N	Error (%)
110	3	132	0.13	3	145	0.33	3	117	–0.25
150	3	97	–0.35	3	106	0.39	3	129	0.16
300	2	194	0.16	2	214	–0.07	3	64	0.16
600	2	97	–0.35	2	106	0.39	2	129	0.16
1200	1	194	0.16	1	214	–0.07	2	64	0.16
2400	1	97	–0.35	1	106	0.39	1	129	0.16
4800	0	194	–1.36	0	214	–0.07	1	64	0.16
9600	0	97	–0.35	0	106	0.39	0	129	0.16
19200	0	48	–0.35	0	53	–0.54	0	64	0.16
31250	0	29	0.00	0	32	0.00	0	39	0.00
38400	0	23	1.73	0	26	–0.54	0	32	–1.36

Note: Settings with an error of 1% or less are recommended.

[After Change]

Table 15.4 Bit Rates and SCBRR Settings (Asynchronous Mode)

Bit Rate (bit/s)	Pϕ (MHz)								
	32			36			40		
	n	N	Error (%)	n	N	Error (%)	n	N	Error (%)
110	3	141	0.03	3	159	–0.12	3	177	–0.25
150	3	103	0.16	3	116	0.16	3	129	0.16
300	3	51	0.16	3	58	–0.69	3	64	0.16
600	2	103	0.16	2	116	0.16	2	129	0.16
1200	2	51	0.16	2	58	–0.69	2	64	0.16
2400	1	103	0.16	1	116	0.16	1	129	0.16
4800	1	51	0.16	1	58	–0.69	1	64	0.16
9600	0	103	0.16	0	116	0.16	0	129	0.16
19200	0	51	0.16	0	58	–0.69	0	64	0.16
31250	0	31	0.00	0	35	0.00	0	39	0.00
38400	0	25	0.16	0	28	1.02	0	32	–1.36

Note: Settings with an error of 1% or less are recommended.

Page 690, Table 15.5 Bit Rates and SCBRR Settings (Clocked Synchronous Mode)

[Before Change]

Bit Rate (bit/s)	Pϕ (MHz)													
	5		8		16		28.7		30		33		40	
	n	N	n	N	n	N	n	N	n	N	n	N	n	N
110														
250	3	77	3	124	3	249								
500	3	38	2	249	3	124	3	223	3	233	3	255	—	—
1 k	2	77	2	124	2	249	3	111	3	116	3	125	3	152
2.5 k	1	124	1	199	2	99	2	178	2	187	2	200	2	243
5 k	0	249	1	99	1	199	2	89	2	93	2	100	2	121
10 k	0	124	0	199	1	99	1	178	1	187	1	200	2	60
25 k	0	49	0	79	0	159	1	71	1	74	1	80	1	97
50 k	0	24	0	39	0	79	0	143	0	149	0	160	1	48
100 k	—	—	0	19	0	39	0	71	0	74	0	80	0	97
250 k	0	4	0	7	0	15	—	—	0	29	0	31	0	38
500 k	—	—	0	3	0	7	—	—	0	14	0	15	0	19
1 M			0	1	0	3					0	7	0	9
2 M			0	0*	0	1							0	3

[Legend]

Blank: No setting possible

—: Setting possible, but error occurs

*: Continuous transmission/reception not possible

[After Change]

Bit Rate (bit/s)	Pϕ (MHz)					
	32		36		40	
	n	N	n	N	n	N
500	—	—				
1 k	3	124	3	140	3	155
2.5 k	2	199	2	224	2	249
5 k	2	99	2	112	2	124
10 k	2	49	2	55	2	62
25 k	1	79	1	89	1	97
50 k	1	39	1	44	1	48
100 k	0	79	0	89	0	97
250 k	0	31	0	35	0	38
500 k	0	15	0	17	0	19
1 M	0	7	0	8	0	9
2 M	0	3	—	—	0	4

[Legend]
Blank: No setting possible
—: Setting possible, but error occurs

Page 691, Table 15.6 Maximum Bit Rates for Various Frequencies with Baud Rate Generator (Asynchronous Mode)

[Before change]

Pϕ (MHz)	Maximum Bit Rate (bits/s)	Settings	
		n	N
5	156250	0	0
8	250000	0	0
9.8304	307200	0	0
12	375000	0	0
14.7456	460800	0	0
16	500000	0	0
19.6608	614400	0	0
20	625000	0	0
24	750000	0	0
24.576	768000	0	0
28.7	896875	0	0
30	937500	0	0
33	1031250	0	0
40	1250000	0	0

[After Change]

		Settings	
Pϕ (MHz)	**Maximum Bit Rate (bits/s)**	**n**	**N**
32	1000000	0	0
36	1125000	0	0
40	1250000	0	0

Page 692, Table 15.7 Maximum Bit Rates with External Clock Input (Asynchronous Mode)

[Before change]

Pϕ (MHz)	**External Input Clock (MHz)**	**Maximum Bit Rate (bits/s)**
5	1.2500	78125
8	2.0000	125000
9.8304	2.4576	153600
12	3.0000	187500
14.7456	3.6864	230400
16	4.0000	250000
19.6608	4.9152	307200
20	5.0000	312500
24	6.0000	375000
24.576	6.1440	384000
28.7	7.1750	448436
30	7.5000	468750
33	8.2500	515625
40	10.0000	625000

[After Change]

Pϕ (MHz)	**External Input Clock (MHz)**	**Maximum Bit Rate (bits/s)**
32	8.0000	500000
36	9.0000	562500
40	10.0000	625000

Page 692, Table 15.8 Maximum Bit Rates with External Clock Input (Clocked Synchronous Mode, $t_{Scyc} = 12t_{pcyc}$)

[Before change]

Pϕ (MHz)	External Input Clock (MHz)	Maximum Bit Rate (bits/s)
5	0.4166	416666.6
8	0.6666	666666.6
16	1.3333	1333333.3
24	2.0000	2000000.0
28.7	2.3916	2391666.6
30	2.5000	2500000.0
33	2.7500	2750000.0

Note: Confirm that these bit rates meet the electrical characteristics of this LSI and the remote communication device.

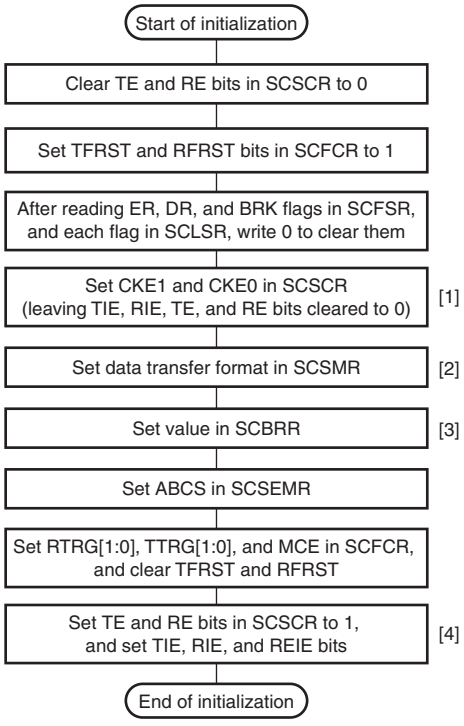
[After Change]

Pϕ (MHz)	External Input Clock (MHz)	Maximum Bit Rate (bits/s)
32	2.6667	2666666.7
36	3.0000	3000000.0
40	3.3333	3333333.3

Note: Confirm that these bit rates meet the electrical characteristics of this LSI and the remote communication device.

Page 705, Figure 15.3 Sample of Flowchart for SCIF Initialization

[Before Change]



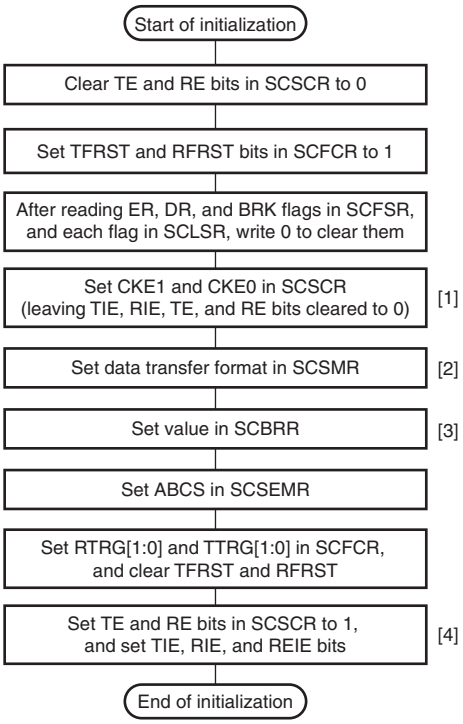
[1] Set the clock selection in SCSCR. Be sure to clear bits TIE, RIE, TE, and RE to 0.

[2] Set the data transfer format in SCSMR.

[3] Write a value corresponding to the bit rate into SCBRR. (Not necessary if an external clock is used.)

[4] Set the TE bit or RE bit in SCSCR to 1. Also set the RIE, REIE, and TIE bits. Setting the TE and RE bits enables the TxD and RxD pins to be used.
When transmitting, the SCIF will go to the mark state; when receiving, it will go to the idle state, waiting for a start bit.

[After Change]



[1] Set the clock selection in SCSCR. Be sure to clear bits TIE, RIE, TE, and RE to 0.

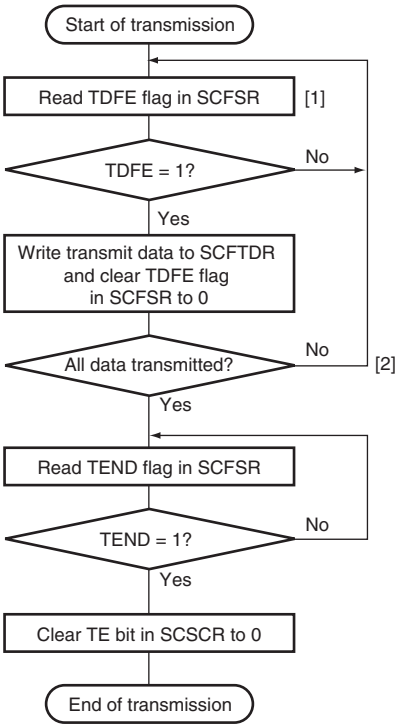
[2] Set the data transfer format in SCSMR.

[3] Write a value corresponding to the bit rate into SCBRR. (Not necessary if an external clock is used.)

[4] Set the TE bit or RE bit in SCSCR to 1. Also set the RIE, REIE, and TIE bits. Setting the TE and RE bits enables the TxD and RxD pins to be used.
When transmitting, the SCIF will go to the mark state; when receiving, it will go to the idle state, waiting for a start bit.

Page 715, Figure 15.11 Sample Flowchart for Transmitting Serial Data

[Before Change]



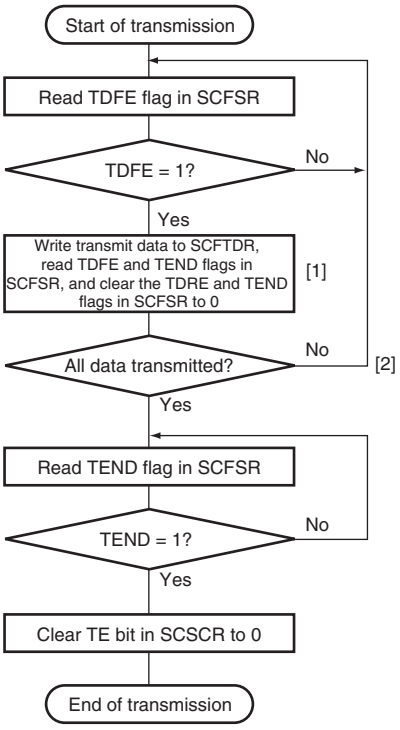
[1] SCIF status check and transmit data write:

Read SCFSR and check that the TDFE flag is set to 1, then write transmit data to SCFTDR, and clear the TDFE flag to 0.

[2] Serial transmission continuation procedeure:

To continue serial transmission, read 1 from the TDFE flag to confirm that writing is possible, them write data to SCFTDR, and then clear the TDFE flag to 0.

[After Change]



[1] SCIF status check and transmit data write:

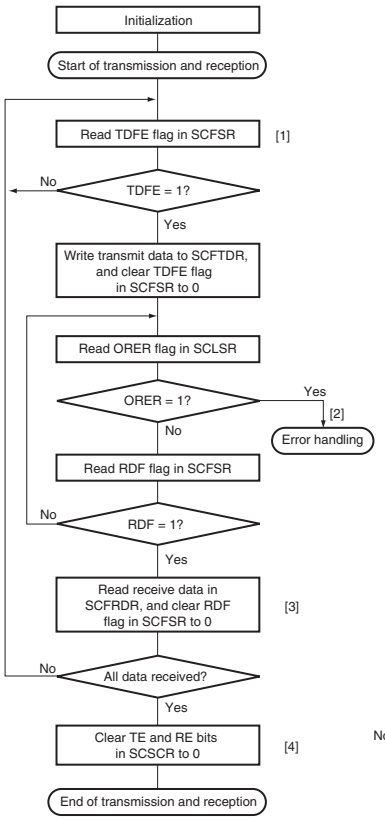
Read SCFSR and check that the TDFE flag is set to 1, then write transmit data to SCFTDR, read 1 from the TDFE and TEND flags, and clear these flags to 0.

[2] Serial transmission continuation procedeure:

To continue serial transmission, read 1 from the TDFE flag to confirm that writing is possible, them write data to SCFTDR, and then clear the TDFE flag to 0.

Page 720, Figure 15.16 Sample Flowchart for Transmitting/Receiving Serial Data

[Before Change]



[1] SCIF status check and transmit data write:

Read SCFSR and check that the TDFE flag is set to 1, then write transmit data to SCFTDR, and clear the TDFE flag to 0. The transition of the TDFE flag from 0 to 1 can also be identified by a TXI interrupt.

[2] Receive error handling:

Read the ORER flag in SCLSR to identify any error, perform the appropriate error handling, then clear the ORER flag to 0. Reception cannot be resumed while the ORER flag is set to 1.

[3] SCIF status check and receive data read:

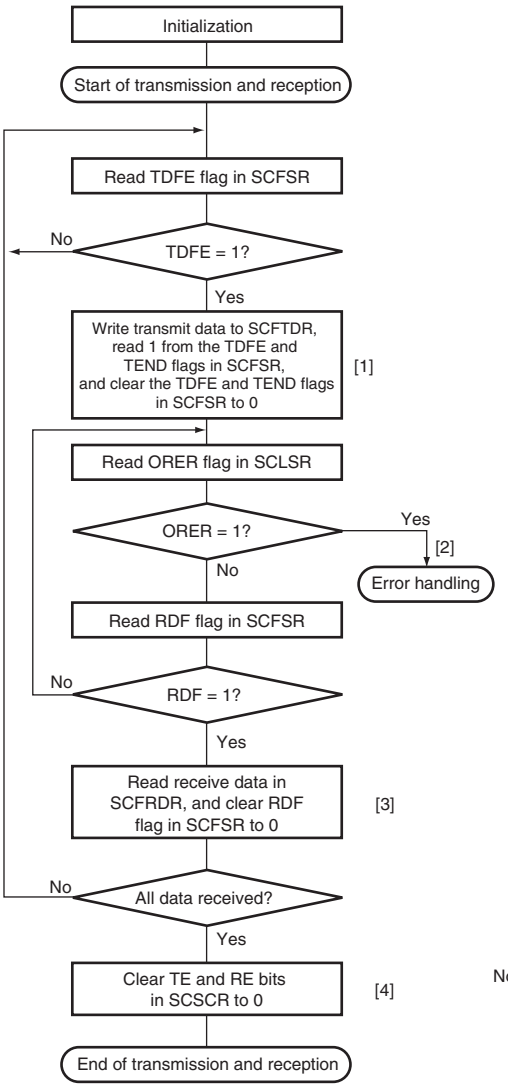
Read SCFSR and check that RDF flag = 1, then read the receive data in SCFRDR, and clear the RDF flag to 0. The transition of the RDF flag from 0 to 1 can also be identified by an RXI interrupt.

[4] Serial transmission and reception continuation procedure:

To continue serial transmission and reception, read 1 from the RDF flag and the receive data in SCFRDR, and clear the RDF flag to 0 before receiving the MSB in the current frame. Similarly, read 1 from the TDFE flag to confirm that writing is possible before transmitting the MSB in the current frame. Then write data to SCFTDR and clear the TDFE flag to 0.

Note: When switching from a transmit operation or receive operation to simultaneous transmission and reception operations, clear the TE and RE bits to 0, and then set them simultaneously to 1.

[After Change]



[1] SCIF status check and transmit data write:

Read SCFSR and check that the TDFE flag is set to 1, then write transmit data to SCFTDR, read 1 from the TDFE and TEND flags, and clear these flags to 0. The transition of the TDFE flag from 0 to 1 can also be identified by a TXI interrupt.

[2] Receive error handling:

Read the ORER flag in SCLSR to identify any error, perform the appropriate error handling, then clear the ORER flag to 0. Reception cannot be resumed while the ORER flag is set to 1.

[3] SCIF status check and receive data read:

Read SCFSR and check that RDF flag = 1, then read the receive data in SCFRDR, and clear the RDF flag to 0. The transition of the RDF flag from 0 to 1 can also be identified by an RXI interrupt.

[4] Serial transmission and reception continuation procedure:

To continue serial transmission and reception, read 1 from the RDF flag and the receive data in SCFRDR, and clear the RDF flag to 0 before receiving the MSB in the current frame. Similarly, read 1 from the TDFE flag to confirm that writing is possible before transmitting the MSB in the current frame. Then write data to SCFTDR and clear the TDFE flag to 0.

Note: When switching from a transmit operation or receive operation to simultaneous transmission and reception operations, clear the TE and RE bits to 0, and then set them simultaneously to 1.

Page 725, 15.6.7 FER and PER Flags in the Serial Status Register (SCFSR)

[Addition]

15.6.7 FER and PER Flags in the Serial Status Register (SCFSR)

The FER (framing error) and PER (parity error) flags in the serial status register (SCFSR) are status flags of the receive FIFO data register (SCFRDR) to be read next. If the CPU or DMAC reads the receive FIFO data register, the FER (framing error) and PER (parity error) flags of the current receive data will be lost. To check the framing error and parity error status of the current receive data correctly, the serial status register (SCFSR) should be read before the receive FIFO data register is read.

Section 16. I²C Bus Interface 3 (IIC3)

Page 731, 16.3.1 I²C Bus Control Register 1 (ICCR1)

[Before change]

Bit	Bit Name	Initial Value	R/W	Description
6	RCVD	0	R/W	Reception Disable Enables or disables the next operation when TRS is 0 and ICDRR is read. 0: Enables next reception 1: Disables next reception

[After change]

Bit	Bit Name	Initial Value	R/W	Description
6	RCVD	0	R/W	Reception Disable Enables or disables continuous reception when TRS = 0 and ICDRR is not read. If ICDRR cannot be read by the rising of 8th clock cycle of SCL in master receive mode, reception in byte units should be performed by setting the RCVD bit to 1. 0: Enables continuous reception 1: Disables continuous reception

Page 733, Table 16.3 Transfer Rate

[Before Change]

Bit 3	Bit 2	Bit 1	Bit 0		Transfer Rate		
CKS3	CKS2	CKS1	CKS0	Clock	Pϕ = 20.0 MHz (160/8)	Pϕ = 26.7 MHz (160/6)	Pϕ = 40.0 MHz (160/4)
0	0	0	0	Pϕ/44	455	606	909
			1	Pϕ/52	385	513	769
		1	0	Pϕ/64	313	417	625
			1	Pϕ/72	278	370	556
	1	0	0	Pϕ/84	238	317	476
			1	Pϕ/92	217	290	435
		1	0	Pϕ/100	200	267	400
			1	Pϕ/108	185	247	370
1	0	0	0	Pϕ/176	114	152	227
			1	Pϕ/208	96.2	128	192
		1	0	Pϕ/256	78.1	104	156
			1	Pϕ/288	69.4	92.6	139
	1	0	0	Pϕ/336	59.5	79.4	119
			1	Pϕ/368	54.3	72.5	109
		1	0	Pϕ/400	50.0	66.7	100
			1	Pϕ/432	46.3	61.7	92.6

Note: The settings should satisfy external specifications.

[After Change]

Bit 3	Bit 2	Bit 1	Bit 0		Transfer Rate		
CKS3	CKS2	CKS1	CKS0	Clock	Pϕ = 32 MHz (128/4)	Pϕ = 36 MHz (144/4)	Pϕ = 40 MHz (160/4)
0	0	0	0	Pϕ/44	727.3	818.2	909.1
			1	Pϕ/52	615.4	692.3	769.2
		1	0	Pϕ/64	500.0	562.5	625.0
			1	Pϕ/72	444.4	500.0	555.6
	1	0	0	Pϕ/84	381.0	428.6	476.2
			1	Pϕ/92	347.8	391.3	434.8
		1	0	Pϕ/100	320.0	360.0	400.0
			1	Pϕ/108	296.3	333.3	370.4
1	0	0	0	Pϕ/176	181.8	204.5	227.3
			1	Pϕ/208	153.8	173.1	192.3
		1	0	Pϕ/256	125.0	140.6	156.3
			1	Pϕ/288	111.1	125.0	138.9
	1	0	0	Pϕ/336	95.2	107.1	119.0
			1	Pϕ/368	87.0	97.8	108.7
		1	0	Pϕ/400	80.0	90.0	100.0
			1	Pϕ/432	74.1	83.3	92.6

Note: The settings should satisfy external specifications.

Page 736, 16.3.3 I^2C Bus Mode Register (ICMR)

[Before Change]

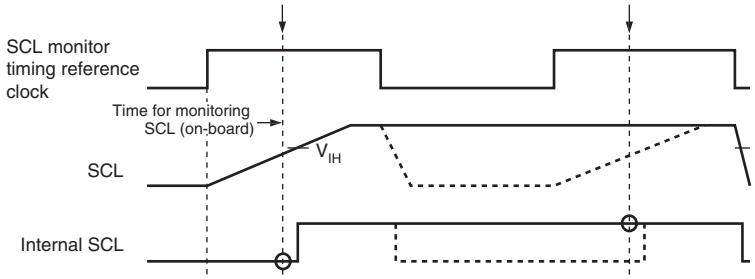
Bit	Bit Name	Initial Value	R/W	Description
6	WAIT	0	R/W	Master Mode Wait Control

[After change]

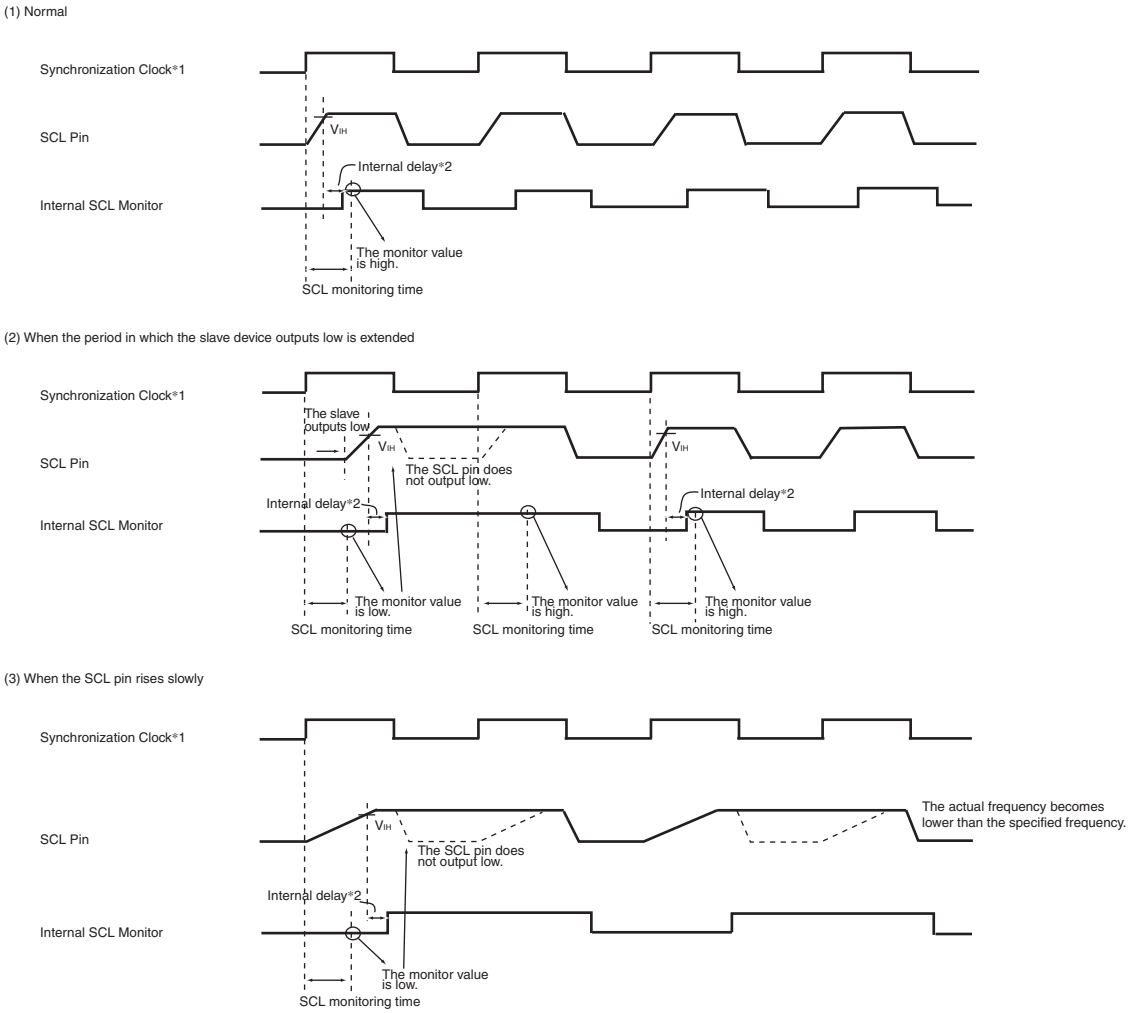
Bit	Bit Name	Initial Value	R/W	Description
6	—	0	R	Reserved This bit is always read as 0. The write value should always be 0.

Page 766, 16.6 Bit Synchronous Circuit, Figure 16.22 Bit Synchronous Circuit Timing

[Before Change]



[After Change]



Notes: 1. A clock whose transfer rate is specified by the CKS[3:0] bits in the I2C bus control register (ICCR1).
2. 3 to 4 tpcyc when the NF2CYC bit in the NF2CYC register (NF2CYC) is cleared to 0; 4 to 5 tpcyc when the NF2CYC bit in NF2CYC is set to 1.

Page 766, Table 16.5 Time for Monitoring SCL

[Before Change]

CKS3	CKS2	Time for Monitoring SCL*[1]
0	0	9 tpcyc*[2]
	1	21 tpcyc*[2]
1	0	19 tpcyc*[2]
	1	43 tpcyc*[2]

Notes: 1. Monitors the (on-board) SCL level after the time (pcyc) for monitoring SCL has passed since the rising edge of the SCL monitor timing reference clock.
2. pcyc= Pϕ × cyc

[After change]

CKS3	CKS2	Time for Monitoring SCL
0	0	9 tpcyc*
	1	21 tpcyc*
1	0	33 tpcyc*
	1	81 tpcyc*

Note: * tpcyc stands for the peripheral clock (Pϕ) cycle.

Page 766, 16.7 Usage Notes are added as follows:

[Addition]

16.7.1 Note on Multiple Master Usage

With multi-master used, if the transfer rate setting (CKS[3:0] in ICCR1) of I^2C in this LSI is slower than the other masters, the SCL with unexpected width may be output in rare cases.

To prevent this problem, the transfer rate of I^2C should be specified as equal to or higher than 1/1.8 of the highest transfer rate among the other masters.

16.7.2 Note on Master Receive Mode

If ICDRR is read near the falling edge of 8th clock, the receive data will not be received in some cases. In addition, if RCVD is set to 1 near the falling edge of 8th clock, a stop condition cannot be issued in some cases. To prevent these errors, one of the following two methods should be selected.

1. In master receive mode, ICDRR should be read before the falling edge of 8th clock.
2. In master receive mode, RCVD should be set to 1 and the processing should be performed in byte units.

16.7.3 Note on Master Receive Mode with ACKBT Setting

In master receive mode operation, ACKBT should be set before the 8th falling edge of SCL in the final data transfer during continuous data transfer. Otherwise, the slave device may overrun.

16.7.4 Note on MST and TRS Bit Status When an Arbitration was Lost

If the master transmission is set according to the MST and TRS bit settings while multiple masters are used, the conflicting status in which the AL bit in ICSR is set to 1 in master transmit mode (MST and TRS are set to 1) depending on the arbitration lost generation timing during TRS bit handling instruction execution.

This problem can be avoided by the following methods.

- When multiple masters are used, the MST and TRS bits should be set by a MOV instruction.
- When an arbitration lost occurs, check if both MST and TRS bits are cleared to 0. If either or both of MST and TRS bits are not cleared to 0, both the bits should be cleared to 0.

Section 17. A/D Converter (ADC)

Page 767, 17.1 Features, High Speed Conversion

[Before Change]

- High-speed conversion
  When Pϕ = 40 MHz: Minimum 1.25 μs per channel

[After Change]

- High-speed conversion
  When Aϕ = 40 MHz: Minimum 1.25 μs per channel

Page 784, Figure 17.4 A/D Conversion Timing (Single-Cycle Scan Mode)

[Before Change]

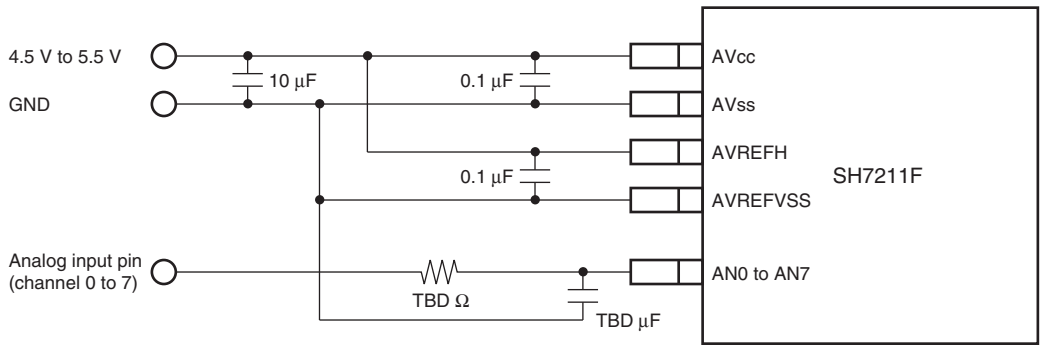
(When Pϕ = 40 MHz: 1.25 μs)

[After Change]

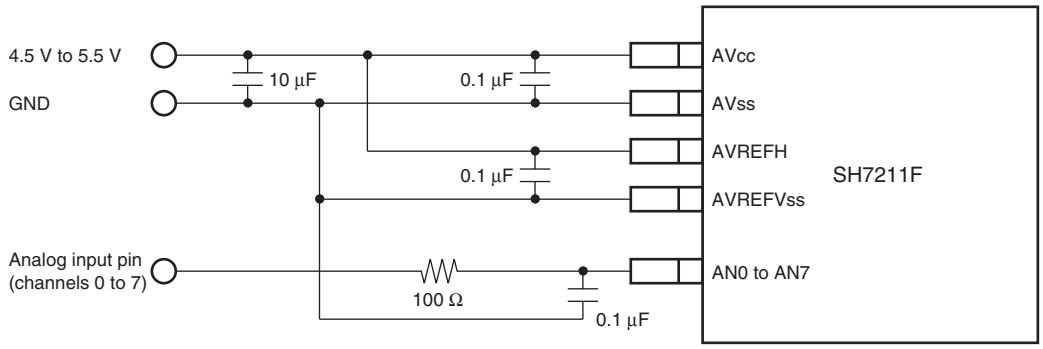
(When Aϕ = 40 MHz: 1.25 μs)

Page 792, Figure 17.8 Example of Analog Input Pin Protection Circuit

[Before Change]



[After Change]



Page 792, 17.7.7 Treatment of AV_{CC} and AV_{SS} When the A/D Converter is Not Used is added as follows.

[Addition]

17.7.7 Treatment of AV_{CC} and AV_{SS} When the A/D Converter is Not Used

When the A/D converter is not used, it is recommended that AV_{CC} be connected to $V_{CC}Q$ and AV_{SS} be connected to $V_{SS}Q$.

Section 18. D/A Converter (DAC)

Page 799, 18.5.3 Setting Analog Input Voltage

[Before Change]

1. AV_{CC} and AV_{SS} input voltages

   Input voltages AV_{CC} and AV_{SS} should be $V_{CC}Q - 0.3\ V \leq AV_{CC}$ and $AV_{SS} = V_{SS}Q$.

[After Change]

1. AV_{CC} and AV_{SS} input voltages

Input voltages AV_{CC} and AV_{SS} should be $V_{CC} \leq AV_{CC} \leq 5.0\ V \pm 0.5\ V$ and $AV_{SS} = V_{SS}$.

[Before Change]

2. Setting range of AVREF input voltage

   Set the voltage range of the AVREF pin as AVREF = 4.5 V to AV_{CC} when the A/D converter or D/A converter is used, or as AVREF = AV_{CC} when no A/D converter or D/A converter is used.

[After Change]

2. Setting range of AVREF input voltage

   Set the voltage range of the AVREF pin as AVREF = $AV_{CC} \pm 0.3$ V when the A/D converter or D/A converter is used, or as AVREF = AV_{CC} when no A/D converter or D/A converter is used.

Section 19. Pin Function Controller (PFC)

Page 808, 19.1 Register Description, Table 19.5 Register Configuration

[Before change]

Register Name	Abbreviation*4	R/W	Initial Value	Address	Access Size
IRQOUT function control register	IFCR	R/W	H'0000	H'FFFE3A22	16

[After change]

Register Name	Abbreviation*4	R/W	Initial Value	Address	Access Size
IRQOUT function control register	IFCR	R/W	H'0000	H'FFFFE38A2	16

Section 20. I/O Ports

Page 868, 20.2 Port B, Figure 20.2 Port

[Before change]

PB30 (input/output)/IRQOUT (output)/REFOUT (output)/UBCTRG (output)/ASEBRKAK (output)/ASEBRK (output)

[After Change]

PB30 (input/output)/IRQOUT (output)/REFOUT (output)/UBCTRG (output)/ASEBRKAK (output)/ASEBRK (input)

Section 21. Flash Memory

Page 884, 21.1 Features, Programming/erasing Time, Number of Programming Operations

[Before change]

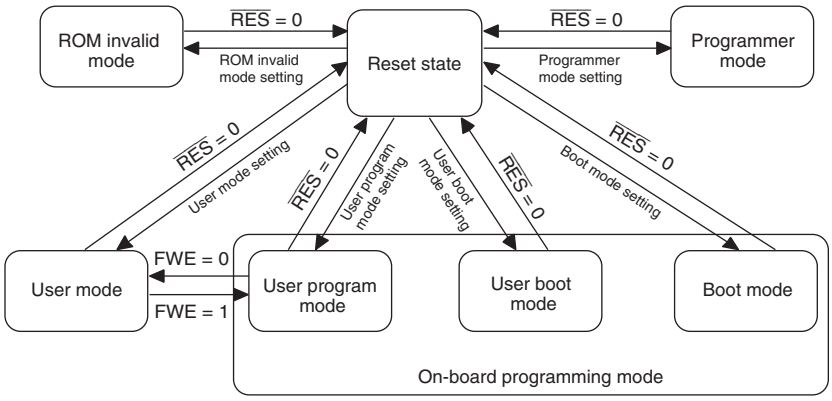
- Programming/erasing time
  The time taken to program 256 bytes of flash memory in a single round is t_P ms (typ.), which is equivalent to t_P/128 ms per byte. The erasing time is t_Es (typ.) per block.
- Number of programming operations
  The flash memory can be programmed up to N_{WEC} times.

[After Change]

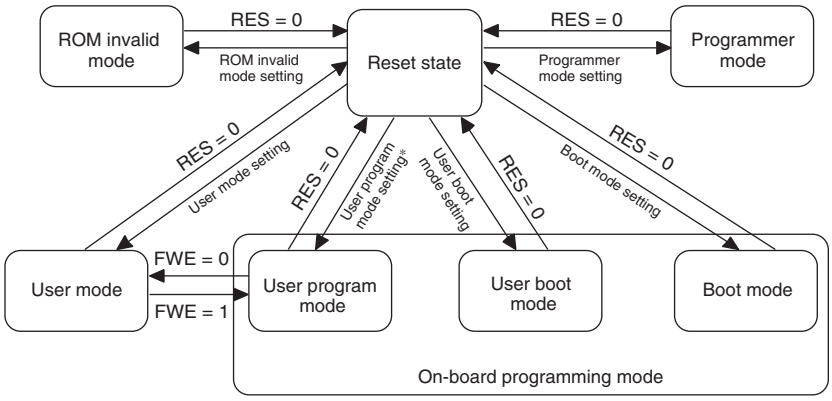
- Programming/erasing time
  The time taken to program 256 bytes of flash memory in a single round is 2 ms (typ.), which is equivalent to 7.8µs per byte. The erasing time is 80 ms (typ.) per 8-Kbyte block, 600 ms (typ.) per 64-Kbyte block, and 1200 ms (typ.) per 128-Kbyte block.
- Number of programming operations
  The flash memory can be programmed up to 100 times.

Page 886, Figure 21.2 Mode Transition of Flash Memory

[Before Change]



[After Change]



Note: * Except for single chip mode

Page 887, Table 21.1 Relation between FEW and MD Pins and Operating Mode

[Before Change]

Pin	Reset State	ROM Invalid Mode	ROM Valid Mode	User Program Mode	User Boot Mode	Boot Mode	Programmer Mode
MD0	0/1	0/1*[1]	0/1*[2]	0/1*[2]	1	0	Setting value depends on the condition of the specialized PROM programmer.

[After change]

Pin	Reset State	ROM Invalid Mode	ROM Valid Mode	User Program Mode	User Boot Mode	Boot Mode	Programmer Mode
MD0	0/1	0/1*1	0/1*2	0	1	0	Setting value depends on the condition of the specialized PROM programmer.

Page 912, (3) Programming Execution

[Before Change]

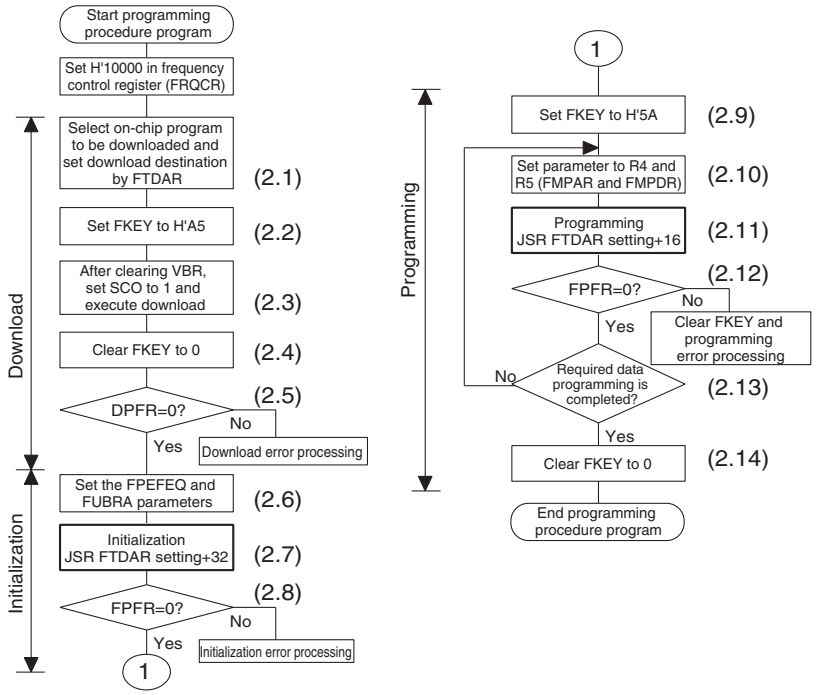
(3.3) Flash Pass/Fail Parameter (FPFR: General Register R0 of CPU)

[After change]

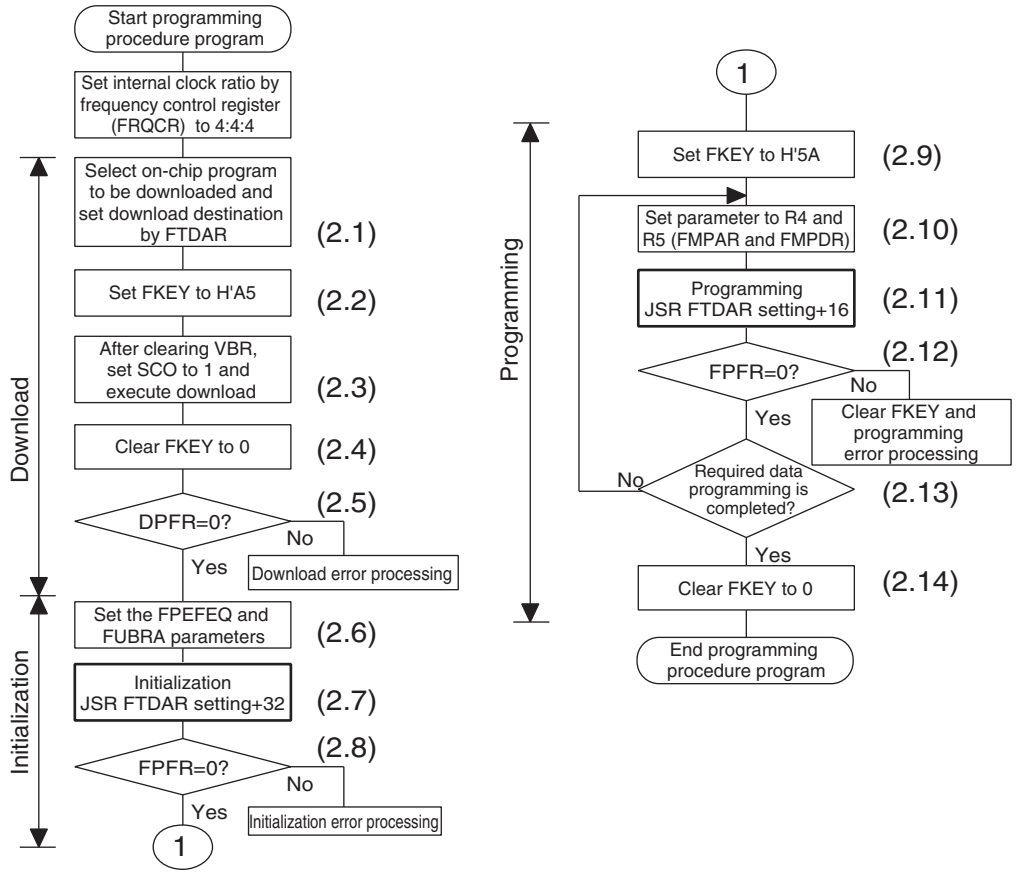
(3.3) Flash Pass/Fail Result Parameter (FPFR: General Register R0 of CPU)

Page 924, (2) Programming Procedure in User Program Mode, Figure 21.11 Programming Procedure

[Before Change]



[After Change]



Page 924

[Before Change]

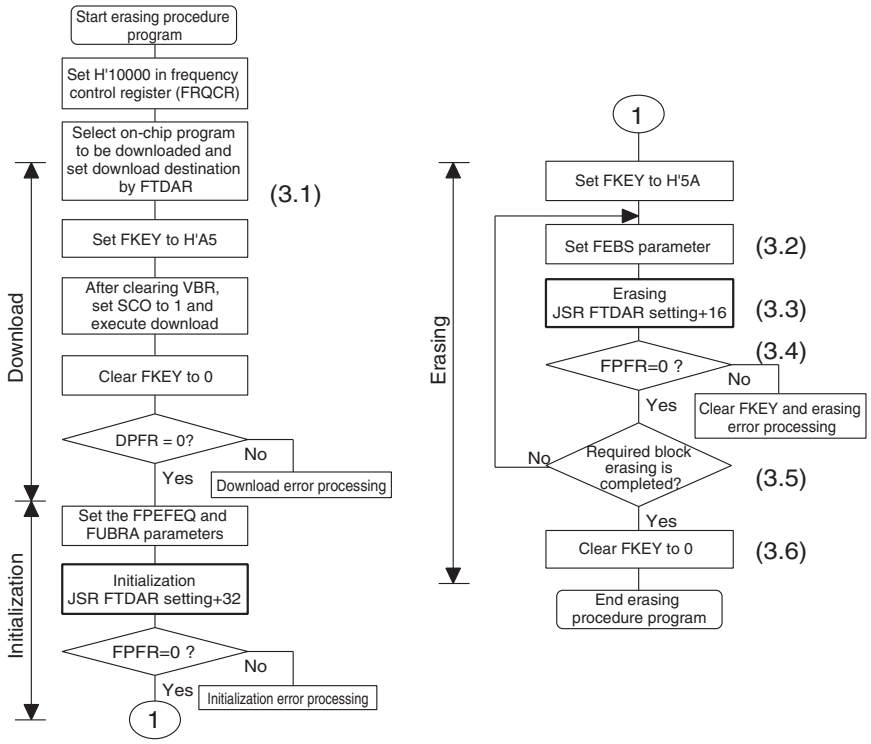
Specify 4:4:4 (H'1000) as the frequency division ratios of an internal clock (Iϕ), a bus clock (Bϕ), and a peripheral clock (Pϕ) through the frequency control register (FRQCR).

[After Change]

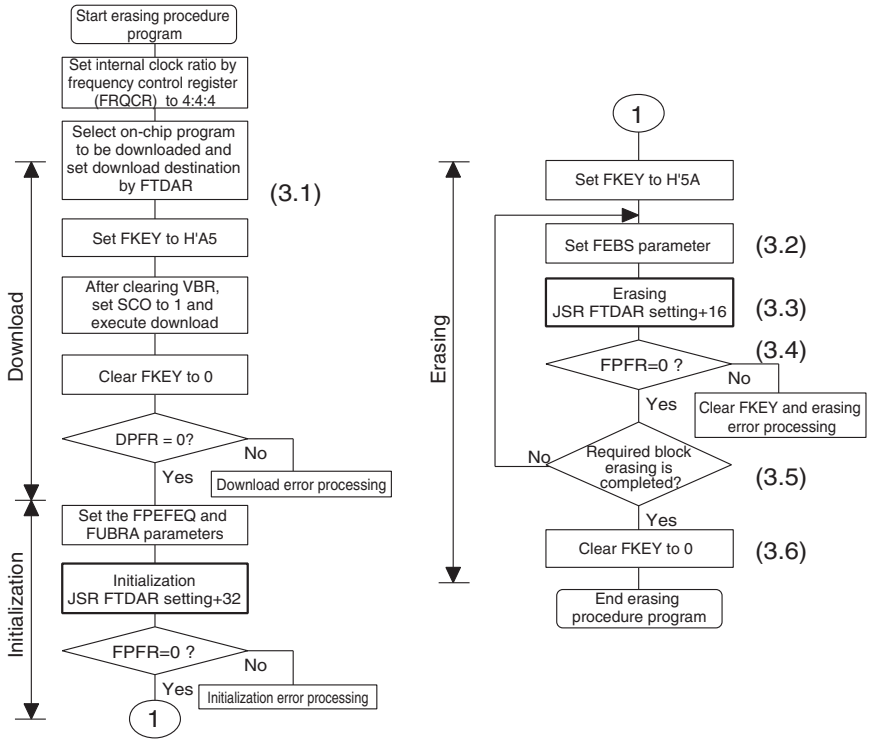
Specify 4:4:4 as the frequency division ratios of an internal clock (Iϕ), a bus clock (Bϕ), and a peripheral clock (Pϕ) through the frequency control register (FRQCR).

Page 930, (3) Erasing Procedure in User Program Mode, Figure 21.12 Erasing Procedure

[Before Change]



[After Change]



Page 931, (3) Erasing Procedure in User Program Mode

[Before Change]

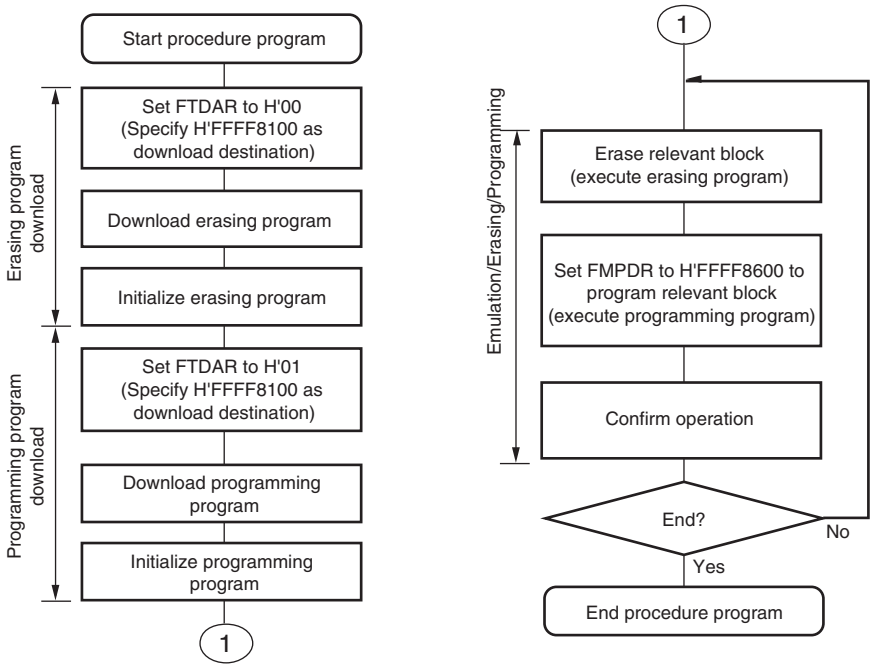
The frequency division ratio of an internal clock (Iϕ), a bus clock (Bϕ), and a peripheral clock (Pϕ) is specified as 4:4:4 (H'1000) by the frequency control register (FRQCR).

[After Change]

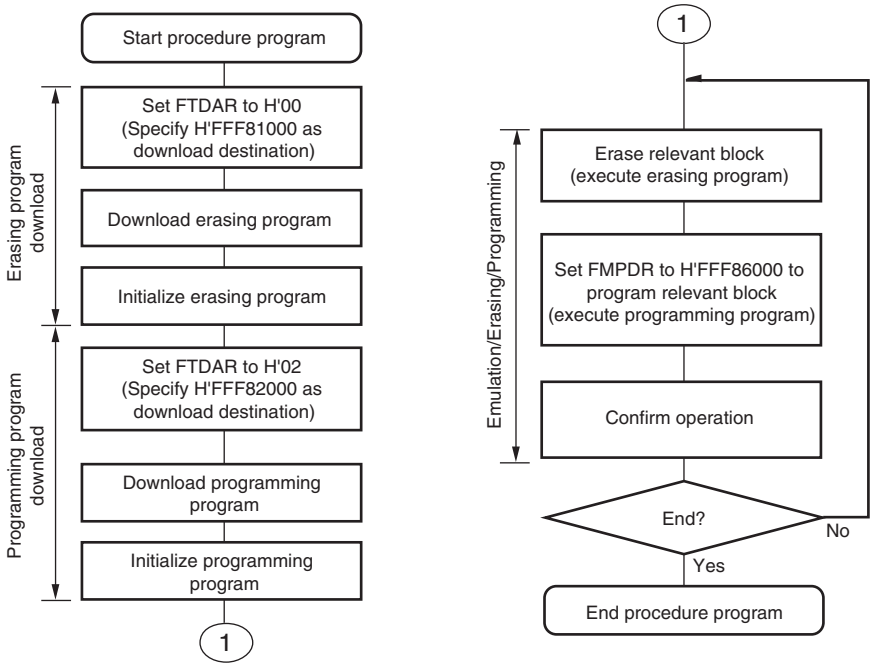
The frequency division ratio of an internal clock (Iϕ), a bus clock (Bϕ), and a peripheral clock (Pϕ) is specified as 4:4:4 by the frequency control register (FRQCR).

Page 932, (4) Erasing and Programming Procedure in User Program Mode, Figure 21.13 Sample Procedure of Repeating RAM Emulation, Erasing, and Programming (Overview)

[Before Change]



[After Change]



Page 933, (4) Erasing and Programming Procedure in User Program Mode, 2. Be sure to initialize both the erasing program and programming program.

[Before Change]

Initialization by setting the FPEFEQ and FUBRA parameters must be performed for both the erasing program and the programming program. Initialization must be executed for both entry addresses: (download start address for erasing program) + 32 bytes (H'FFF81020 in this example) and (download start address for programming program) + 32 bytes (H'FFF81820 in this example).

[After Change]

Initialization by setting the FPEFEQ and FUBRA parameters must be performed for both the erasing program and the programming program. Initialization must be executed for both entry addresses: (download start address for erasing program) + 32 bytes (H'FFF81020 in this example) and (download start address for programming program) + 32 bytes (H'FFF82020 in this example).

Page 945, 21.7.3 Other Notes, (2) User Branch Processing Intervals

[Before Change]

The intervals for executing the user branch processing differs in programming and erasing. The processing phase also differs. Table 21.10 lists the maximum and minimum intervals for initiating the user branch processing when the CPU clock frequency is 40 MHz.

Table 21.10 Initiation Intervals of User Branch Processing

Processing Name	Maximum	Minimum
Programming	TBD	TBD
Erasing	TBD	TBD

However, when operation is done with CPU clock of 40 MHz, maximum and minimum values of the time until first user branch processing are as shown in table 21.11.

Table 21.11 Initial User Branch Processing Time

Processing Name	Maximum	Minimum
Programming	TBD	TBD
Erasing	TBD	TBD

[After Change]

The intervals for executing the user branch processing differs in programming and erasing. The processing phase also differs. Table 21.10 lists the maximum intervals for initiating the user branch processing when the CPU clock frequency is 40 MHz.

Table 21.10 Initiation Intervals of User Branch Processing

Processing Name	Maximum Interval
Programming	Approximately 2 ms*
Erasing	Approximately 15 ms*

Note: * Reference value

However, when operation is done with CPU clock of 40 MHz, maximum values of the time until first user branch processing are as shown in table 21.11.

Table 21.11 Initial User Branch Processing Time

Processing Name	Maximum Interval
Programming	Approximately 2 ms*
Erasing	Approximately 15 ms*

Note: * Reference value

Page 946, 21.7.3 Other Notes, (7) The Operating Frequency in On-Board Programming Mode is added as follows:

[Addition]

(7) The Operating Frequency in On-Board Programming Mode

The frequency control register (FRQCR) should be set as follows in the erasing and programming procedure, described in section 21.5, On-Board Programming Mode.

- Specify (Iϕ: Bϕ: Pϕ) = (4:4:4) as the frequency division ratios of internal clocks.
  When the input clock is 10 MHz, (Iϕ: Bϕ: Pϕ) = (40 MHz:40 MHz:40 MHz)
  When the input clock is 8 MHz, (Iϕ: Bϕ: Pϕ) = (32 MHz:32 MHz:32 MHz)
- The following shows the frequency control register (FRQCR) values where (Iϕ: Bϕ: Pϕ) = (4:4:4) as the frequency division ratios of internal clocks.
  H'1000*
  H'1111*
  H'1333*

Note: * The CKOEN bit (bit 12) can be specified as either 0 or 1.

Page 946, 21.7.3 Other Notes, (8) Programming the User MAT in User Program Mode has been added as follows.

[Addition]

(8) Programming the User MAT in User Program Mode

This LSI does not allow transitions from single chip mode to user program mode. Therefore, in order to program the user MAT in user program mode, be sure to activate the LSI in MCU extension mode 2 rather than in single chip mode.

Page 959, (k) New Bit Rate Selection

[Before Change]

This should be the frequency in MHz to the second decimal place, multiplied by 100 (for example, if the frequency is 28.882 MHz, the values is truncated to the second decimal place and multiplied by 100, making 2888; so H'0B48 should be set in this field).

[After Change]

This should be the frequency in MHz to the second decimal place, multiplied by 100 (for example, if the frequency is 8.882 MHz, the value is truncated to the second decimal place and multiplied by 100, making 888; so H'0378 should be set in this field).

Page 977 to 978, 21.8.2 Areas for Storage of the Procedural Program and Data for Programming

[Before Change]

4. The flash memory is accessible until the start of programming or erasing, that is, until the result of downloading has been decided. When in a mode in which the external address space is not accessible, such as single-chip mode, the required procedure programs, interrupt vector table, interrupt processing routine, and user branch program should be transferred to on-chip RAM before programming/erasing of the flash memory starts.

[After Change]

4. The flash memory is accessible until the start of programming or erasing, that is, until the result of downloading has been decided.

Section 26. List of Registers

Pages 1035 to 1036, 26.2 Register Bits

[Before Change]

Module Name	Register Abbreviation	Bit 31/23/15/7	Bit 30/22/14/6	Bit 29/21/13/5	Bit 28/20/12/4	Bit 27/19/11/3	Bit 26/18/10/2	Bit 25/17/9/1	Bit 24/16/8/0
CPG	FRQCR				CKOEN				STC[1:0]
		—		IFC[2:0]		RNGS		PFC[2:0]	
	MCLKCR	MSSCS[1:0]		—	—	—	—	MSDIVS[1:0]	
	ACLKCR	ASSCS[1:0]		—	—	—	—	ASDIVS[1:0]	
INTC	ICR0	NMIL	—	—	—	—	—	—	NMIE
		—	—	—	—	—	—	—	—
	ICR1	IRQ71S	IRQ70S	IRQ61S	IRQ60S	IRQ51S	IRQ50S	IRQ41S	IRQ40S
		IRQ31S	IRQ30S	IRQ21S	IRQ20S	IRQ11S	IRQ10S	IRQ01S	IRQ00S
	IRQRR	—	—	—	—	—	—	—	—
		IRQ7F	IRQ6F	IRQ5F	IRQ4F	IRQ3F	IRQ2F	IRQ1F	IRQ0F
	IBCR	E15	E14	E13	E12	E11	E10	E9	E8
		E7	E6	E5	E4	E3	E2	E1	—
	IBNR	BE[1:0]		BOVE	—	—	—	—	—
		—	—	—	—	BN[3:0]			
	IPR01	—	—	—	—	—	—	—	—
		—	—	—	—	—	—	—	—
	IPR02	—	—	—	—	—	—	—	—
		—	—	—	—	—	—	—	—
	IPR05	—	—	—	—	—	—	—	—
		—	—	—	—	—	—	—	—
	IPR06	—	—	—	—	—	—	—	—
		—	—	—	—	—	—	—	—
	IPR07	—	—	—	—	—	—	—	—
		—	—	—	—	—	—	—	—
	IPR08	—	—	—	—	—	—	—	—
		—	—	—	—	—	—	—	—
	IPR09	—	—	—	—	—	—	—	—
		—	—	—	—	—	—	—	—

Module Name	Register Abbreviation	Bit 31/23/15/7	Bit 30/22/14/6	Bit 29/21/13/5	Bit 28/20/12/4	Bit 27/19/11/3	Bit 26/18/10/2	Bit 25/17/9/1	Bit 24/16/8/0
INTC	IPR10	—	—	—	—	—	—	—	—
		—	—	—	—	—	—	—	—
	IPR11	—	—	—	—	—	—	—	—
		—	—	—	—	—	—	—	—
	IPR12	—	—	—	—	—	—	—	—
		—	—	—	—	—	—	—	—
	IPR13	—	—	—	—	—	—	—	—
		—	—	—	—	—	—	—	—
	IPR14	—	—	—	—	—	—	—	—
		—	—	—	—	—	—	—	—
	IPR15	—	—	—	—	—	—	—	—
		—	—	—	—	—	—	—	—
UBC	BAR_0	BA0_31	BA0_30	BA0_29	BA0_28	BA0_27	BA0_26	BA0_25	BA0_24
		BA0_23	BA0_22	BA0_21	BA0_20	BA0_19	BA0_18	BA0_17	BA0_16
		BA0_15	BA0_14	BA0_13	BA0_12	BA0_11	BA0_10	BA0_9	BA0_8
		BA0_7	BA0_6	BA0_5	BA0_4	BA0_3	BA0_2	BA0_1	BA0_0
	BAMR_0	BAM0_31	BAM0_30	BAM0_29	BAM0_28	BAM0_27	BAM0_26	BAM0_25	BAM0_24
		BAM0_23	BAM0_22	BAM0_21	BAM0_20	BAM0_19	BAM0_18	BAM0_17	BAM0_16
		BAM0_15	BAM0_14	BAM0_13	BAM0_12	BAM0_11	BAM0_10	BAM0_9	BAM0_8
		BAM0_7	BAM0_6	BAM0_5	BAM0_4	BAM0_3	BAM0_2	BAM0_1	BAM0_0
	BBR_0	—	—	UBID0	—	—	—	CP0[1:0]	
		CD0[1:0]		ID0[1:0]		RW0[1:0]		SZ0[1:0]	
	BAR_1	BA1_31	BA1_30	BA1_29	BA1_28	BA1_27	BA1_26	BA1_25	BA1_24
		BA1_23	BA1_22	BA1_21	BA1_20	BA1_19	BA1_18	BA1_17	BA1_16
		BA1_15	BA1_14	BA1_13	BA1_12	BA1_11	BA1_10	BA1_9	BA1_8
		BA1_7	BA1_6	BA1_5	BA1_4	BA1_3	BA1_2	BA1_1	BA1_0
	BAMR_1	BAM1_31	BAM1_30	BAM1_29	BAM1_28	BAM1_27	BAM1_26	BAM1_25	BAM1_24
		BAM1_23	BAM1_22	BAM1_21	BAM1_20	BAM1_19	BAM1_18	BAM1_17	BAM1_16
		BAM1_15	BAM1_14	BAM1_13	BAM1_12	BAM1_11	BAM1_10	BAM1_9	BAM1_8
		BAM1_7	BAM1_6	BAM1_5	BAM1_4	BAM1_3	BAM1_2	BAM1_1	BAM1_0
	BBR_1	—	—	UBID1	—	—	—	CP1[1:0]	
		CD1[1:0]		ID1[1:0]		RW1[1:0]		SZ1[1:0]	
	BAR_2	BA2_31	BA2_30	BA2_29	BA2_28	BA2_27	BA2_26	BA2_25	BA2_24
		BA2_23	BA2_22	BA2_21	BA2_20	BA2_19	BA2_18	BA2_17	BA2_16
		BA2_15	BA2_14	BA2_13	BA2_12	BA2_11	BA2_10	BA2_9	BA2_8
		BA2_7	BA2_6	BA2_5	BA2_4	BA2_3	BA2_2	BA2_1	BA2_0
	BAMR_2	BAM2_31	BAM2_30	BAM2_29	BAM2_28	BAM2_27	BAM2_26	BAM2_25	BAM2_24
		BAM2_23	BAM2_22	BAM2_21	BAM2_20	BAM2_19	BAM2_18	BAM2_17	BAM2_16
		BAM2_15	BAM2_14	BAM2_13	BAM2_12	BAM2_11	BAM2_10	BAM2_9	BAM2_8
		BAM2_7	BAM2_6	BAM2_5	BAM2_4	BAM2_3	BAM2_2	BAM2_1	BAM2_0

[After Change]

Module Name	Register Abbreviation	Bit 31/23/15/7	Bit 30/22/14/6	Bit 29/21/13/5	Bit 28/20/12/4	Bit 27/19/11/3	Bit 26/18/10/2	Bit 25/17/9/1	Bit 24/16/8/0
CPG	FRQCR	—	—	—	CKOEN	—	—	STC[1:0]	
		—		IFC[2:0]		RNGS		PFC[2:0]	
	MCLKCR	MSSCS[1:0]		—	—	—	—	MSDIVS[1:0]	
	ACLKCR	ASSCS[1:0]		—	—	—	—	ASDIVS[1:0]	
INTC	ICR0	NMIL	—	—	—	—	—	—	NMIE
		—	—	—	—	—	—	—	—
	ICR1	IRQ71S	IRQ70S	IRQ61S	IRQ60S	IRQ51S	IRQ50S	IRQ41S	IRQ40S
		IRQ31S	IRQ30S	IRQ21S	IRQ20S	IRQ11S	IRQ10S	IRQ01S	IRQ00S
	IRQRR	—	—	—	—	—	—	—	—
		IRQ7F	IRQ6F	IRQ5F	IRQ4F	IRQ3F	IRQ2F	IRQ1F	IRQ0F
	IBCR	E15	E14	E13	E12	E11	E10	E9	E8
		E7	E6	E5	E4	E3	E2	E1	—
	IBNR	BE[1:0]		BOVE	—	—	—	—	—
		—	—	—	—	BN[3:0]			
	IPR01	IRQ0[3:0]				IRQ1[3:0]			
		IRQ2[3:0]				IRQ3[3:0]			
	IPR02	IRQ4[3:0]				IRQ5[3:0]			
		IRQ6[3:0]				IRQ7[3:0]			
	IPR05	—	—	—	—	—	—	—	—
		ADI[3:0]				—	—	—	—
	IPR06	DMAC0[3:0]				DMAC1[3:0]			
		DMAC2[3:0]				DMAC3[3:0]			
	IPR07	DMAC4[3:0]				DMAC5[3:0]			
		DMAC6[3:0]				DMAC7[3:0]			
	IPR08	CMT0[3:0]				CMT1[3:0]			
		BSC[3:0]				WDT[3:0]			
	IPR09	MTU0(TGI0A to TGI0D)[3:0]				MTU0(TCI0V, TGI0E, TGI0F)[3:0]			
		MTU1(TGI1A, TGI1B)[3:0]				MTU1(TCI1V, TCI1U)[3:0]			

Module Name	Register Abbreviation	Bit 31/23/15/7	Bit 30/22/14/6	Bit 29/21/13/5	Bit 28/20/12/4	Bit 27/19/11/3	Bit 26/18/10/2	Bit 25/17/9/1	Bit 24/16/8/0
INTC	IPR10	MTU2(TGI2A, TGI2B)[3:0]				MTU2(TCI2V, TCI2U)[3:0]			
		MTU3(TGI3A to TGI3D)[3:0]				MTU3(TCI3V)[3:0]			
	IPR11	MTU4(TGI4A to TGI4D)[3:0]				MTU4(TCI4V)[3:0]			
		MTU5(TGI5U, TGI5V, TGI5W)[3:0]				POE2(OEI1, OEI2)[3:0]			
	IPR12	MTU3S(TGI3A to TGI3D)[3:0]				MTU3S(TCI3V)[3:0]			
		MTU4S(TGI4A to TGI4D)[3:0]				MTU4S(TCI4V)[3:0]			
	IPR13	MTU5S(TGI5U, TGI5V, TGI5W)[3:0]				POE2(OEI3)[3:0]			
		IIC3[3:0]				—	—	—	—
	IPR14	SCIF0[3:0]				SCIF1[3:0]			
		SCIF2[3:0]				SCIF3[3:0]			
	IPR15	WAVEIF[3:0]				—	—	—	—
		—	—	—	—	—	—	—	—
UBC	BAR_0	BA0_31	BA0_30	BA0_29	BA0_28	BA0_27	BA0_26	BA0_25	BA0_24
		BA0_23	BA0_22	BA0_21	BA0_20	BA0_19	BA0_18	BA0_17	BA0_16
		BA0_15	BA0_14	BA0_13	BA0_12	BA0_11	BA0_10	BA0_9	BA0_8
		BA0_7	BA0_6	BA0_5	BA0_4	BA0_3	BA0_2	BA0_1	BA0_0
	BAMR_0	BAM0_31	BAM0_30	BAM0_29	BAM0_28	BAM0_27	BAM0_26	BAM0_25	BAM0_24
		BAM0_23	BAM0_22	BAM0_21	BAM0_20	BAM0_19	BAM0_18	BAM0_17	BAM0_16
		BAM0_15	BAM0_14	BAM0_13	BAM0_12	BAM0_11	BAM0_10	BAM0_9	BAM0_8
		BAM0_7	BAM0_6	BAM0_5	BAM0_4	BAM0_3	BAM0_2	BAM0_1	BAM0_0
	BBR_0	—	—	UBID0	—	—	—	CP0[1:0]	
		CD0[1:0]		ID0[1:0]		RW0[1:0]		SZ0[1:0]	
	BAR_1	BA1_31	BA1_30	BA1_29	BA1_28	BA1_27	BA1_26	BA1_25	BA1_24
		BA1_23	BA1_22	BA1_21	BA1_20	BA1_19	BA1_18	BA1_17	BA1_16
		BA1_15	BA1_14	BA1_13	BA1_12	BA1_11	BA1_10	BA1_9	BA1_8
		BA1_7	BA1_6	BA1_5	BA1_4	BA1_3	BA1_2	BA1_1	BA1_0
	BAMR_1	BAM1_31	BAM1_30	BAM1_29	BAM1_28	BAM1_27	BAM1_26	BAM1_25	BAM1_24
		BAM1_23	BAM1_22	BAM1_21	BAM1_20	BAM1_19	BAM1_18	BAM1_17	BAM1_16
		BAM1_15	BAM1_14	BAM1_13	BAM1_12	BAM1_11	BAM1_10	BAM1_9	BAM1_8
		BAM1_7	BAM1_6	BAM1_5	BAM1_4	BAM1_3	BAM1_2	BAM1_1	BAM1_0
	BBR_1	—	—	UBID1	—	—	—	CP1[1:0]	
		CD1[1:0]		ID1[1:0]		RW1[1:0]		SZ1[1:0]	
	BAR_2	BA2_31	BA2_30	BA2_29	BA2_28	BA2_27	BA2_26	BA2_25	BA2_24
		BA2_23	BA2_22	BA2_21	BA2_20	BA2_19	BA2_18	BA2_17	BA2_16
		BA2_15	BA2_14	BA2_13	BA2_12	BA2_11	BA2_10	BA2_9	BA2_8
		BA2_7	BA2_6	BA2_5	BA2_4	BA2_3	BA2_2	BA2_1	BA2_0
	BAMR_2	BAM2_31	BAM2_30	BAM2_29	BAM2_28	BAM2_27	BAM2_26	BAM2_25	BAM2_24
		BAM2_23	BAM2_22	BAM2_21	BAM2_20	BAM2_19	BAM2_18	BAM2_17	BAM2_16
		BAM2_15	BAM2_14	BAM2_13	BAM2_12	BAM2_11	BAM2_10	BAM2_9	BAM2_8
		BAM2_7	BAM2_6	BAM2_5	BAM2_4	BAM2_3	BAM2_2	BAM2_1	BAM2_0

Page 1059, 26.2 Register Bits, Module Name ADC

[Before Change]

Module Name	Register Abbreviation	Bit 31/23/15/7	Bit 30/22/14/6	Bit 29/21/13/5	Bit 28/20/12/4	Bit 27/19/11/3	Bit 26/18/10/2	Bit 25/17/9/1	Bit 24/16/8/0
ADC	ADCR	ADST	ADCS	ACE	ADIE	—	—	TRGE	EXTRG
	ADSR	—	—	—	—	—	—	—	ADF
	ADSTRGR	—	STR6	STR5	STR4	STR3	STR2	STR1	STR0
	ADANSR	ANS7	ANS6	ANS5	ANS4	ANS3	ANS2	ANS1	ANS0
	ADDR0	—	—	—	—			ADD[11:8]	
						ADD[7:0]			
	ADDR1	—	—	—	—			ADD[11:8]	
						ADD[7:0]			
	ADDR2	—	—	—	—			ADD[11:8]	
						ADD[7:0]			
	ADDR3	—	—	—	—			ADD[11:8]	
						ADD[7:0]			
	ADDR4	—	—	—	—			ADD[11:8]	
						ADD[7:0]			
	ADDR5	—	—	—	—			ADD[11:8]	
						ADD[7:0]			
	ADDR6	—	—	—	—			ADD[11:8]	
						ADD[7:0]			
	ADDR7	—	—	—	—			ADD[11:8]	
						ADD[7:0]			

[After Change]

Module Name	Register Abbreviation	Bit 31/23/15/7	Bit 30/22/14/6	Bit 29/21/13/5	Bit 28/20/12/4	Bit 27/19/11/3	Bit 26/18/10/2	Bit 25/17/9/1	Bit 24/16/8/0
ADC	ADCR	ADST	ADCS	ACE	ADIE	—	—	TRGE	EXTRG
	ADSR								ADF
	ADSTRGR	—	STR6	STR5	STR4	STR3	STR2	STR1	STR0
	ADANSR	ANS7	ANS6	ANS5	ANS4	ANS3	ANS2	ANS1	ANS0
	ADDR0	—	—	—	—			ADD0[11:8]	
						ADD0[7:0]			
	ADDR1	—	—	—	—			ADD1[11:8]	
						ADD1[7:0]			
	ADDR2	—	—	—	—			ADD2[11:8]	
						ADD2[7:0]			
	ADDR3	—	—	—	—			ADD3[11:8]	
						ADD3[7:0]			
	ADDR4	—	—	—	—			ADD4[11:8]	
						ADD4[7:0]			
	ADDR5	—	—	—	—			ADD5[11:8]	
						ADD5[7:0]			
	ADDR6	—	—	—	—			ADD6[11:8]	
						ADD6[7:0]			
	ADDR7	—	—	—	—			ADD7[11:8]	
						ADD7[7:0]			

Pages 1060 to 1062, 26.2 Register Bits, Module Name PFC

[Before Change]

Module Name	Register Abbreviation	Bit 31/23/15/7	Bit 30/22/14/6	Bit 29/21/13/5	Bit 28/20/12/4	Bit 27/19/11/3	Bit 26/18/10/2	Bit 25/17/9/1	Bit 24/16/8/0
PFC	PATLRH	—	—	—	—	—	—	PA25TLR	PA24TLR
		PA23TLR	PA22TLR	—	—	—	—	—	—
	PATLRL	—	—	—	—	—	—	—	—
		—	—	—	—	—	—	—	—
	PBTLRH	—	—	PB29TLR	PB28TLR	PB27TLR	PB26TLR	PB25TLR	PB24TLR
		PB23TLR	PB22TLR	PB21TLR	PB20TLR	PB19TLR	PB18TLR	PB17TLR	PB16TLR
	PBTLRL	—	—	—	—	—	—	—	—
		—	—	—	—	—	PB2TLR	PB1TLR	PB0TLR
	PDTLR	—	—	—	—	—	—	—	—
		PD7TLR	PD6TLR	PD5TLR	PD4TLR	PD3TLR	PB2TLR	PB1TLR	PB0TLR

[After Change]

Deleted

Pages 1068 to 1073, 26.3 Register States in Each Operating Mode, Module Name MTU2 and MTU2S

[Before Change]

Module Name	Register Abbreviation	Power-On Reset	Manual Reset	Software Standby	Module Standby	Sleep
MTU2	TCR_0	Initialized	Retained	Initialized	Initialized	Retained
	TMDR_0	Initialized	Retained	Initialized	Initialized	Retained
	TIORH_0	Initialized	Retained	Initialized	Initialized	Retained
	TIORL_0	Initialized	Retained	Initialized	Initialized	Retained
	TIER_0	Initialized	Retained	Initialized	Initialized	Retained
	TSR_0	Initialized	Retained	Initialized	Initialized	Retained
	TCNT_0	Initialized	Retained	Initialized	Initialized	Retained
	TGRA_0	Initialized	Retained	Initialized	Initialized	Retained
	TGRB_0	Initialized	Retained	Initialized	Initialized	Retained
	TGRC_0	Initialized	Retained	Initialized	Initialized	Retained
	TGRD_0	Initialized	Retained	Initialized	Initialized	Retained
	TGRE_0	Initialized	Retained	Initialized	Initialized	Retained
	TGRF_0	Initialized	Retained	Initialized	Initialized	Retained
	TIER2_0	Initialized	Retained	Initialized	Initialized	Retained
	TSR2_0	Initialized	Retained	Initialized	Initialized	Retained
	TBTM_0	Initialized	Retained	Initialized	Initialized	Retained
	TCR_1	Initialized	Retained	Initialized	Initialized	Retained
	TMDR_1	Initialized	Retained	Initialized	Initialized	Retained
	TIOR_1	Initialized	Retained	Initialized	Initialized	Retained
	TIER_1	Initialized	Retained	Initialized	Initialized	Retained
	TSR_1	Initialized	Retained	Initialized	Initialized	Retained
	TCNT_1	Initialized	Retained	Initialized	Initialized	Retained
	TGRA_1	Initialized	Retained	Initialized	Initialized	Retained
	TGRB_1	Initialized	Retained	Initialized	Initialized	Retained
	TICCR	Initialized	Retained	Initialized	Initialized	Retained
	TCR_2	Initialized	Retained	Initialized	Initialized	Retained
	TMDR_2	Initialized	Retained	Initialized	Initialized	Retained
	TIOR_2	Initialized	Retained	Initialized	Initialized	Retained
	TIER_2	Initialized	Retained	Initialized	Initialized	Retained
	TSR_2	Initialized	Retained	Initialized	Initialized	Retained
	TCNT_2	Initialized	Retained	Initialized	Initialized	Retained

Module Name	Register Abbreviation	Power-On Reset	Manual Reset	Software Standby	Module Standby	Sleep
MTU2	TGRA_2	Initialized	Retained	Initialized	Initialized	Retained
	TGRB_2	Initialized	Retained	Initialized	Initialized	Retained
	TCR_3	Initialized	Retained	Initialized	Initialized	Retained
	TMDR_3	Initialized	Retained	Initialized	Initialized	Retained
	TIORH_3	Initialized	Retained	Initialized	Initialized	Retained
	TIORL_3	Initialized	Retained	Initialized	Initialized	Retained
	TIER_3	Initialized	Retained	Initialized	Initialized	Retained
	TSR_3	Initialized	Retained	Initialized	Initialized	Retained
	TCNT_3	Initialized	Retained	Initialized	Initialized	Retained
	TGRA_3	Initialized	Retained	Initialized	Initialized	Retained
	TGRB_3	Initialized	Retained	Initialized	Initialized	Retained
	TGRC_3	Initialized	Retained	Initialized	Initialized	Retained
	TGRD_3	Initialized	Retained	Initialized	Initialized	Retained
	TBTM_3	Initialized	Retained	Initialized	Initialized	Retained
	TCR_4	Initialized	Retained	Initialized	Initialized	Retained
	TMDR_4	Initialized	Retained	Initialized	Initialized	Retained
	TIORH_4	Initialized	Retained	Initialized	Initialized	Retained
	TIORL_4	Initialized	Retained	Initialized	Initialized	Retained
	TIER_4	Initialized	Retained	Initialized	Initialized	Retained
	TSR_4	Initialized	Retained	Initialized	Initialized	Retained
	TCNT_4	Initialized	Retained	Initialized	Initialized	Retained
	TGRA_4	Initialized	Retained	Initialized	Initialized	Retained
	TGRB_4	Initialized	Retained	Initialized	Initialized	Retained
	TGRC_4	Initialized	Retained	Initialized	Initialized	Retained
	TGRD_4	Initialized	Retained	Initialized	Initialized	Retained
	TBTM_4	Initialized	Retained	Initialized	Initialized	Retained
	TADCR	Initialized	Retained	Initialized	Initialized	Retained
	TADCORA_4	Initialized	Retained	Initialized	Initialized	Retained
	TADCORB_4	Initialized	Retained	Initialized	Initialized	Retained
	TADCOBRA_4	Initialized	Retained	Initialized	Initialized	Retained
	TADCOBRB_4	Initialized	Retained	Initialized	Initialized	Retained

Module Name	Register Abbreviation	Power-On Reset	Manual Reset	Software Standby	Module Standby	Sleep
MTU2	TCRU_5	Initialized	Retained	Initialized	Initialized	Retained
	TCRV_5	Initialized	Retained	Initialized	Initialized	Retained
	TCRW_5	Initialized	Retained	Initialized	Initialized	Retained
	TIORU_5	Initialized	Retained	Initialized	Initialized	Retained
	TIORV_5	Initialized	Retained	Initialized	Initialized	Retained
	TIORW_5	Initialized	Retained	Initialized	Initialized	Retained
	TIER_5	Initialized	Retained	Initialized	Initialized	Retained
	TSR_5	Initialized	Retained	Initialized	Initialized	Retained
	TSTR_5	Initialized	Retained	Initialized	Initialized	Retained
	TCNTU_5	Initialized	Retained	Initialized	Initialized	Retained
	TCNTV_5	Initialized	Retained	Initialized	Initialized	Retained
	TCNTW_5	Initialized	Retained	Initialized	Initialized	Retained
	TGRU_5	Initialized	Retained	Initialized	Initialized	Retained
	TGRV_5	Initialized	Retained	Initialized	Initialized	Retained
	TGRW_5	Initialized	Retained	Initialized	Initialized	Retained
	TCNTCMPCLR	Initialized	Retained	Initialized	Initialized	Retained
	TSTR	Initialized	Retained	Initialized	Initialized	Retained
	TSYR	Initialized	Retained	Initialized	Initialized	Retained
	TCSYSTR	Initialized	Retained	Initialized	Initialized	Retained
	TRWER	Initialized	Retained	Initialized	Initialized	Retained
	TOER	Initialized	Retained	Initialized	Initialized	Retained
	TOCR1	Initialized	Retained	Initialized	Initialized	Retained
	TOCR2	Initialized	Retained	Initialized	Initialized	Retained
	TGCR	Initialized	Retained	Initialized	Initialized	Retained
	TCDR	Initialized	Retained	Initialized	Initialized	Retained
	TDDR	Initialized	Retained	Initialized	Initialized	Retained
	TCNTS	Initialized	Retained	Initialized	Initialized	Retained
	TCBR	Initialized	Retained	Initialized	Initialized	Retained
	TITCR	Initialized	Retained	Initialized	Initialized	Retained
	TITCNT	Initialized	Retained	Initialized	Initialized	Retained
	TBTER	Initialized	Retained	Initialized	Initialized	Retained

Module Name	Register Abbreviation	Power-On Reset	Manual Reset	Software Standby	Module Standby	Sleep
MTU2	TDER	Initialized	Retained	Initialized	Initialized	Retained
	TSYCR	Initialized	Retained	Initialized	Initialized	Retained
	TWCR	Initialized	Retained	Initialized	Initialized	Retained
	TOLBR	Initialized	Retained	Initialized	Initialized	Retained
MTU2S	TCR_3S	Initialized	Retained	Initialized	Initialized	Retained
	TMDR_3S	Initialized	Retained	Initialized	Initialized	Retained
	TIORH_3S	Initialized	Retained	Initialized	Initialized	Retained
	TIORL_3S	Initialized	Retained	Initialized	Initialized	Retained
	TIER_3S	Initialized	Retained	Initialized	Initialized	Retained
	TSR_3S	Initialized	Retained	Initialized	Initialized	Retained
	TCNT_3S	Initialized	Retained	Initialized	Initialized	Retained
	TGRA_3S	Initialized	Retained	Initialized	Initialized	Retained
	TGRB_3S	Initialized	Retained	Initialized	Initialized	Retained
	TGRC_3S	Initialized	Retained	Initialized	Initialized	Retained
	TGRD_3S	Initialized	Retained	Initialized	Initialized	Retained
	TBTM_3S	Initialized	Retained	Initialized	Initialized	Retained
	TCR_4S	Initialized	Retained	Initialized	Initialized	Retained
	TMDR_4S	Initialized	Retained	Initialized	Initialized	Retained
	TIORH_4S	Initialized	Retained	Initialized	Initialized	Retained
	TIORL_4S	Initialized	Retained	Initialized	Initialized	Retained
	TIER_4S	Initialized	Retained	Initialized	Initialized	Retained
	TSR_4S	Initialized	Retained	Initialized	Initialized	Retained
	TCNT_4S	Initialized	Retained	Initialized	Initialized	Retained
	TGRA_4S	Initialized	Retained	Initialized	Initialized	Retained
	TGRB_4S	Initialized	Retained	Initialized	Initialized	Retained
	TGRC_4S	Initialized	Retained	Initialized	Initialized	Retained
	TGRD_4S	Initialized	Retained	Initialized	Initialized	Retained
	TBTM_4S	Initialized	Retained	Initialized	Initialized	Retained
	TADCRS	Initialized	Retained	Initialized	Initialized	Retained
	TADCORA_4S	Initialized	Retained	Initialized	Initialized	Retained
	TADCORB_4S	Initialized	Retained	Initialized	Initialized	Retained

Module Name	Register Abbreviation	Power-On Reset	Manual Reset	Software Standby	Module Standby	Sleep
MTU2S	TADCOBRA_4S	Initialized	Retained	Initialized	Initialized	Retained
	TADCOBRB_4S	Initialized	Retained	Initialized	Initialized	Retained
	TCRU_5S	Initialized	Retained	Initialized	Initialized	Retained
	TCRV_5S	Initialized	Retained	Initialized	Initialized	Retained
	TCRW_5S	Initialized	Retained	Initialized	Initialized	Retained
	TIORU_5S	Initialized	Retained	Initialized	Initialized	Retained
	TIORV_5S	Initialized	Retained	Initialized	Initialized	Retained
	TIORW_5S	Initialized	Retained	Initialized	Initialized	Retained
	TIER_5S	Initialized	Retained	Initialized	Initialized	Retained
	TSR_5S	Initialized	Retained	Initialized	Initialized	Retained
	TSTR_5S	Initialized	Retained	Initialized	Initialized	Retained
	TCNTU_5S	Initialized	Retained	Initialized	Initialized	Retained
	TCNTV_5S	Initialized	Retained	Initialized	Initialized	Retained
	TCNTW_5S	Initialized	Retained	Initialized	Initialized	Retained
	TGRU_5S	Initialized	Retained	Initialized	Initialized	Retained
	TGRV_5S	Initialized	Retained	Initialized	Initialized	Retained
	TGRW_5S	Initialized	Retained	Initialized	Initialized	Retained
	TCNTCMPCLRS	Initialized	Retained	Initialized	Initialized	Retained
	TSTRS	Initialized	Retained	Initialized	Initialized	Retained
	TSYRS	Initialized	Retained	Initialized	Initialized	Retained
	TRWERS	Initialized	Retained	Initialized	Initialized	Retained
	TOERS	Initialized	Retained	Initialized	Initialized	Retained
	TOCR1S	Initialized	Retained	Initialized	Initialized	Retained
	TOCR2S	Initialized	Retained	Initialized	Initialized	Retained
	TGCRS	Initialized	Retained	Initialized	Initialized	Retained
	TCDRS	Initialized	Retained	Initialized	Initialized	Retained
	TDDRS	Initialized	Retained	Initialized	Initialized	Retained
	TCNTSS	Initialized	Retained	Initialized	Initialized	Retained
	TCBRS	Initialized	Retained	Initialized	Initialized	Retained
	TITCRS	Initialized	Retained	Initialized	Initialized	Retained
	TITCNTS	Initialized	Retained	Initialized	Initialized	Retained
	TBTERS	Initialized	Retained	Initialized	Initialized	Retained
	TDERS	Initialized	Retained	Initialized	Initialized	Retained
	TSYCRS	Initialized	Retained	Initialized	Initialized	Retained
	TWCRS	Initialized	Retained	Initialized	Initialized	Retained
	TOLBRS	Initialized	Retained	Initialized	Initialized	Retained

[After Change]

Module Name	Register Abbreviation	Power-On Reset	Manual Reset	Software Standby	Module Standby	Sleep
MTU2	TCR_0	Initialized	Retained	Retained	Initialized	Retained
	TMDR_0	Initialized	Retained	Retained	Initialized	Retained
	TIORH_0	Initialized	Retained	Retained	Initialized	Retained
	TIORL_0	Initialized	Retained	Retained	Initialized	Retained
	TIER_0	Initialized	Retained	Retained	Initialized	Retained
	TSR_0	Initialized	Retained	Retained	Initialized	Retained
	TCNT_0	Initialized	Retained	Retained	Initialized	Retained
	TGRA_0	Initialized	Retained	Retained	Initialized	Retained
	TGRB_0	Initialized	Retained	Retained	Initialized	Retained
	TGRC_0	Initialized	Retained	Retained	Initialized	Retained
	TGRD_0	Initialized	Retained	Retained	Initialized	Retained
	TGRE_0	Initialized	Retained	Retained	Initialized	Retained
	TGRF_0	Initialized	Retained	Retained	Initialized	Retained
	TIER2_0	Initialized	Retained	Retained	Initialized	Retained
	TSR2_0	Initialized	Retained	Retained	Initialized	Retained
	TBTM_0	Initialized	Retained	Retained	Initialized	Retained
	TCR_1	Initialized	Retained	Retained	Initialized	Retained
	TMDR_1	Initialized	Retained	Retained	Initialized	Retained
	TIOR_1	Initialized	Retained	Retained	Initialized	Retained
	TIER_1	Initialized	Retained	Retained	Initialized	Retained
	TSR_1	Initialized	Retained	Retained	Initialized	Retained
	TCNT_1	Initialized	Retained	Retained	Initialized	Retained
	TGRA_1	Initialized	Retained	Retained	Initialized	Retained
	TGRB_1	Initialized	Retained	Retained	Initialized	Retained
	TICCR	Initialized	Retained	Retained	Initialized	Retained
	TCR_2	Initialized	Retained	Retained	Initialized	Retained
	TMDR_2	Initialized	Retained	Retained	Initialized	Retained
	TIOR_2	Initialized	Retained	Retained	Initialized	Retained
	TIER_2	Initialized	Retained	Retained	Initialized	Retained
	TSR_2	Initialized	Retained	Retained	Initialized	Retained
	TCNT_2	Initialized	Retained	Retained	Initialized	Retained

Module Name	Register Abbreviation	Power-On Reset	Manual Reset	Software Standby	Module Standby	Sleep
MTU2	TGRA_2	Initialized	Retained	Retained	Initialized	Retained
	TGRB_2	Initialized	Retained	Retained	Initialized	Retained
	TCR_3	Initialized	Retained	Retained	Initialized	Retained
	TMDR_3	Initialized	Retained	Retained	Initialized	Retained
	TIORH_3	Initialized	Retained	Retained	Initialized	Retained
	TIORL_3	Initialized	Retained	Retained	Initialized	Retained
	TIER_3	Initialized	Retained	Retained	Initialized	Retained
	TSR_3	Initialized	Retained	Retained	Initialized	Retained
	TCNT_3	Initialized	Retained	Retained	Initialized	Retained
	TGRA_3	Initialized	Retained	Retained	Initialized	Retained
	TGRB_3	Initialized	Retained	Retained	Initialized	Retained
	TGRC_3	Initialized	Retained	Retained	Initialized	Retained
	TGRD_3	Initialized	Retained	Retained	Initialized	Retained
	TBTM_3	Initialized	Retained	Retained	Initialized	Retained
	TCR_4	Initialized	Retained	Retained	Initialized	Retained
	TMDR_4	Initialized	Retained	Retained	Initialized	Retained
	TIORH_4	Initialized	Retained	Retained	Initialized	Retained
	TIORL_4	Initialized	Retained	Retained	Initialized	Retained
	TIER_4	Initialized	Retained	Retained	Initialized	Retained
	TSR_4	Initialized	Retained	Retained	Initialized	Retained
	TCNT_4	Initialized	Retained	Retained	Initialized	Retained
	TGRA_4	Initialized	Retained	Retained	Initialized	Retained
	TGRB_4	Initialized	Retained	Retained	Initialized	Retained
	TGRC_4	Initialized	Retained	Retained	Initialized	Retained
	TGRD_4	Initialized	Retained	Retained	Initialized	Retained
	TBTM_4	Initialized	Retained	Retained	Initialized	Retained
	TADCR	Initialized	Retained	Retained	Initialized	Retained
	TADCORA_4	Initialized	Retained	Retained	Initialized	Retained
	TADCORB_4	Initialized	Retained	Retained	Initialized	Retained
	TADCOBRA_4	Initialized	Retained	Retained	Initialized	Retained
	TADCOBRB_4	Initialized	Retained	Retained	Initialized	Retained

Module Name	Register Abbreviation	Power-On Reset	Manual Reset	Software Standby	Module Standby	Sleep
MTU2	TCRU_5	Initialized	Retained	Retained	Initialized	Retained
	TCRV_5	Initialized	Retained	Retained	Initialized	Retained
	TCRW_5	Initialized	Retained	Retained	Initialized	Retained
	TIORU_5	Initialized	Retained	Retained	Initialized	Retained
	TIORV_5	Initialized	Retained	Retained	Initialized	Retained
	TIORW_5	Initialized	Retained	Retained	Initialized	Retained
	TIER_5	Initialized	Retained	Retained	Initialized	Retained
	TSR_5	Initialized	Retained	Retained	Initialized	Retained
	TSTR_5	Initialized	Retained	Retained	Initialized	Retained
	TCNTU_5	Initialized	Retained	Retained	Initialized	Retained
	TCNTV_5	Initialized	Retained	Retained	Initialized	Retained
	TCNTW_5	Initialized	Retained	Retained	Initialized	Retained
	TGRU_5	Initialized	Retained	Retained	Initialized	Retained
	TGRV_5	Initialized	Retained	Retained	Initialized	Retained
	TGRW_5	Initialized	Retained	Retained	Initialized	Retained
	TCNTCMPCLR	Initialized	Retained	Retained	Initialized	Retained
	TSTR	Initialized	Retained	Retained	Initialized	Retained
	TSYR	Initialized	Retained	Retained	Initialized	Retained
	TCSYSTR	Initialized	Retained	Retained	Initialized	Retained
	TRWER	Initialized	Retained	Retained	Initialized	Retained
	TOER	Initialized	Retained	Retained	Initialized	Retained
	TOCR1	Initialized	Retained	Retained	Initialized	Retained
	TOCR2	Initialized	Retained	Retained	Initialized	Retained
	TGCR	Initialized	Retained	Retained	Initialized	Retained
	TCDR	Initialized	Retained	Retained	Initialized	Retained
	TDDR	Initialized	Retained	Retained	Initialized	Retained
	TCNTS	Initialized	Retained	Retained	Initialized	Retained
	TCBR	Initialized	Retained	Retained	Initialized	Retained
	TITCR	Initialized	Retained	Retained	Initialized	Retained
	TITCNT	Initialized	Retained	Retained	Initialized	Retained
	TBTER	Initialized	Retained	Retained	Initialized	Retained

Module Name	Register Abbreviation	Power-On Reset	Manual Reset	Software Standby	Module Standby	Sleep
MTU2	TDER	Initialized	Retained	Retained	Initialized	Retained
	TSYCR	Initialized	Retained	Retained	Initialized	Retained
	TWCR	Initialized	Retained	Retained	Initialized	Retained
	TOLBR	Initialized	Retained	Retained	Initialized	Retained
MTU2S	TCR_3S	Initialized	Retained	Retained	Initialized	Retained
	TMDR_3S	Initialized	Retained	Retained	Initialized	Retained
	TIORH_3S	Initialized	Retained	Retained	Initialized	Retained
	TIORL_3S	Initialized	Retained	Retained	Initialized	Retained
	TIER_3S	Initialized	Retained	Retained	Initialized	Retained
	TSR_3S	Initialized	Retained	Retained	Initialized	Retained
	TCNT_3S	Initialized	Retained	Retained	Initialized	Retained
	TGRA_3S	Initialized	Retained	Retained	Initialized	Retained
	TGRB_3S	Initialized	Retained	Retained	Initialized	Retained
	TGRC_3S	Initialized	Retained	Retained	Initialized	Retained
	TGRD_3S	Initialized	Retained	Retained	Initialized	Retained
	TBTM_3S	Initialized	Retained	Retained	Initialized	Retained
	TCR_4S	Initialized	Retained	Retained	Initialized	Retained
	TMDR_4S	Initialized	Retained	Retained	Initialized	Retained
	TIORH_4S	Initialized	Retained	Retained	Initialized	Retained
	TIORL_4S	Initialized	Retained	Retained	Initialized	Retained
	TIER_4S	Initialized	Retained	Retained	Initialized	Retained
	TSR_4S	Initialized	Retained	Retained	Initialized	Retained
	TCNT_4S	Initialized	Retained	Retained	Initialized	Retained
	TGRA_4S	Initialized	Retained	Retained	Initialized	Retained
	TGRB_4S	Initialized	Retained	Retained	Initialized	Retained
	TGRC_4S	Initialized	Retained	Retained	Initialized	Retained
	TGRD_4S	Initialized	Retained	Retained	Initialized	Retained
	TBTM_4S	Initialized	Retained	Retained	Initialized	Retained
	TADCRS	Initialized	Retained	Retained	Initialized	Retained
	TADCORA_4S	Initialized	Retained	Retained	Initialized	Retained
	TADCORB_4S	Initialized	Retained	Retained	Initialized	Retained

Module Name	Register Abbreviation	Power-On Reset	Manual Reset	Software Standby	Module Standby	Sleep
MTU2S	TADCOBRA_4S	Initialized	Retained	Retained	Initialized	Retained
	TADCOBRB_4S	Initialized	Retained	Retained	Initialized	Retained
	TCRU_5S	Initialized	Retained	Retained	Initialized	Retained
	TCRV_5S	Initialized	Retained	Retained	Initialized	Retained
	TCRW_5S	Initialized	Retained	Retained	Initialized	Retained
	TIORU_5S	Initialized	Retained	Retained	Initialized	Retained
	TIORV_5S	Initialized	Retained	Retained	Initialized	Retained
	TIORW_5S	Initialized	Retained	Retained	Initialized	Retained
	TIER_5S	Initialized	Retained	Retained	Initialized	Retained
	TSR_5S	Initialized	Retained	Retained	Initialized	Retained
	TSTR_5S	Initialized	Retained	Retained	Initialized	Retained
	TCNTU_5S	Initialized	Retained	Retained	Initialized	Retained
	TCNTV_5S	Initialized	Retained	Retained	Initialized	Retained
	TCNTW_5S	Initialized	Retained	Retained	Initialized	Retained
	TGRU_5S	Initialized	Retained	Retained	Initialized	Retained
	TGRV_5S	Initialized	Retained	Retained	Initialized	Retained
	TGRW_5S	Initialized	Retained	Retained	Initialized	Retained
	TCNTCMPCLRS	Initialized	Retained	Retained	Initialized	Retained
	TSTRS	Initialized	Retained	Retained	Initialized	Retained
	TSYRS	Initialized	Retained	Retained	Initialized	Retained
	TRWERS	Initialized	Retained	Retained	Initialized	Retained
	TOERS	Initialized	Retained	Retained	Initialized	Retained
	TOCR1S	Initialized	Retained	Retained	Initialized	Retained
	TOCR2S	Initialized	Retained	Retained	Initialized	Retained
	TGCRS	Initialized	Retained	Retained	Initialized	Retained
	TCDRS	Initialized	Retained	Retained	Initialized	Retained
	TDDRS	Initialized	Retained	Retained	Initialized	Retained
	TCNTSS	Initialized	Retained	Retained	Initialized	Retained
	TCBRS	Initialized	Retained	Retained	Initialized	Retained
	TITCRS	Initialized	Retained	Retained	Initialized	Retained
	TITCNTS	Initialized	Retained	Retained	Initialized	Retained
	TBTERS	Initialized	Retained	Retained	Initialized	Retained
	TDERS	Initialized	Retained	Retained	Initialized	Retained
	TSYCRS	Initialized	Retained	Retained	Initialized	Retained
	TWCRS	Initialized	Retained	Retained	Initialized	Retained
	TOLBRS	Initialized	Retained	Retained	Initialized	Retained

Page 1076, 26.3 Register States in Each Operating Mode, Module Name PFC is deleted as follows:

[Before Change]

Module Name	Register Abbreviation	Power-On Reset	Manual Reset	Software Standby	Module Standby	Sleep
PFC	PATLRH	Initialized	Retained	Retained	—	Retained
	PATLRL	Initialized	Retained	Retained	—	Retained
	PBTLRH	Initialized	Retained	Retained	—	Retained
	PBTLRL	Initialized	Retained	Retained	—	Retained
	PDTLR	Initialized	Retained	Retained	—	Retained

[After Change]

Deleted

Section 27. Electrical Characteristics

Page 1080, 27.2 Power-on/Power-off Sequence is revised as follows:

[Before Change]

Note: The table shown above is recommended values, so they represent guidelines rather than strict requirements. VccQ ≥ Vcc = PLLVcc is recommended. Either VccQ, Vcc, or PLLVcc power supply can be turned on or off first, though, an undefined period appears until the power that is turned on later rises to the Min. voltage or after the power that is turned off earlier passes the Min. voltage. During these periods, pin or internal states become undefined. To avoid an increase in the current consumption during the undefined period at power-on, it is recommended that VccQ, Vcc, and PLLVcc be turned on simultaneously.

AV_{CC} = AVREF > V_{CC} = $PLLV_{CC}$ is recommended. Either AV_{CC} or $V_{CC}Q$ power supply can be turned on or off first. However, note that the equation AV_{CC} ±0.3 V = AVREF should always be true. Using the LSI under the following conditions may result in decreased reliability or permanent damage to the LSI.

AVREF > AV_{CC} + 0.3 V or AVREFVSS < AV_{SS} – 0.3

[After Change]

VccQ ≥ Vcc = PLLVcc is recommended. Either VccQ, Vcc, or PLLVcc power supply can be turned on or off first, though, an undefined period appears until Vcc rises to the Min. voltage or after Vcc passes the Min. voltage. During these periods, pin or internal states become undefined. Design the system so that such undefined states do not cause a system malfunction. To avoid an increase in the current consumption during the undefined period at power-on, it is recommended that VccQ, Vcc, and PLLVcc be turned on simultaneously. This undefined period can be eliminated by turning on the power supplies in the order shown in figure 27.2.

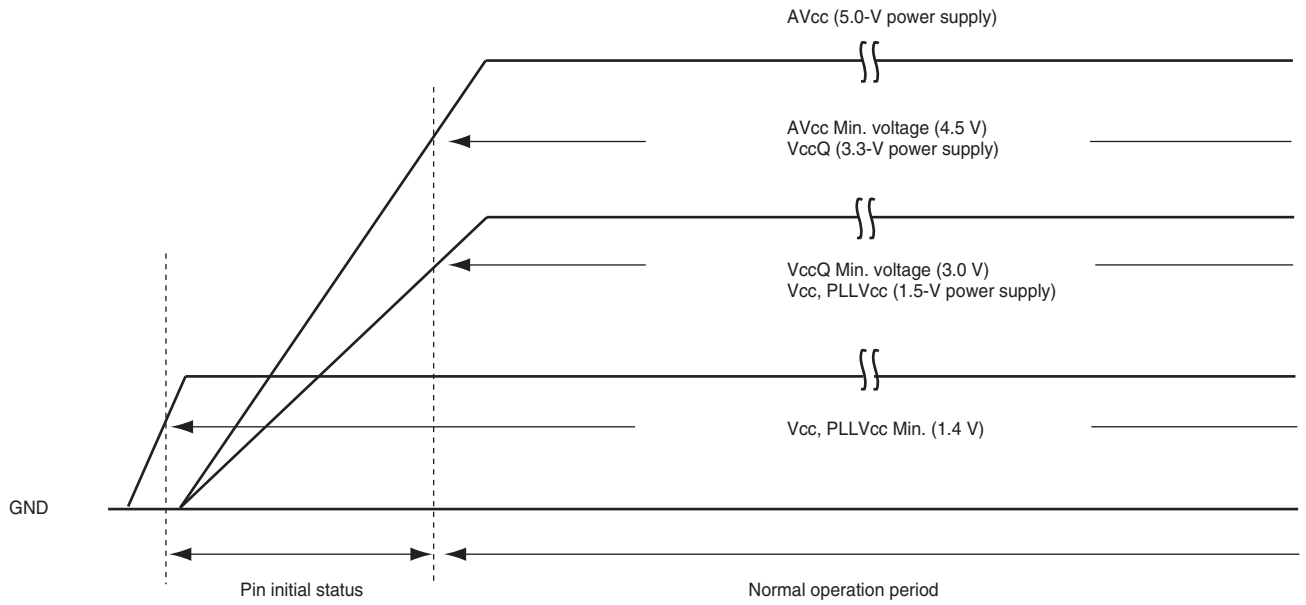


Figure 27.2 Power-On Sequence

Notes: 1. AV_{CC} = AVREF > V_{CC} = $PLLV_{CC}$ is recommended. Either AV_{CC} or $V_{CC}Q$ power supply can be turned on or off first. However, note that the equation AV_{CC} ±0.3 V = AVREF should always be true. Using the LSI under the following conditions may result in decreased reliability or permanent damage to the LSI.

AVREF > AV_{CC} ± 0.3 V

2. To prevent the pin and internal states from being undefined, VccQ and AVcc should be kept GND voltage level (0 V) and they should not be placed in floating state until Vcc reaches the Min. voltage. In addition, the RES pin should be input low to place power-on reset state. In this case, care must be taken for the power consumption increase caused by sink current because each pin is placed in low-impedance state until VccQ reaches the Min. voltage.

Page 1081, 27.3 DC Characteristics, Table 27.3 DC Characteristics (1) [Common Items]

[Before Change]

Item		Symbol	Min.	Typ.	Max.	Unit	Test Conditions
Power supply voltage		$V_{CC}Q$	3.0	3.3	3.6	V	
		V_{CC} $PLLV_{CC}$	1.4	1.5	1.6	V	
Analog power supply voltage		AV_{CC}	4.5	5.0	5.5	V	
Current consumption*1	Normal operation	I_{CC}	—	200	400	mA	V_{CC} = 1.5 V Iϕ = 160 MHz Bϕ = 40 MHz Pϕ = 40 MHz
	Software standby mode	I_{stby}	—	5	60	mA	Ta = 25°C $V_{CC}Q$ = 3.3 V V_{CC} = 1.5 V Bϕ = 40 MHz Pϕ = 40 MHz
		PI_{stby}	—	1	5	mA	
	Sleep mode	I_{sleep}	—	120	170	mA	
Input leakage current	All input pins (except PF0, PF1)	$\|I_{in}\|$	—	—	1	µA	V_{in} = 0.5 to $V_{CC}Q$ – 0.5 V
	PF0, PF1		—	—	10	µA	
Three-state leakage current	Input/output pins, all output pins (off state)	$\|I_{STI}\|$	—	—	1	µA	Vin = 0.5 to $V_{CC}Q$ – 0.5 V
Input capacitance	All pins	C_{in}	—	—	20	pF	
Analog power supply current	During A/D or D/A conversion	AI_{CC}	—	5	10	mA	Including AVREF
	Waiting for A/D or D/A conversion		—	1	2	mA	
	Standby mode		—	—	20	µA	

[After Change]

Item		Symbol	Min.	Typ.	Max.	Unit	Test Conditions
Power supply voltage		$V_{CC}Q$	3.0	3.3	3.6	V	
		V_{CC} $PLLV_{CC}$	1.4	1.5	1.6	V	
Analog power supply voltage		AV_{CC}	4.5	5.0	5.5	V	
Current consumption*1	Normal operation	I_{CC}	—	200	310	mA	V_{CC} = 1.5 V Iϕ = 160 MHz Bϕ = 40 MHz Pϕ = 40 MHz
	Software standby mode	I_{stby}	—	5	60	mA	Ta = 25°C $V_{CC}Q$ = 3.3 V V_{CC} = 1.5 V Bϕ = 40 MHz Pϕ = 40 MHz
		PI_{stby}	—	0.1	1	mA	
	Sleep mode	I_{sleep}	—	60	100	mA	
Input leakage current	All input pins (except PF0, PF1)	$\|I_{in}\|$	—	—	1	µA	V_{in} = 0.5 to $V_{CC}Q$ – 0.5 V
	PF0, PF1		—	—	1	µA	
Three-state leakage current	Input/output pins, all output pins (off state)	$\|I_{STI}\|$	—	—	1	µA	Vin = 0.5 to $V_{CC}Q$ – 0.5 V
Input capacitance	All pins	C_{in}	—	—	10	pF	
Analog power supply current	During A/D or D/A conversion	AI_{CC}	—	5	10	mA	Including AVREF
	Waiting for A/D or D/A conversion		—	1	2	mA	
	Standby mode		—	—	20	µA	

Page 1081, 27.3 DC Characteristics, Table 27.3 DC Characteristics (1) [Common Items], Caution

[Before Change]

When the A/D converter or D/A converter is not in use, the AV_{CC}, AV_{SS}, AVREF, and AVREFVSS pins should not be open.

[After Change]

When neither the A/D converter nor the D/A converter is in use, set $V_{CC} \leq AV_{CC} \leq 5.0\ V \pm 0.5\ V$ and $AV_{SS} = V_{SS}$, and do not leave the AV_{CC}, AV_{SS}, AVREF, and $AVREFV_{SS}$ pins open.

Page 1083, 27.3 DC Characteristics, Table 27.3 DC Characteristics (2) [Except for I^2C -Related Pins]

[Before Change]

Item		Symbol	Min.	Typ.	Max.	Unit	Test Conditions
Output high voltage	All output pins	V_{OH}	$V_{CC}Q - 0.5$	—	—	V	$I_{OH} = -200\ \mu A$
Output low voltage	PB21 to PB18, PB13 to PB10, PB7 to 4	V_{OL}	—	—	0.9	V	$I_{OL} = 15\ mA$
	All output pins except for above pins		—	—	0.5	V	$I_{OL} = 2\ mA$

[After Change]

Item		Symbol	Min.	Typ.	Max.	Unit	Test Conditions
Output high voltage	TIOC3B, TIOC3D TIOC4A to TIOC4D TIOC3BS, TIOC3DS TIOC4AS to TIOC4DS	V_{OH}	$V_{CC}Q$ – 0.8	—	—	V	I_{OH} = –5 mA
	All output pins except for above pins		$V_{CC}Q$ – 0.5	—	—	V	I_{OH} = –200 µA
Output low voltage	TIOC3B, TIOC3D TIOC4A to TIOC4D TIOC3BS, TIOC3DS TIOC4AS to TIOC4DS	V_{OL}	—	—	0.9	V	I_{OL} = 15 mA
	All output pins except for above pins		—	—	0.4	V	I_{OL} = 2 mA

Page 1084, 27.3 DC Characteristics, Table 27.3 DC Characteristics (3) [I^2C-Related Pins*]

[Before Change]

Item	Symbol	Min.	Typ.	Max.	Unit	Test Conditions
Input high voltage	V_{IH}	$V_{CC}Q \times 0.7$	—	$V_{CC}Q$ + 0.5	V	
Input low voltage	V_{IL}	–0.5	—	$V_{CC}Q \times 0.3$	V	
Schmitt trigger input characteristics	$V_{IH} – V_{IL}$	0.4	—	—	V	
Output low voltage	V_{OL}	—	—	0.4	V	I_{OL} = 3.0 mA

[After Change]

Item	Symbol	Min.	Typ.	Max.	Unit	Test Conditions
Input high voltage	V_{IH}	$V_{CC}Q \times 0.7$	—	$V_{CC}Q$ + 0.3	V	
Input low voltage	V_{IL}	–0.3	—	$V_{CC}Q \times 0.3$	V	
Schmitt trigger input characteristics	$V_{IH} – V_{IL}$	0.4	—	—	V	
Output low voltage	V_{OL}	—	—	0.4	V	I_{OL} = 3.0 mA

Page 1084, Table 27.4 Permissible Output Currents

[Before Change]

Conditions: V_{CC} = $PLLV_{CC}$ = 1.4 V to 1.6 V, $V_{CC}Q$ = 3.0 V to 3.6 V, AV_{CC} = 4.5 V to 5.5 V,
V_{SS} = $PLLV_{SS}$ = $V_{SS}Q$ = AV_{SS} = 0 V, Ta = -40°C to = ┼85°C

Item		Symbol	Min.	Typ.	Max.	Unit
Permissible output low current (per pin)	PB21 to PB18, PB13 to PB10, PB7 to PB4	I_{OL}	—	—	15	mA
	PF1 to PF0				10	mA
	Output pins other than above				2	mA
Permissible output low current (total)		ΣI_{OL}	—	—	80	mA
Permissible output high current (per pin)		$-I_{OH}$	—	—	2	mA
Permissible output high current (total)		$\Sigma -I_{OH}$	—	—	25	mA

[After Change]

Conditions: V_{CC} = $PLLV_{CC}$ = 1.4 V to 1.6 V, $V_{CC}Q$ = 3.0 V to 3.6 V,
V_{SS} = $PLLV_{SS}$ = $V_{SS}Q$ = 0 V, Ta = -40°C to ┼85°C

Item		Symbol	Min.	Typ.	Max.	Unit
Permissible output low current (per pin)	TIOC3B, TIOC3D TIOC4A to TIOC4D TIOC3BS, TIOC3DS TIOC4AS to TIOC4DS	I_{OL}	—	—	15	mA
	SCL, SDA				10	mA
	Output pins other than above				2	mA
Permissible output low current (total)		ΣI_{OL}	—	—	80	mA
Permissible output high current (per pin)	TIOC3B, TIOC3D TIOC4A to TIOC4D TIOC3BS, TIOC3DS TIOC4AS to TIOC4DS	$-I_{OH}$	—	—	5	mA
	Output pins other than above		—	—	2	mA
Permissible output high current (total)		$\Sigma -I_{OH}$	—	—	25	mA

Page 1085, 27.4 AC Characteristics, Table 27.5 Maximum Operating Frequency

[Before Change]

Item		Symbol	Min.	Typ.	Max.	Unit	Remarks
Operating frequency	CPU (Iϕ)	f	16	—	160	MHz	
	Internal bus, external bus (Bϕ)		16	—	40		
	Peripheral module (Pϕ)		2	—	40		

[After Change]

Item		Symbol	Min.	Typ.	Max.	Unit	Remarks
Operating frequency	CPU (Iϕ)	f	32	—	160	MHz	
	Internal bus, external bus (Bϕ)		32	—	40		
	Peripheral module (Pϕ)		4	—	40		

Page 1086, 27.4.1 Clock Timing, Table 27.6 Clock Timing is deleted as follows:

[Before Change]

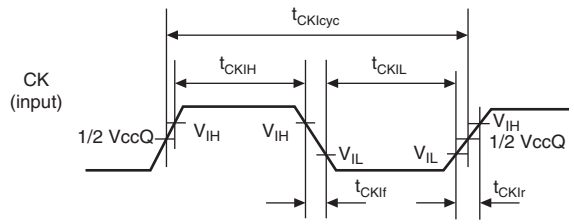
Item	Symbol	Min.	Max.	Unit	Figure
CK clock input frequency	f_{CK}	16	40	MHz	

[After Change]

Deleted

Page 1087, 27.4 AC Characteristics, Figure 27.3 CK Clock Input Timing is deleted as follows:

[Before Change]



[After Change]

Deleted

Page 1089, 27.4.2 Control Signal Timing, Table 27.7 Control Signal Timing

[Before Change]

		Bϕ = 40 MHz			
Item	**Symbol**	**Min.**	**Max.**	**Unit**	**Figure**
MD1, MD0 setup time	t_{MDS}	20	—	t_{Bcyc}*4	Figure 27.8

[After Change]

		Bϕ = 40 MHz			
Item	**Symbol**	**Min.**	**Max.**	**Unit**	**Figure**
MD1, MD0 setup time	t_{MDS}	20	—	t_{cyc}	Figure 27.8

Page 1089, 27.4.2 Control Signal Timing, Table 27.7 Control Signal Timing

[Before Change]

Notes: 2. In standby mode or when the clock multiplication ratio is changed, $t_{RESW} = t_{OSC2}$ (T.B.D. ms).

3. In standby mode, $t_{RESW} = t_{OSC2}$ (T.B.D. ms).

[After Change]

Notes: 2. In standby mode or when the clock multiplication ratio is changed, $t_{RESW} = t_{OSC2}$ (Min.10 ms).

3. In standby mode, $t_{RESW} = t_{OSC2}$ (Min.10 ms).

Page 1093, 27.4.3 Bus Timing, Table 27.8 Bus Timing

[Before Change]

		Bϕ = 40 MHz*			
Item	**Symbol**	**Min.**	**Max.**	**Unit**	**Figure**
Read data hold time 2	t_{RDH2}	5	—	ns	Figures 27.20 to 27.23, 27.28 to 27.30

[After Change]

		Bϕ = 40 MHz*			
Item	**Symbol**	**Min.**	**Max.**	**Unit**	**Figure**
Read data hold time 2	t_{RDH2}	2	—	ns	Figures 27.20 to 27.23, 27.28 to 27.30

Page 1131, 27.4.14 AC Characteristics Measurement Conditions, Figure 27.53 Output Load Current, [Note] 2

[Before Change]

2. I_{OL} and I_{OH} are shown in table 26.4.

[After Change]

2. I_{OL} and I_{OH} are shown in table 27.4.

Page 1133, 27.7 Flash Memory Characteristics

[Before Change]

Table 27.21 Flash Memory Characteristics

Conditions: V_{CC} = 1.4 V to 1.6 V, $V_{CC}Q$ = 3.0 V to 3.6 V, AV_{CC} = 4.5 V to 5.5 V, AVREF = 4.5V to AV_{CC}, V_{SS} = $PLLV_{SS}$ = AV_{SS} = 0 V, Ta = -40°C to 85°C

Item	Symbol	Min.	Typ.	Max.	Unit
Write time *1*2*4	t_P	—	20	400	ms/256 bytes
Erase time *1*3*5	t_E	—	2	20	s/byte
Number of rewrite times	N_{WEC}	—	—	100	times

Notes:
1. Use the on-chip writing/erasing routine for writing or erasing.
2. When all 0 is written
3. When a 64-kbyte block is erased
4. Total rewrite time (write time + erase time) is as follows.
   60 s (Typ.), reference value: 90 s, 120 s (Max.)
   However, 90% of this time falls within the range of the reference value.
5. t_E is distributed centering around the typical value (Typ.).

[After Change]

Table 27.21 Flash Memory Characteristics

Conditions: V_{CC} = $PLLV_{CC}$ = 1.4 V to 1.6 V, $V_{CC}Q$ = 3.0 V to 3.6 V,
V_{SS} = $PLLV_{SS}$ = $V_{CC}Q$= 0 V, Ta = -40°C to 85°C

Item	Symbol	Min.	Typ.	Max.	Unit
Write time *1*2*4	t_P	—	2	20	ms/256 bytes
Erase time *1*2*4	t_E	—	80	260	ms/8-kbyte block
		—	600	1600	ms/64-kbyte block
		—	1200	3000	ms/128-kbyte block
Write time (total) *1*2*4	Σt_P	—	4.5	12	s/512 kbytes
Erase time (total) *1*2*4	Σt_E	—	4.5	12	s/512 kbytes
Write and erase time (total) *1*2*4	Σt_{PE}	—	9	24	s/512 kbytes
Number of rewrite times	N_{WEC}	100*3	—	—	times

Notes:
1. Write time and erase time depend on data.
2. Data transfer time is not included in the write and erase time.
3. Minimum value that guarantees all characteristics after rewriting (guarantees in the range from 1 to Min. value)
4. Characteristics when the number of rewrite times falls within the range including the Min. value.

Appendix

[Appendix –A] Table A.1 Pin States

[Before Change]

Pin Function		Pin State							
		Reset State				Power-Down State			
		Power-On*8							
Type	Pin Name	Extended without ROM 8 Bits	Extended without ROM 16 Bits	Extended with ROM	Single Chip	Manual	Software Standby	Sleep	Bus Master-ship Release
Clock	CK (clock mode 6)			O		O	O/Z*4	O	O/Z*4

[After Change]

Pin Function		Pin State							
		Reset State				Power-Down State			
		Power-On*8							
Type	Pin Name	Extended without ROM 8 Bits	Extended without ROM 16 Bits	Extended with ROM	Single Chip	Manual	Software Standby	Sleep	Bus Master-ship Release
Clock	CK (clock mode 6)		O		Z	O	O/Z*4	O	O/Z*4

[Appendix-A] Table A.1 Pin States

[Before Change]

Pin Function		Pin State							
		Reset State				Power-Down State			
		Power-On*[8]							
		Extended without ROM		Extended with					Bus Master-ship
Type	Pin Name	8 Bits	16 Bits	ROM	Single Chip	Manual	Software Standby	Sleep	Release
Emulator	ASEBRK			I		I	I	I	I
	ASEBRKAK			O		O	I	O	O
	TDO			Z		O/Z*[5]	O/Z*[5]	O/Z*[5]	O/Z*[5]

[After Change]

Pin Function		Pin State							
		Reset State				Power-Down State			
		Power-On*[8]							
		Extended without ROM		Extended with					Bus Master-ship
Type	Pin Name	8 Bits	16 Bits	ROM	Single Chip	Manual	Software Standby	Sleep	Release
Emulator	ASEBRK/ ASEBRKAK			O		O	I	O	O
	TDO			O/Z*[5]		O/Z*[5]	O/Z*[5]	O/Z*[5]	O/Z*[5]