To our customers,

Old Company Name in Catalogs and Other Documents

On April 1st, 2010, NEC Electronics Corporation merged with Renesas Technology Corporation, and Renesas Electronics Corporation took over all the business of both companies. Therefore, although the old company name remains in this document, it is a valid Renesas Electronics document. We appreciate your understanding.

Renesas Electronics website: http://www.renesas.com

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Renesas Electronics Corporation

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HITACHI SEMICONDUCTOR TECHNICAL UPDATE

Classification of Production	MPU			No	TN-SH7-473A/E	Rev	1
THEME	A SH3 and SH3-DSP usage notice on the IRQ edge interrupt		Classification of Information	1. Spec change 2. Supplement of Documents (3.) Limitation of Use 4. Change of Mask 5. Change of Production Line			
PRODUCT NAME	SH7729R SH7709S SH7727 SH7706	Lot No. ALL	Reference Documents	SH7729R Hardware Manual Rev.3.0, ADE-602-229B SH7709S Hardware Manual Rev.3.0, ADE-602-250B SH7727 Hardware Manual Rev.4.0, ADE-602-209C SH7706 Hardware Manual Rev.2.0, ADE-602-235A	Effective Date Eternal		

SH7709S, SH7729R, SH7727 and SH7706 have followed usage notice on the IRQ edge interrupt mode.

1. Phenomenon

When the Interrupt Request Register 0 (IRR0) is read and the IRQnR bits (n=0~5) are set at the same time, the read value of the IRQnR bits are “0”, however the IRQnR bits are read as “1” internally. Thus the IRQnR bits will be cleared when they will be written as “0”.

Our original specification was that the IRQnR bits are cleared only when they are read after they are set to “1”. However this particular case does not meet the original specification.

The errata will be the problem in the following sequence.

(1) IRR0 is read in the IRQn interrupt handler

(2) IRQm(m is not equal n) edge interrupt is input at the same time with (1)

(3) The read value of the IRQnR is “1” and the read value of the IRQmR is “0” at the read (1)

(4) Write H’00 in the IRR0 in order to clear the IRQnR bit.

(5) The IRQnR bit and the IRQmR bit are cleared (the write at (4) does not intend to clear the IRQmR bits)

(6) The IRQm interrupt is cleared because of the write at (4)

2. workaround

When you use the IRQ interrupt as edge mode, please use the following note.

Note:

Please write “0” to the bits which you want to clear and write “1” to the other bits. The value “1” will not be written in any bit of the IRR0.