To our customers,

Old Company Name in Catalogs and Other Documents

On April 1st, 2010, NEC Electronics Corporation merged with Renesas Technology Corporation, and Renesas Electronics Corporation took over all the business of both companies. Therefore, although the old company name remains in this document, it is a valid Renesas Electronics document. We appreciate your understanding.

Renesas Electronics website: http://www.renesas.com

April 1st, 2010
Renesas Electronics Corporation

Issued by: Renesas Electronics Corporation (http://www.renesas.com)

Send any inquiries to http://www.renesas.com/inquiry.

HITACHI MICROCOMPUTER TECHNICAL UPDATE

DATE	8 September 2000	No.	TN-SH7-252A/E
THEME	SH-4 SCI transmission usage notice		
CLASSIFICATION	☐ Spec change ■ Limitation on Use ☐ Supplement of Documents		
PRODUCTNAME	HD6417750BP200, HD6417750BP200M, HD6417750F167, HD6417750F167I, HD6417750VF128, HD6417750SF167A, HD6417750SVF133A, HD6417750SVBT133A	Lot	All
REFERENCE DOCUMENTS	SH7750 Series Hardware Manual	Rev. 1 - 4	EffectiveDate From Eternity

When a transmission is done using built-in SCI, a failure may occur.

1. Contents

1.1 Conditions

a. The input mode of an external SCK clock (SCSCR1.CKE1=1).

b. Synchronous clock mode (SCSMR1.C/A=1).

c. “Transmission” or “transmission and reception” (SCSCR1.TE=1).

When all above, i.e., a, b and c, are satisfied.

1.2 Phenomenon

A data may be transmitted twice(or more).

2. Workaround

To avoid this failure, please keep one of the 2.1 or 2.2.

2.1 Workaround #1

a. In the case of “PLL ON”.

As shown in Fig.1, please synchronize SH-4 SCK signal using CKIO.

The minimum SCK clock cycle time in this case becomes a (peripheral clock cycle time×8).

By doing this workaround, because the timing margin of an equivalent for the synchronization of SCK terminal, TxD terminal, and RxD terminal decreases, please be careful.

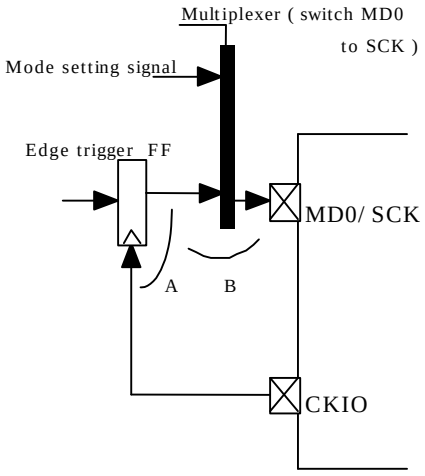

Fig.1 The example of a plan in SH-4

b. In the case of “PLL OFF”.

An operation cannot be warranted.

2.2 Workaround #2

a. External clock mode (=SCK clock input mode).

b. Synchronous clock mode.

c. “Transmission” or “transmission and reception”.

Please do not set it as the conditions of a, b and c.

3. For SCK, Input Timing of CKIO

Including edge-trigger type F.F and delay of multiplexer on Fig1, which should satisfy the conditions of the timing below.

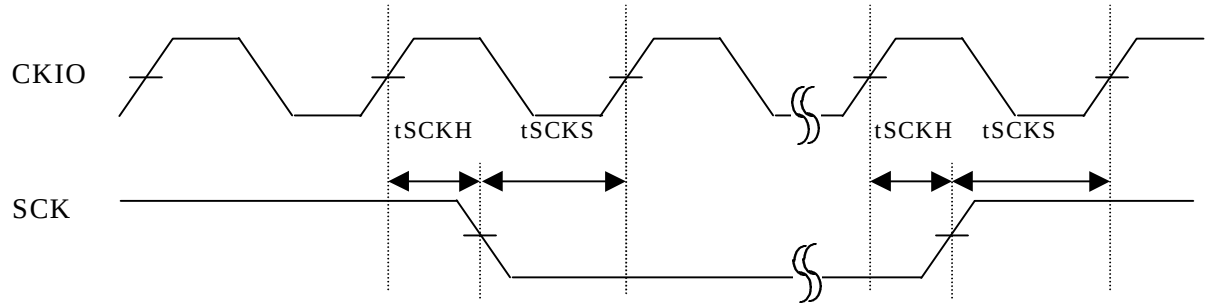

Fig 2. For SCK, Input Timing of CKIO

Table 1. Timing of Peripheral Module Signal

Product Name	tSCKS		tSCKH		Unit
	Min.	Max.	Min.	Max.	
HD6417750BP200	5	-	0	-	ns
HD6417750BP200M	5	-	0	-	ns
HD6417750F167	5	-	0	-	ns
HD6417750F167I	5	-	0	-	ns
HD6417750VF128	8	-	0	-	ns
HD6417750SF167A	5	-	0	-	ns
HD6417750SVF133A	8	-	0	-	ns
HD6417750SVBT133A	8	-	0	-	ns