To our customers,

Old Company Name in Catalogs and Other Documents

On April 1st, 2010, NEC Electronics Corporation merged with Renesas Technology Corporation, and Renesas Electronics Corporation took over all the business of both companies. Therefore, although the old company name remains in this document, it is a valid Renesas Electronics document. We appreciate your understanding.

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Renesas Electronics Corporation

Issued by: Renesas Electronics Corporation (http://www.renesas.com)

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HITACHI SEMICONDUCTOR TECHNICAL UPDATE

Classification of Production	MPU			No	TN-SH7-409A/E	Rev	1
THEME	Set to BSC MCR of SH7615/SH7616, when Synchronous DRAM is connected.		Classification of Information	1. Spec change 2. Supplement of Documents 3. Limitation of Use 4. Change of Mask 5. Change of Production Line			
PRODUCT NAME	HD6417615ARF HD6417616RF	Lot No. ALL	Reference Documents	SH7615 Hardware Manual ADE-602-198 Rev.1.0 SH7616 Hardware Manual ADE-602-243 Rev.1.0		Effective Date Permanent	

When Synchronous DRAM is connected, you can set to TRP1, TRP0 bit of SH7615/SH7616 BSC MCR as follows.

[Error]

7.2.7 Individual Memory Control Register (MCR)

Bits 1 and 15 - $\overline{\text{RAS}}$ Precharge Time(TRP1,TRP0) : When DRAM is connected, specifies the minimum number of cycles after $\overline{\text{RAS}}$ is negated before the next assert. When Synchronous DRAM is connected, specifies the minimum number of cycles after precharge until a bank active command is output. See section 7.5, Synchronous DRAM Interface, for details.

Bit 1: TRP1	Bit 15: TRP0	Description	
0	0	1 cycle	(Initial value)
	1	2 cycles	
1	0	Reserved (do not set)	
	1	Reserved (do not set)	

[Correct]

7.2.7 Individual Memory Control Register (MCR)

Bits 1 and 15 - $\overline{\text{RAS}}$ Precharge Time(TRP1,TRP0) : When DRAM is connected, specifies the minimum number of cycles after $\overline{\text{RAS}}$ is negated before the next assert. When Synchronous DRAM is connected, specifies the minimum number of cycles after precharge until a bank active command is output. See section 7.5, Synchronous DRAM Interface, for details.

• For DRAM interface

Bit 1: TRP1	Bit 15: TRP0	Description	
0	0	1 cycle	(Initial value)
	1	2 cycles	
1	0	Reserved (do not set)	
	1	Reserved (do not set)	

• For Synchronous DRAM interface

Bit 1: TRP1	Bit 15: TRP0	Description	
0	0	1 cycle	(Initial value)
	1	2 cycles	
1	0	3 cycles	
	1	4 cycles	