

RENESAS TECHNICAL UPDATE

TOYOSU FORESIA, 3-2-24, Toyosu, Koto-ku, Tokyo
135-0061, Japan

Renesas Electronics Corporation

<https://www.renesas.com/jp/ja/support/contact/>

Product Category	MPU & MCU	Document No.	TN-SY*-A0081A/E	Rev.	1.00
Title	Correction of FCACHE2 errors		Information Category	Technical Notification	
Applicable Product	S3A1 Microcontroller Group S3A3 Microcontroller Group S3A6 Microcontroller Group S3A7 Microcontroller Group S5D3 Microcontroller Group S5D5 Microcontroller Group S5D9 Microcontroller Group S7G2 Microcontroller Group	Lot No.	Reference Document	Refer the table 1	
		All			

Table 1 Reference Document List

No	Reference Document Name	Rev	Document Control Number
1	S3A1 Microcontroller Group User's Manual	1.20	R01UM0010EU0120
2	S3A3 Microcontroller Group User's Manual	1.10	R01UM0006EU0110
3	S3A6 Microcontroller Group User's Manual	1.30	R01UM0007EU0130
4	S3A7 User's Manual: Microcontroller	1.40	R01UM0002EU0140
5	S5D3 Microcontroller Group User's Manual	1.20	R01UM0011EU0120
6	S5D5 Microcontroller Group User's Manual	1.40	R01UM0009EU0140
7	S5D9 Microcontroller Group User's Manual	1.40	R01UM0004EU0140
8	S7G2 Microcontroller Group User's Manual	1.40	R01UM0001EU0140

1. The changes to the S3A1 microcontroller group are as follows.

<Current description>

47.3 Flash Cache

47.3.1 Overview

The flash cache (FCACHE) speeds up read access from the bus master to the flash memory. The FCACHE includes:

- FCACHE1, for CPU instruction fetches
- FCACHE2, for CPU operand access and DMA
- FLPF, for prefetch access in CPU instruction fetch.

Table 47.4 Flash cache overview

Parameter	Flash cache 1 (FCACHE1)	Flash cache 2 (FCACHE2)	Prefetch buffer (FLPF)
Cache target region	0000 0000h - 007F FFFFh	0000 0000h - 007F FFFFh	0000 0000h - 007F FFFFh
Target bus master	CPU instruction fetch	CPU operand access and access from other than CPU	FLPF
Capacity	128 bytes	8 bytes	16 bytes
Associativity	2-way set associative	Fully associative	-
	-	-	64 bits/entry (64-bit aligned data), 2 entries
	64 bits/entry (64-bit aligned data), 8 entries/ways	64 bits/entry (64-bit aligned data) 1 entry	Next address of previous CPU instruction
Access cycle	Cache hit: 0 wait Cache miss: According to SYSTEM.MEMWAIT register: MEMWAIT = 0: 0 wait MEMWAIT = 1: 1 or 2 waits	Cache hit: 0 wait Cache miss: According to SYSTEM.MEMWAIT register: MEMWAIT = 0: 0 wait MEMWAIT = 1: 1 or 2 waits	Cache hit: 0 wait Cache miss: According to SYSTEM.MEMWAIT register: MEMWAIT = 0: 0 wait MEMWAIT = 1: 1 or 2 waits

<Changed description>

47.3 Flash Cache

47.3.1 Overview

The flash cache (FCACHE) speeds up read access from the bus master to the flash memory. The FCACHE includes:

- FCACHE1, for CPU instruction fetches
- **FCACHE2, for CPU operand access and access from DMAC/DTC**
- FLPF, for prefetch access in CPU instruction fetch.

Table 47.4 Flash cache overview

Parameter	Flash cache 1 (FCACHE1)	Flash cache 2 (FCACHE2)	Prefetch buffer (FLPF)
Cache target region	0000 0000h - 007F FFFFh	0000 0000h - 007F FFFFh	0000 0000h - 007F FFFFh
Target bus master	CPU instruction fetch	CPU operand access and access from DMAC/DTC	CPU instruction fetches
Capacity	128 bytes	8 bytes	16 bytes
Associativity	2-way set associative	Fully associative	-
	-	-	64 bits/entry (64-bit aligned data), 2 entries
	64 bits/entry (64-bit aligned data), 8 entries/ways	64 bits/entry (64-bit aligned data) 1 entry	Next address of previous CPU instruction
Access cycle	Cache hit: 0 wait Cache miss: According to SYSTEM.MEMWAIT register: MEMWAIT = 0: 0 wait MEMWAIT = 1: 1 or 2 waits	Cache hit: 0 wait Cache miss: According to SYSTEM.MEMWAIT register: MEMWAIT = 0: 0 wait MEMWAIT = 1: 1 or 2 waits	Cache hit: 0 wait Cache miss: According to SYSTEM.MEMWAIT register: MEMWAIT = 0: 0 wait MEMWAIT = 1: 1 or 2 waits

2. The changes to the S3A3 microcontroller group are as follows.

<Current description>

47.3 Flash Cache

47.3.1 Overview

The flash cache (FCACHE) speeds up read access from the bus master to the flash memory. The FCACHE includes:

- FCACHE1, for CPU instruction fetch
- FCACHE2, for CPU operand access and DMA
- FLPF, for prefetch access of CPU instruction fetch.

Table 47.4 Flash cache overview

Parameter	Flash cache 1 (FCACHE1)	Flash cache 2 (FCACHE2)	Prefetch buffer (FLPF)
Cache target region	0000 0000h - 007F FFFFh	0000 0000h - 007F FFFFh	0000 0000h - 007F FFFFh
Target bus master	CPU instruction fetch	CPU operand access and access from other than CPU	FLPF
Capacity	128 bytes	8 bytes	16 bytes
Associativity	2-way set associative	Fully associative	-
	• 64 bits/entry (64-bit aligned data) • 8 entries/ways.	• 64 bits/entry (64-bit aligned data) • 1 entry.	• 64 bits/entry (64-bit aligned data) • 2 entries • Next address of previous CPU instruction.
Access cycle	Cache hit: 0 wait Cache miss: According to SYSTEM.MEMWAIT register: MEMWAIT = 0: 0 wait MEMWAIT = 1: 1 and 2 waits	Cache hit: 0 wait Cache miss: According to SYSTEM.MEMWAIT register: MEMWAIT = 0: 0 wait MEMWAIT = 1: 1 and 2 waits	Cache hit: 0 wait Cache miss: According to SYSTEM.MEMWAIT register: MEMWAIT = 0: 0 wait MEMWAIT = 1: 1 and 2 waits

<Changed description>

47.3 Flash Cache

47.3.1 Overview

The flash cache (FCACHE) speeds up read access from the bus master to the flash memory. The FCACHE includes:

- FCACHE1, for CPU instruction fetch
- **FCACHE2, for CPU operand access and access from DMAC/DTC**
- FLPF, for prefetch access of CPU instruction fetch.

Table 47.4 Flash cache overview

Parameter	Flash cache 1 (FCACHE1)	Flash cache 2 (FCACHE2)	Prefetch buffer (FLPF)
Cache target region	0000 0000h - 007F FFFFh	0000 0000h - 007F FFFFh	0000 0000h - 007F FFFFh
Target bus master	CPU instruction fetch	CPU operand access and access from DMAC/DTC	CPU instruction fetches
Capacity	128 bytes	8 bytes	16 bytes
Associativity	2-way set associative	Fully associative	-
	• 64 bits/entry (64-bit aligned data) • 8 entries/ways.	• 64 bits/entry (64-bit aligned data) • 1 entry.	• 64 bits/entry (64-bit aligned data) • 2 entries • Next address of previous CPU instruction.
Access cycle	Cache hit: 0 wait Cache miss: According to SYSTEM.MEMWAIT register: MEMWAIT = 0: 0 wait MEMWAIT = 1: 1 and 2 waits	Cache hit: 0 wait Cache miss: According to SYSTEM.MEMWAIT register: MEMWAIT = 0: 0 wait MEMWAIT = 1: 1 and 2 waits	Cache hit: 0 wait Cache miss: According to SYSTEM.MEMWAIT register: MEMWAIT = 0: 0 wait MEMWAIT = 1: 1 and 2 waits

3. The changes to the S3A6 microcontroller group are as follows.

<Current description>

44.3 Flash Cache

44.3.1 Overview

The flash cache (FCACHE) speeds up read access from the bus master to the flash memory. The FCACHE includes:

- FCACHE1, for CPU instruction fetches
- FCACHE2, for CPU operand access and DMA
- FLPF, for prefetch access of CPU instruction fetches.

Table 44.4 Flash cache overview

Parameter	Flash cache 1 (FCACHE1)	Flash cache 2 (FCACHE2)	Prefetch buffer (FLPF)
Cache target region	0000 0000h - 007F FFFFh	0000 0000h - 007F FFFFh	0000 0000h - 007F FFFFh
Target bus master	CPU instruction fetch	CPU operand access and access from other than CPU	FLPF
Capacity	128 bytes	8 bytes	16 bytes
Associativity	2-way set associative • 64 bits/entry (64-bit aligned data) • 8 entries/ways.	Fully associative • 64 bits/entry (64-bit aligned data) • 1 entry.	- • 64 bits/entry (64-bit aligned data) • 2 entries • Next address of previous CPU instruction.
Access cycle	Cache hit: 0 waits Cache miss: According to SYSTEM.MEMWAIT register: MEMWAIT = 0: 0 wait MEMWAIT = 1: 1 or 2 waits	Cache hit: 0 wait Cache miss: According to SYSTEM.MEMWAIT register: MEMWAIT = 0: 0 wait MEMWAIT = 1: 1 or 2 waits	Cache hit: 0 wait Cache miss: According to SYSTEM.MEMWAIT register: MEMWAIT = 0: 0 wait MEMWAIT = 1: 1 or 2 waits

<Changed description>

44.3 Flash Cache

44.3.1 Overview

The flash cache (FCACHE) speeds up read access from the bus master to the flash memory. The FCACHE includes:

- FCACHE1, for CPU instruction fetches
- **FCACHE2, for CPU operand access and access from DMAC/DTC**
- FLPF, for prefetch access of CPU instruction fetches.

Table 44.4 Flash cache overview

Parameter	Flash cache 1 (FCACHE1)	Flash cache 2 (FCACHE2)	Prefetch buffer (FLPF)
Cache target region	0000 0000h - 007F FFFFh	0000 0000h - 007F FFFFh	0000 0000h - 007F FFFFh
Target bus master	CPU instruction fetch	CPU operand access and access from DMAC/DTC	CPU instruction fetches
Capacity	128 bytes	8 bytes	16 bytes
Associativity	2-way set associative • 64 bits/entry (64-bit aligned data) • 8 entries/ways.	Fully associative • 64 bits/entry (64-bit aligned data) • 1 entry.	- • 64 bits/entry (64-bit aligned data) • 2 entries • Next address of previous CPU instruction.
Access cycle	Cache hit: 0 waits Cache miss: According to SYSTEM.MEMWAIT register: MEMWAIT = 0: 0 wait MEMWAIT = 1: 1 or 2 waits	Cache hit: 0 wait Cache miss: According to SYSTEM.MEMWAIT register: MEMWAIT = 0: 0 wait MEMWAIT = 1: 1 or 2 waits	Cache hit: 0 wait Cache miss: According to SYSTEM.MEMWAIT register: MEMWAIT = 0: 0 wait MEMWAIT = 1: 1 or 2 waits

4. The changes to the S3A7 microcontroller group are as follows.

<Current description>

48.3 Flash Cache

48.3.1 Overview

The flash cache (FCACHE) speeds up read access from the bus master to the flash memory. The FCACHE includes:

- FCACHE1, for CPU instruction fetch
- FCACHE2, for CPU operand access and DMA
- FLPF, for prefetch access of CPU instruction fetch.

Table 48.4 Flash cache overview

Parameter	Flash cache 1 (FCACHE1)	Flash cache 2 (FCACHE2)	Prefetch buffer (FLPF)
Cache target region	0000 0000h - 007F FFFFh	0000 0000h - 007F FFFFh	0000 0000h - 007F FFFFh
Target bus master	CPU instruction fetch	CPU operand access and access from other than CPU	FLPF
Capacity	256 bytes	8 bytes	16 bytes
Associativity	• 8-way set associative • 64 bits/entry (64-bit aligned data) • 4 entries/ways	• Fully associative • 64 bits/entry (64-bit aligned data) • 1 entry	• 64 bits/entry (64-bit aligned data) • 2 entries • Next address of previous CPU instruction
Access cycle	Cache hit: 0 wait Cache miss: According to SYSTEM.MEMWAIT Register setting: MEMWAIT = 0: 0 wait MEMWAIT = 1: 1 or 2 waits	Cache hit: 0 wait Cache miss: According to SYSTEM.MEMWAIT Register setting: MEMWAIT = 0: 0 wait MEMWAIT = 1: 1 or 2 waits	Cache hit: 0 wait Cache miss: According to SYSTEM.MEMWAIT Register setting: MEMWAIT = 0: 0 wait MEMWAIT = 1: 1 or 2 waits

<Changed description>

48.3 Flash Cache

48.3.1 Overview

The flash cache (FCACHE) speeds up read access from the bus master to the flash memory. The FCACHE includes:

- FCACHE1, for CPU instruction fetch
- **FCACHE2, for CPU operand access and access from DMAC/DTC**
- FLPF, for prefetch access of CPU instruction fetch.

Table 48.4 Flash cache overview

Parameter	Flash cache 1 (FCACHE1)	Flash cache 2 (FCACHE2)	Prefetch buffer (FLPF)
Cache target region	0000 0000h - 007F FFFFh	0000 0000h - 007F FFFFh	0000 0000h - 007F FFFFh
Target bus master	CPU instruction fetch	CPU operand access and access from DMAC/DTC	CPU instruction fetches
Capacity	256 bytes	8 bytes	16 bytes
Associativity	• 8-way set associative • 64 bits/entry (64-bit aligned data) • 4 entries/ways	• Fully associative • 64 bits/entry (64-bit aligned data) • 1 entry	• 64 bits/entry (64-bit aligned data) • 2 entries • Next address of previous CPU instruction
Access cycle	Cache hit: 0 wait Cache miss: According to SYSTEM.MEMWAIT Register setting: MEMWAIT = 0: 0 wait MEMWAIT = 1: 1 or 2 waits	Cache hit: 0 wait Cache miss: According to SYSTEM.MEMWAIT Register setting: MEMWAIT = 0: 0 wait MEMWAIT = 1: 1 or 2 waits	Cache hit: 0 wait Cache miss: According to SYSTEM.MEMWAIT Register setting: MEMWAIT = 0: 0 wait MEMWAIT = 1: 1 or 2 waits

5. The changes to the S5D3 microcontroller group are as follows.

<Current description>

50.4 Flash Cache

50.4.1 Overview

The flash cache (FCACHE) speeds up read access from the bus master to the flash memory. The FCACHE includes:

- FCACHE1, for CPU instruction fetches
- FCACHE2, for CPU operand access and DMA
- FLPF, for the prefetch access in CPU instruction fetches.

Table 50.3 Flash cache overview

Parameter	Flash cache 1 (FCACHE1)	Flash cache 2 (FCACHE2)	Prefetch buffer (FLPF)
Cache target region	0000 0000h - 0007 FFFFh	0000 0000h - 0007 FFFFh	0000 0000h - 0007 FFFFh
Target bus master	CPU instruction fetch	CPU operand access and access from other than CPU	FLPF
Capacity	256 bytes	16 bytes	32 bytes

<Changed description>

50.4 Flash Cache

50.4.1 Overview

The flash cache (FCACHE) speeds up read access from the bus master to the flash memory. The FCACHE includes:

- FCACHE1, for CPU instruction fetches
- FCACHE2, for CPU operand access and **DMAC/DTC**
- FLPF, for the prefetch access in CPU instruction fetches.

Table 50.3 Flash cache overview

Parameter	Flash cache 1 (FCACHE1)	Flash cache 2 (FCACHE2)	Prefetch buffer (FLPF)
Cache target region	0000 0000h - 0007 FFFFh	0000 0000h - 0007 FFFFh	0000 0000h - 0007 FFFFh
Target bus master	CPU instruction fetch	CPU operand access and access the DMAC/DTC	CPU instruction fetches
Capacity	256 bytes	16 bytes	32 bytes

6. The changes to the S5D5 microcontroller group are as follows.

<Current description>

53.4.1 Overview

The flash cache (FCACHE) speeds up read access from the bus master to the flash memory. The FCACHE includes:

- FCACHE1, for CPU instruction fetches
- FCACHE2, for CPU operand access and DMA
- FLPF, for the prefetch access in CPU instruction fetches.

Table 53.3 Flash cache overview

Parameter	Flash cache 1 (FCACHE1)	Flash cache 2 (FCACHE2)	Prefetch buffer (FLPF)
Cache target region	0000 0000h - 000F FFFFh	0000 0000h - 000F FFFFh	0000 0000h - 000F FFFFh
Target bus master	CPU instruction fetch	CPU Operand Access and Access from other than CPU	FLPF
Capacity	256 bytes	16 bytes	32 bytes
Associativity	• 8-way set associative • 128 bits/entry (128-bit aligned data) • 2 entries/way	• Fully associative • 128 bits/entry (128-bit aligned data) • 1 entry for FCACHE2	• Fully associative • 128 bits/entry (128-bit aligned data) • 2 entries
Access cycles	• Cache hit: 0 waits • Cache miss: Number of waits set in Flash Wait Cycle Register	• Cache hit: 0 waits • Cache miss: Number of waits set in Flash Wait Cycle Register	• Cache hit: 0 waits • Cache miss: Number of waits set in Flash Wait Cycle Register

<Changed description>

53.4.1 Overview

The flash cache (FCACHE) speeds up read access from the bus master to the flash memory. The FCACHE includes:

- FCACHE1, for CPU instruction fetches
- **FCACHE2, for CPU operand access and access from DMAC/DTC and EDMAC**
- FLPF, for the prefetch access in CPU instruction fetches.

Table 53.3 Flash cache overview

Parameter	Flash cache 1 (FCACHE1)	Flash cache 2 (FCACHE2)	Prefetch buffer (FLPF)
Cache target region	0000 0000h - 000F FFFFh	0000 0000h - 000F FFFFh	0000 0000h - 000F FFFFh
Target bus master	CPU instruction fetch	CPU Operand Access and Access from DMAC/DTC and EDMAC	CPU instruction fetches
Capacity	256 bytes	16 bytes	32 bytes
Associativity	• 8-way set associative • 128 bits/entry (128-bit aligned data) • 2 entries/way	• Fully associative • 128 bits/entry (128-bit aligned data) • 1 entry for FCACHE2	• Fully associative • 128 bits/entry (128-bit aligned data) • 2 entries
Access cycles	• Cache hit: 0 waits • Cache miss: Number of waits set in Flash Wait Cycle Register	• Cache hit: 0 waits • Cache miss: Number of waits set in Flash Wait Cycle Register	• Cache hit: 0 waits • Cache miss: Number of waits set in Flash Wait Cycle Register

7. The changes to the S5D9 microcontroller group are as follows.

<Current description>

55.4.1 Overview

The flash cache (FCACHE) speeds up read access from the bus master to the flash memory. The FCACHE includes:

- FCACHE1, for CPU instruction fetches
- FCACHE2, for CPU operand access and DMA
- FLPF, for the prefetch access in CPU instruction fetches.

Table 55.3 Flash cache overview

Parameter	Flash cache 1 (FCACHE1)	Flash cache 2 (FCACHE2)	Prefetch Buffer (FLPF)
Cache target region	0000 0000h - 001F FFFFh	0000 0000h - 001F FFFFh	0000 0000h - 001F FFFFh
Target bus master	CPU instruction fetch	CPU Operand Access and Access from other than CPU	FLPF
Capacity	256 bytes	16 bytes	32 bytes
Associativity	• 8-way set associative • 128 bits/entry (128-bit aligned data) • 2 entries/way	• Fully associative • 128 bits/entry (128-bit aligned data) • 1 entry for FCACHE2	• Fully associative • 128 bits/entry (128-bit aligned data) • 2 entries
Access cycles	• Cache hit: 0 waits • Cache miss: Number of waits set in Flash Wait Cycle Register	• Cache hit: 0 waits • Cache miss: Number of waits set in Flash Wait Cycle Register	• Cache hit: 0 waits • Cache miss: Number of waits set in Flash Wait Cycle Register

<Changed description>

55.4.1 Overview

The flash cache (FCACHE) speeds up read access from the bus master to the flash memory. The FCACHE includes:

- FCACHE1, for CPU instruction fetches
- **FCACHE2, for CPU operand access and access from DMAC/DTC, EDMAC, and graphic IP**
- FLPF, for the prefetch access in CPU instruction fetches.

Table 55.3 Flash cache overview

Parameter	Flash cache 1 (FCACHE1)	Flash cache 2 (FCACHE2)	Prefetch Buffer (FLPF)
Cache target region	0000 0000h - 001F FFFFh	0000 0000h - 001F FFFFh	0000 0000h - 001F FFFFh
Target bus master	CPU instruction fetch	CPU Operand Access and Access from DMAC/DTC, EDMAC, and graphic IP	CPU instruction fetches
Capacity	256 bytes	16 bytes	32 bytes
Associativity	• 8-way set associative • 128 bits/entry (128-bit aligned data) • 2 entries/way	• Fully associative • 128 bits/entry (128-bit aligned data) • 1 entry for FCACHE2	• Fully associative • 128 bits/entry (128-bit aligned data) • 2 entries
Access cycles	• Cache hit: 0 waits • Cache miss: Number of waits set in Flash Wait Cycle Register	• Cache hit: 0 waits • Cache miss: Number of waits set in Flash Wait Cycle Register	• Cache hit: 0 waits • Cache miss: Number of waits set in Flash Wait Cycle Register

8. The changes to the S7G2 microcontroller group are as follows.

<Current description>

55.3 Flash Cache

55.3.1 Overview

The flash cache (FCACHE) speeds up read access from the bus master to the flash memory. The FCACHE includes:

- FCACHE1, for CPU instruction fetches
- FCACHE2, for CPU operand access and DMA
- FLPF, for the prefetch access in CPU instruction fetches.

Table 55.3 Flash cache overview

Parameter	Flash cache 1 (FCACHE1)	Flash cache 2 (FCACHE2)	Prefetch Buffer (FLPF)
Cache target region	0000 0000h - 003F FFFFh	0000 0000h - 003F FFFFh	0000 0000h - 003F FFFFh
Target bus master	CPU instruction fetch	CPU Operand Access and Access from other than CPU	FLPF
Capacity	256 bytes	16 bytes	32 bytes
Associativity	• 8-way set associative • 128 bits/entry (128-bit aligned data) • 2 entries/way	• Fully associative • 128 bits/entry (128-bit aligned data) • 1 entry for FCACHE2	• Fully associative • 128 bits/entry (128-bit aligned data) • 2 entries
Access cycles	• Cache hit: 0 waits • Cache miss: Number of waits set in Flash Wait Cycle Register	• Cache hit: 0 waits • Cache miss: Number of waits set in Flash Wait Cycle Register	• Cache hit: 0 waits • Cache miss: Number of waits set in Flash Wait Cycle Register

<Changed description>

55.3 Flash Cache

55.3.1 Overview

The flash cache (FCACHE) speeds up read access from the bus master to the flash memory. The FCACHE includes:

- FCACHE1, for CPU instruction fetches
- **FCACHE2, for CPU operand access and access from DMAC/DTC, EDMAC, and graphic IP**
- FLPF, for the prefetch access in CPU instruction fetches.

Table 55.3 Flash cache overview

Parameter	Flash cache 1 (FCACHE1)	Flash cache 2 (FCACHE2)	Prefetch Buffer (FLPF)
Cache target region	0000 0000h - 003F FFFFh	0000 0000h - 003F FFFFh	0000 0000h - 003F FFFFh
Target bus master	CPU instruction fetch	CPU Operand Access and Access from DMAC/DTC, EDMAC, and graphic IP	CPU instruction fetches
Capacity	256 bytes	16 bytes	32 bytes
Associativity	• 8-way set associative • 128 bits/entry (128-bit aligned data) • 2 entries/way	• Fully associative • 128 bits/entry (128-bit aligned data) • 1 entry for FCACHE2	• Fully associative • 128 bits/entry (128-bit aligned data) • 2 entries
Access cycles	• Cache hit: 0 waits • Cache miss: Number of waits set in Flash Wait Cycle Register	• Cache hit: 0 waits • Cache miss: Number of waits set in Flash Wait Cycle Register	• Cache hit: 0 waits • Cache miss: Number of waits set in Flash Wait Cycle Register

- That's all-