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# RENESAS TECHNICAL UPDATE

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| Product Category | MPU/MCU | | Document No. | TN-RZ*-A045A/E | Rev. | 1.00 |
|---|---|---|---|---|---|---|
| Title | RZ/T1 Group User's Manual: Hardware Restriction for Cortex-M3 Nested Vector Interrupt Controller when it is used with DMAC | | Information Category | Technical Notification | | |
| Applicable Product | RZ/T1 Group (only in products incorporating an R-IN Engine) | Lot No.<br>All lots | Reference Document | RZ/T1 Group User's Manual: Hardware Rev1.30<br>R01UH0483EJ0130 Rev.1.30 | | |

We have identified restriction, when Cortex-M3 Nested Vector Interrupt Controller (NVIC) No.97-101, 103-108 or 111-113 interrupt are used as DMA transfer completion interrupt.

The following describes restriction, workaround and correction.

1.Conditions

In case Cortex-M3 Nested Vector Interrupt Controller (NVIC) No.97-101, 103-108 or 111-113 interrupt are used as DMA transfer completion interrupt.

Table 1. CM3 interrupt vector table

| Vector Number | Request source | Source | | Detection type | DMAC | DMAC setting vector number |
|---|---|---|---|---|---|---|
| 97 | EtherCAT Slave | ETHCSI0 | EtherCAT Sync0 interrupt | Level/Edge | Y | 73 |
| 98 | | ETHCSI1 | EtherCAT Sync1 interrupt | Level/Edge | Y | 74 |
| 99 | | ETHCI | EtherCAT interrupt | Level/Edge | Y | 75 |
| 100 | | ETHCSOFI | EtherCAT SOF interrupt | Edge | Y | 76 |
| 101 | | ETHCEOFI | EtherCAT EOF interrupt | Edge | Y | 77 |
| 103 | EtherMAC | ETHMMAI | Ether MII management access completion interrupt | Edge | Y | 64 |
| 104 | | ETHPPIT | Ether pause packet transmission completed | Edge | Y | 65 |
| 105 | | ETHIT | Ether transmission completed interrupt | Edge | Y | 66 |
| 106 | Switch with IEEE1588 | ETHSWI | Ether SWITCH interrupt | Level/Edge | Y | 45 |
| 107 | | ETHSWDLRI | Ether SWITCH DLR interrupt | Level/Edge | Y | 46 |
| 108 | | ETHSWSOI | Ether SWITCH SYNCOUT interrupt | Edge | Y | 47 |
| 111 | EtherMAC | ETHDMAIR | Ether MACDMA reception completed | Level/Edge | Y | 51 |
| 112 | | ETHDMAIT | Ether MACDMA transmission completed | Edge | Y | 52 |
| 113 | | ETHRFI | Reception frame normal interrupt | Level/Edge | Y | 53 |

2.Phenomenon

An interrupt is generated when DMA transfer starts.

DMA transfer completion interrupt is not generated.

3.Workaround

Interrupt in table 1. cannot be used as DMA transfer completion interrupt. To confirm DMA transfer completion, check END bit of CHSTAT_n register.

4.Correction

Table.1 Correction for User's Manual Hardware

| Page | Chapter | Description |
|---|---|---|
| 383 | 12.5.2.1 | [Current description]<br>Table 12.6 CM3 Interrupt Vector Table (3/4) |

| Vector Number | Request Source | Source | | Detection Type | DMAC | DMAC setting vector Number |
|---|---|---|---|---|---|---|
| 80 | RSPI Unit0 | SPRI0 | Reception buffer full | Edge | Y | 80 |
| 81 | | SPTI0 | Transmission buffer empty | Edge | Y | 81 |
| 82 | | SPEI0 | Mode fault error/overrun error/parity error | Level | N | 82 |
| 83 | | SPII0 | RSPI idle | Level | N | 83 |
| 84 | RSPI Unit1 | SPRI1 | Reception buffer full | Edge | Y | 84 |
| 85 | | SPTI1 | Transmission buffer empty | Edge | Y | 85 |
| 86 | | SPEI1 | Mode fault error/overrun error/parity error | Level | N | 86 |
| 87 | | SPII1 | RSPI idle | Level | N | 87 |
| 88 | RS-CAN | CANRFI | CAN reception FIFO | Level | N | 104 |
| 89 | | CANFIR0 | CAN0 transmission and reception FIFO reception completed | Level | N | 105 |
| 90 | | CANTI0 | CAN0 transmission | Level | N | 106 |
| 91 | | CANFIR1 | CAN1 transmission and reception FIFO reception completed | Level | N | 107 |
| 92 | | CANTI1 | CAN1 transmission | Level | N | 108 |
| 93 | | CANGE | CAN global error | Level | N | 262 |
| 94 | | CANIE0 | CAN0 error | Level | N | 263 |
| 95 | | CANIE1 | CAN1 error | Level | N | 264 |
| 96 | EtherCAT Slave (optional) | HWRTOS | HW-RTOS interrupt | Level | N | 253 |
| 97 | | ETHCSI0 | EtherCAT Sync0 interrupt | Level/Edge*3 | Y | 73 |
| 98 | | ETHCSI1 | EtherCAT Sync1 interrupt | Level/Edge*3 | Y | 74 |
| 99 | | ETHCI | EtherCAT interrupt | Level/Edge*2 | Y | 75 |
| 100 | | ETHCSOFI | EtherCAT SOF interrupt | Edge | Y | 76 |
| 101 | | ETHCEOFI | EtherCAT EOF interrupt | Edge | Y | 77 |
| 102 | Ether MAC | - | Reserved | - | - | - |
| 103 | | ETHMMAI | Ether MII management access completion interrupt | Edge | Y | 64 |
| 104 | | ETHPPIT | Ether pause packet transmission completed | Edge | Y | 65 |
| 105 | | ETHIT | Ether transmission completed interrupt | Edge | Y | 66 |
| 106 | Switch with IEEE1588 | ETHSWI | Ether SWITCH interrupt | Level/Edge*2 | Y | 45 |
| 107 | | ETHSWDLRI | Ether SWITCH DLR interrupt | Level/Edge*2 | Y | 46 |
| 108 | | ETHSWSOI | Ether SWITCH SYNCOUT interrupt | Edge | Y | 47 |
| 109 | Ether MAC | ETHRFIV | RX FIFO overflow | Edge | N | 67 |
| 110 | | ETHTFIU | TX FIFO underflow | Edge | N | 68 |
| 111 | | ETHDMAIR | Ether MACDMA reception completed | Level/Edge*2 | Y | 51 |
| 112 | | ETHDMAIT | Ether MACDMA transmission completed | Edge | Y | 52 |
| 113 | | ETHRFI | Reception frame normal interrupt | Level/Edge*2 | Y | 53 |
| 114 | | - | Reserved | - | - | - |
| 115 | | ETHTFIE | TX-FIFO error interrupt | Level | N | 69 |
| 116 | | ETHRFE | Ether reception frame error | Level | N | 70 |
| 117 | | ETHDRIE | MACDMA reception error interrupt | Edge | N | 246 |
| 118 | | ETHDTIE | MACDMA transmission error interrupt | Edge | N | 247 |
| 119 | | - | Reserved | - | - | - |
| 120 | EtherCAT Slave (optional) | ETHCRSTI | EtherCAT RESET interrupt | Edge | N | 79 |
| 121 | | ETHCWDTI | EtherCAT WDT interrupt | Edge | N | 78 |

| Page | Chapter | Description |
|---|---|---|

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|---|---|---|
| 383 | 12.5.2.1 | [Correct description】<br>Table 12.6 CM3 Interrupt Vector Table (3/4) |

| Vector Number | Request Source | Source | | Detection Type | DMAC | DMAC setting vector Number |
|---|---|---|---|---|---|---|
| 80 | RSPI Unit0 | SPRI0 | Reception buffer full | Edge | Y | 80 |
| 81 | | SPTI0 | Transmission buffer empty | Edge | Y | 81 |
| 82 | | SPEI0 | Mode fault error/overrun error/parity error | Level | N | 82 |
| 83 | | SPII0 | RSPI idle | Level | N | 83 |
| 84 | RSPI Unit1 | SPRI1 | Reception buffer full | Edge | Y | 84 |
| 85 | | SPTI1 | Transmission buffer empty | Edge | Y | 85 |
| 86 | | SPEI1 | Mode fault error/overrun error/parity error | Level | N | 86 |
| 87 | | SPII1 | RSPI idle | Level | N | 87 |
| 88 | RS-CAN | CANRFI | CAN reception FIFO | Level | N | 104 |
| 89 | | CANFIR0 | CAN0 transmission and reception FIFO reception completed | Level | N | 105 |
| 90 | | CANTI0 | CAN0 transmission | Level | N | 106 |
| 91 | | CANFIR1 | CAN1 transmission and reception FIFO reception completed | Level | N | 107 |
| 92 | | CANTI1 | CAN1 transmission | Level | N | 108 |
| 93 | | CANGE | CAN global error | Level | N | 262 |
| 94 | | CANIE0 | CAN0 error | Level | N | 263 |
| 95 | | CANIE1 | CAN1 error | Level | N | 264 |
| 96 | EtherCAT Slave (optional) | HWRTOS | HW-RTOS interrupt | Level | N | 253 |
| 97 | | ETHCSI0 | EtherCAT Sync0 interrupt | Level/Edge*3 | Y *4 | 73 |
| 98 | | ETHCSI1 | EtherCAT Sync1 interrupt | Level/Edge*3 | Y *4 | 74 |
| 99 | | ETHCI | EtherCAT interrupt | Level/Edge*2 | Y *4 | 75 |
| 100 | | ETHCSOFI | EtherCAT SOF interrupt | Edge | Y *4 | 76 |
| 101 | | ETHCEOFI | EtherCAT EOF interrupt | Edge | Y *4 | 77 |
| 102 | Ether MAC | - | Reserved | - | - | - |
| 103 | | ETHMMAI | Ether MII management access completion interrupt | Edge | Y *4 | 64 |
| 104 | | ETHPPIT | Ether pause packet transmission completed | Edge | Y *4 | 65 |
| 105 | | ETHIT | Ether transmission completed interrupt | Edge | Y *4 | 66 |
| 106 | Switch with IEEE1588 | ETHSWI | Ether SWITCH interrupt | Level/Edge*2 | Y *4 | 45 |
| 107 | | ETHSWDLRI | Ether SWITCH DLR interrupt | Level/Edge*2 | Y *4 | 46 |
| 108 | | ETHSWSOI | Ether SWITCH SYNCOUT interrupt | Edge | Y *4 | 47 |
| 109 | Ether MAC | ETHRFIV | RX FIFO overflow | Edge | N | 67 |
| 110 | | ETHTFIU | TX FIFO underflow | Edge | N | 68 |
| 111 | | ETHDMAIR | Ether MACDMA reception completed | Level/Edge*2 | Y *4 | 51 |
| 112 | | ETHDMAIT | Ether MACDMA transmission completed | Edge | Y *4 | 52 |
| 113 | | ETHRFI | Reception frame normal interrupt | Level/Edge*2 | Y *4 | 53 |
| 114 | | - | Reserved | - | - | - |
| 115 | | ETHTFIE | TX-FIFO error interrupt | Level | N | 69 |
| 116 | | ETHRFE | Ether reception frame error | Level | N | 70 |
| 117 | | ETHDRIE | MACDMA reception error interrupt | Edge | N | 246 |
| 118 | | ETHDTIE | MACDMA transmission error interrupt | Edge | N | 247 |
| 119 | | - | Reserved | - | - | - |
| 120 | EtherCAT slave (optional) | ETHCRSTI | EtherCAT RESET interrupt | Edge | N | 79 |
| 121 | | ETHCWDTI | EtherCAT WDT interrupt | Edge | N | 78 |

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[Current description]

Table 12.6 CM3 Interrupt Vector Table (4/4)

| Vector Number | Request Source | Source | | Detection Type | DMAC | DMAC setting vector Number |
|---|---|---|---|---|---|---|
| 122 | Ether MAC | ETHLPIST | LPI start notification interrupt from the MII | Edge | N | 71 |
| 123 | | ETHLPIEND | LPI end notification interrupt from the MII | Edge | N | 72 |
| 124 | RAM | ETHRSE1 | 1-bit ECC error interrupt from the on-chip extended SRAM *1 | Edge | N | - |
| 125 | | ETHRSE2 | 1-bit ECC error interrupt from the on-chip extended SRAM *1 | Edge | N | - |
| 126 | System | ETHCTO0 | CTI trigger output signal 0 | Edge | N | - |
| 127 | | ETHCTO1 | CTI trigger output signal 1 | Edge | N | - |

Note: Do not select the interrupt request destinations that do not have Y for the request destination.
Note 1. Only in products with extended on-chip SRAM.
Note 2. Select level detection when using this source to generate interrupts for the CPU and edge detection when using it as a trigger for DMA activation.
Note 3. Select the level or edge detection when using this source to generate interrupts for the CPU, and edge detection when using it as a trigger for DMA activation.

[Correct description】

Table 12.6 CM3 Interrupt Vector Table (4/4)

| Vector Number | Request Source | Source | | Detection Type | DMAC | DMAC setting vector Number |
|---|---|---|---|---|---|---|
| 122 | Ether MAC | ETHLPIST | LPI start notification interrupt from the MII | Edge | N | 71 |
| 123 | | ETHLPIEND | LPI end notification interrupt from the MII | Edge | N | 72 |
| 124 | RAM | ETHRSE1 | 1-bit ECC error interrupt from the on-chip extended SRAM *1 | Edge | N | - |
| 125 | | ETHRSE2 | 1-bit ECC error interrupt from the on-chip extended SRAM *1 | Edge | N | - |
| 126 | System | ETHCTO0 | CTI trigger output signal 0 | Edge | N | - |
| 127 | | ETHCTO1 | CTI trigger output signal 1 | Edge | N | - |

Note: Do not select the interrupt request destinations that do not have Y for the request destination.
Note 1. Only in products with extended on-chip SRAM.
Note 2. Select level detection when using this source to generate interrupts for the CPU and edge detection when using it as a trigger for DMA activation.
Note 3. Select the level or edge detection when using this source to generate interrupts for the CPU, and edge detection when using it as a trigger for DMA activation.
Note 4. DMA transfer completion interrupt is not generated and an interrupt is generated at the same time as DMA request. Check CHSTAT_n.END register for DMA transfer completion.