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RENESAS TECHNICAL UPDATE

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Product Category	MPU/MCU		Document No.	TN-RZ*-A0086A/E	Rev.	1.00
Title	RZ/G2M V1.3, V3.0 Additional Explanations for Pin Multiplex		Information Category	Technical Notification		
Applicable Product	RZ/G Series, 2nd Generation RZ/G2M V1.3, V3.0	Lot No. All lots	Reference Document	RZ/G Series, 2nd Generation User's Manual: Hardware Rev.1.10 Dedicated document for Pin Multiplex of RZ/G2M V1.3, V3.0 (EPMP-IMB-20-0058)		

This technical update describes document correction of RZ/G Series, 2nd Generation product.

[Summary]

Additional explanations for “RZ/G Series, 2nd Generation User's Manual: Rev.1.10 Dedicated document for Pin Multiplex of RZ/G2M.

[Priority level]

Importance: “Normal”

Urgency: “Normal”

[Products]

RZ/G2M V1.3, V3.0

[Section number and title]

(Dedicated document) Pin Multiplexing [RZ/G2M V1.3, V3.0]

“This is empty adjustment page to compare next Current (from) and Correction (to) on facing page. “

(By using two pages view of PDF readers this enables previously and prospectively view on odd and even pages.)

[Correction]

1. (Dedicated document) Pin Multiplexing [RZ/G2M V1.3, V3.0]

Current (from):

**:U32/U31, V5/V4, W2/W1 are shered function pin with I2C *:When you select the function of the multiplexed LSI pins, refer to setion 8 (PFC), Table 8.5 in RZ/G2 user's manual.

Pin location of FCBGA	#MODE	#GPIO	#Function0	#control of PFC(IPSR=H'0)*		#Function1	#control of PFC(IPSR=H'1)*		#Function2	#control of PFC(IPSR=H'2)*	
			Module	Pin Name	IO	Module	Pin Name	IO	Module	Pin Name	IO
V5		GP2_13	EtherAVB	AVB_AVTP_MATCH_A	O				MSIOF2	MSIOF2_RXD_C	I
V4		GP2_14	EtherAVB	AVB_AVTP_CAPTURE_A	I				MSIOF2	MSIOF2_TXD_C	O
			I2C5	SCL5	IO						
			I2C5	SDA5	IO						
W2		GP2_07	PWM1	PWM1_A	O						
W1		GP2_08	PWM2	PWM2_A	O						
			I2C3	SCL3	IO						
			I2C3	SDA3	IO						
U32		GP3_14	SDHI1	SD1_CD	I				NDFC	NFRB#_A	I
U31		GP3_15	SDHI1	SD1_WP	I				NDFC	NFCE#_A	O
			I2C0	SCL0	IO						
			I2C0	SDA0	IO						

Correction (to):

**:U32/U31, V5/V4, W2/W1 are shared function pin with I2C *:When you select the function of the multiplexed LSI pins, refer to setion 8 (PFC), Table 8.5 in RZ/G2 user's manual.

	Pin location of FCBGA	#MODE	#GPIO	#Function0	#control of PFC(IPSR=H'0)*		#Function1	#control of PFC(IPSR=H'1)*		#Function2	#control of PFC(IPSR=H'2)*	
				Module	Pin Name	IO	Module	Pin Name	IO	Module	Pin Name	IO
**	V5		GP2_13	EtherAVB	AVB_AVTP_MATCH_A	O				MSIOF2	MSIOF2_RXD_C	I
**	V4		GP2_14	EtherAVB	AVB_AVTP_CAPTURE_A	I				MSIOF2	MSIOF2_TXD_C	O
**				I2C5	SCL5	IO						
**				I2C5	SDA5	IO						
**	W2		GP2_07	PWM1	PWM1_A	O						
**	W1		GP2_08	PWM2	PWM2_A	O						
**				I2C3	SCL3	IO						
**				I2C3	SDA3	IO						
**	U32		GP3_14	SDHI1	SD1_CD	I				NDFC	NFRB#_A	I
**	U31		GP3_15	SDHI1	SD1_WP	I				NDFC	NFCE#_A	O
**				I2C0	SCL0	IO						
**				I2C0	SDA0	IO						

[Description]

**: U32/U31, V5/V4, W2/W1 are shared function pin with I2C.

[Reason for Correction]

General error correction.

End of Document -