Date: May 23, 2024

RENESAS TECHNICAL UPDATE

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Product Category	MPU/MCU		Document No.	TN-RZ*-A0079B/E	Rev.	2.00
Title	RZ/G2H, RZ/G2M V1.3, RZ/G2M V3.0, RZ/G2N and RZ/G2E Additional explanation for Electrical Characteristics		Information Category	Technical Notification		
Applicable Product	RZ/G Series, 2nd Generation RZ/G2H, G2M V1.3, G2M V3.0, G2N and G2E	Lot No. All lots	Reference Document	RZ/G Series, 2nd Generation User's Manual: Hardware Rev.1.01 (R01UH0808EJ0101)		

This technical update describes specification change of RZ/G Series, 2nd Generation product.

[Summary]

Additional explanation for “Hardware Electrical Characteristics Common to RZ/G Series, 2nd Generation products”.

[Priority level]

Importance: “Normal”

Urgency: “Normal”

[Products]

RZG2H

RZG2M V1.3

RZG2M V3.0

RZG2N

RZG2E

[Section number and title]

73.3 Sequence of Tuning On/Off Power Supplies

73.4 DC Characteristics

73.6 EXTAL Clock Input / output Timing [RZ/G2H] [RZ/G2M V1.3] [RZ/G2M V3.0] [RZ/G2N]

73.7 EXTAL Clock Input / output Timing [RZ/G2E]

[Remarks]

The content corrected in this TU is written in red characters, and the content corrected in the conventional TU is written in dark blue.

“This is empty adjustment page to compare next Current (from) and Correction (to) on facing page. “

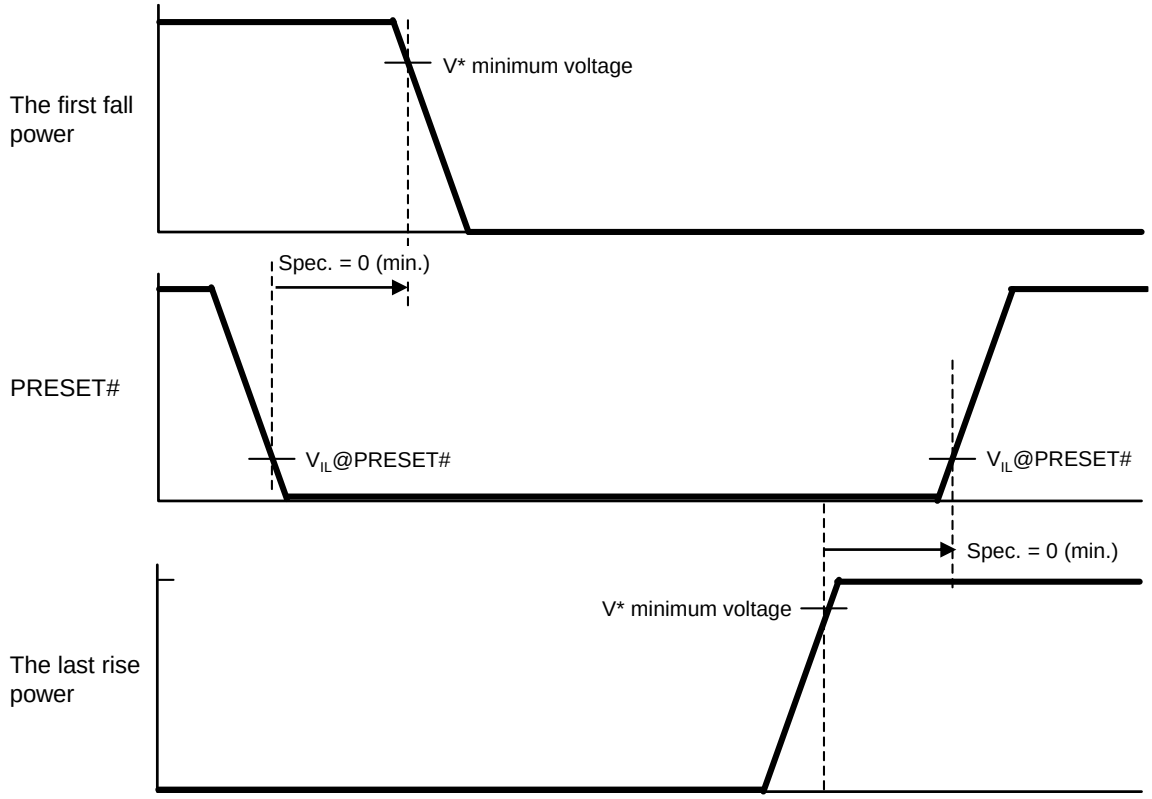
(By using two pages view of PDF readers this enables previously and prospectively view on odd and even pages.)

[Correction]

1. Section 73.3 Sequence of Tuning On/Off Power Supplies, Page 73-10, 73.3.1 Sequence of Turning On/Off Power Supplies for [RZ/G2H] [RZ/G2M V1.3] [RZ/G2M V3.0] [RZ/G2N]. (1) PRESET# VS. Power

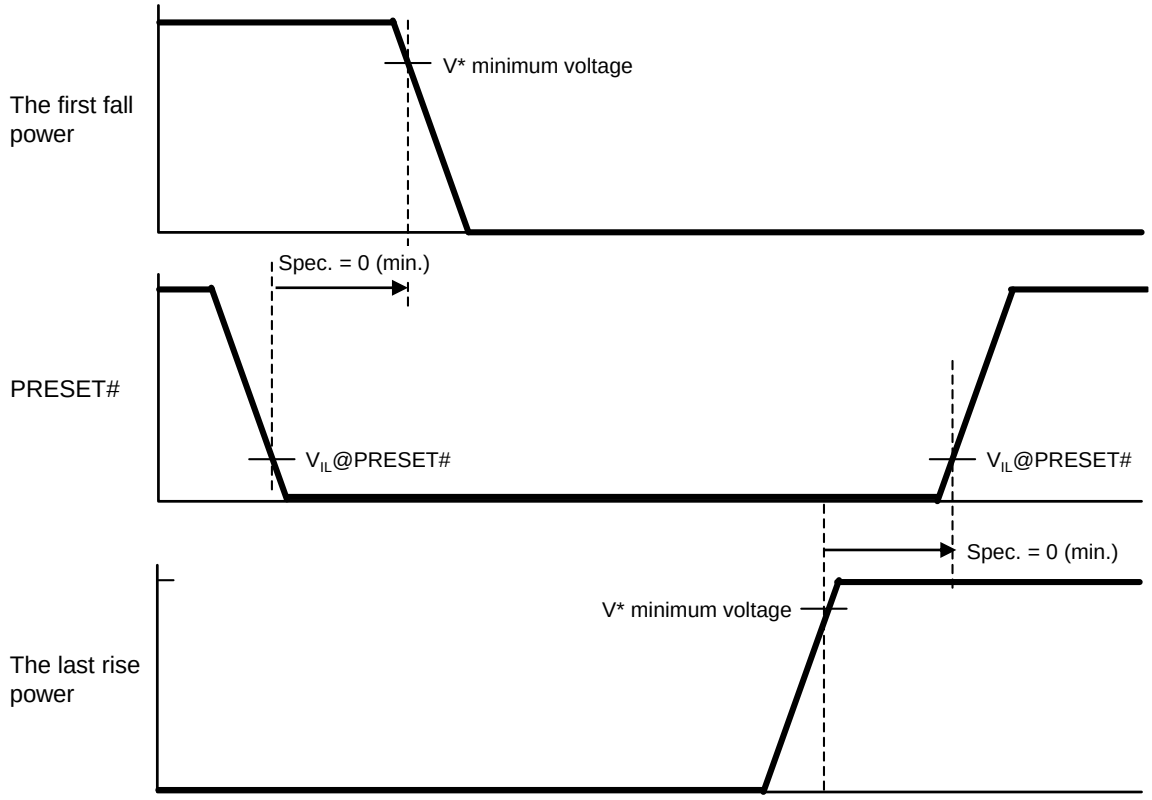
Current (from):

(1) PRESET# VS. Power



Correction (to):

(1) PRESET# VS. Power [RZ/G2H］[RZ/G2M V1.3] [RZ/G2M V3.0] [RZ/G2N]



Note that at power-on reset, refer to the specifications shown in section 73.5 “Clock and Reset Timings”.

Figure 73.3.1.1 PRESET# VS. Power [RZ/G2H] [RZ/G2M V1.3] [RZ/G2M V3.0] [RZ/G2N]

[Description]

Added figure number and figure title.

[Reason for Correction]

General error correction

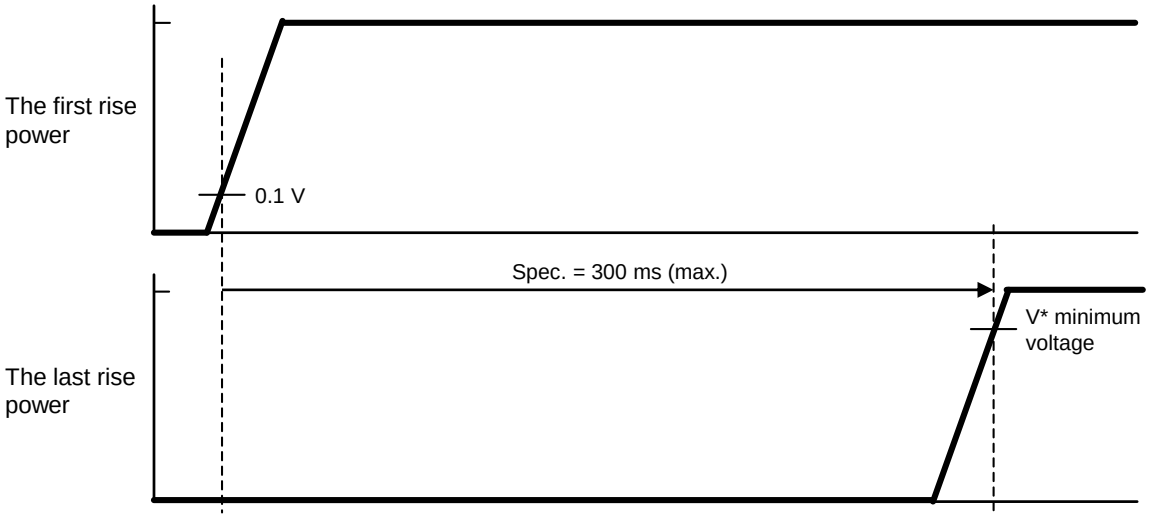
[Reference document]

None

2. Section 73.3 Sequence of Tuning On/Off Power Supplies, Page 73-11, 73.3.1 Sequence of Turning On/Off Power Supplies for [RZ/G2H] [RZ/G2M V1.3] [RZ/G2M V3.0] [RZ/G2N]. (2) Period for Power Rise for RZ/G2H, RZ/G2M V1.3, RZ/G2N

Current (from):

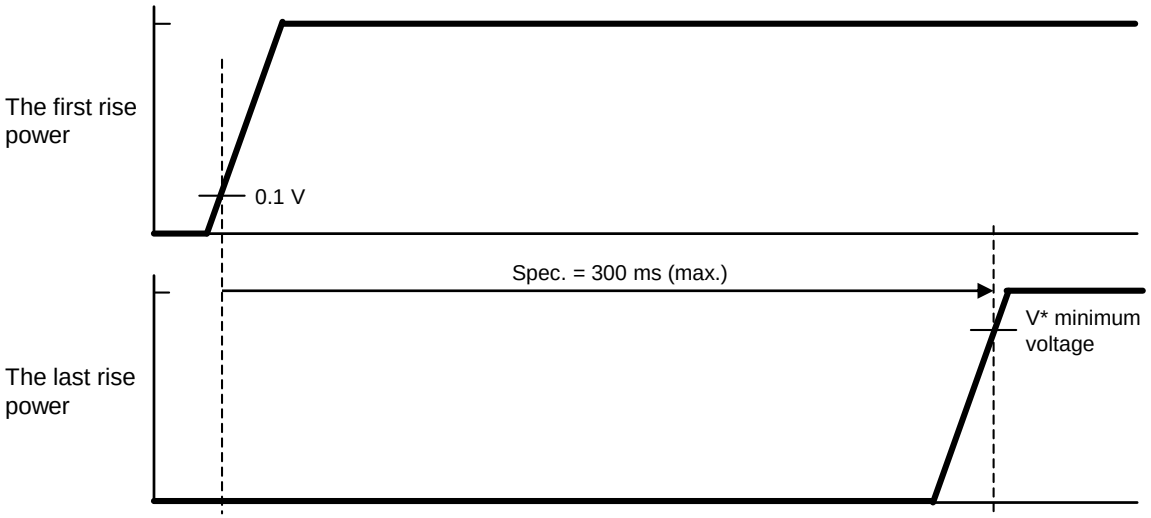
(2) Period for Power Rise for RZ/G2H, RZ/G2M V1.3, RZ/G2N



For all V*, power off state must be 0 V (GND), power rising must be started from 0 V, and end to 0 V respectively. (excluding DDR-SDRAM power-supply backup state)
Period from 0 V to 0.1V at power-on and from 0.2 V to 0 V at power-off should be shorten as much as possible.

Correction (to):

(2) Period for Power Rise for [RZ/G2H] [RZ/G2M V1.3] [RZ/G2M V3.0] [RZ/G2N]



For all V*, power off state must be 0 V (GND), power rising must be started from 0 V, and end to 0 V respectively. (excluding DDR-SDRAM power-supply backup state)
Period from 0 V to 0.1V at power-on and from 0.2 V to 0 V at power-off should be shorten as much as possible.

Figure 73.3.1.2 Period for Power Rise for [RZ/G2H] [RZ/G2M V1.3] [RZ/G2M V3.0] [RZ/G2N]

[Description]

Added figure number and figure title.

[Reason for Correction]

General error correction

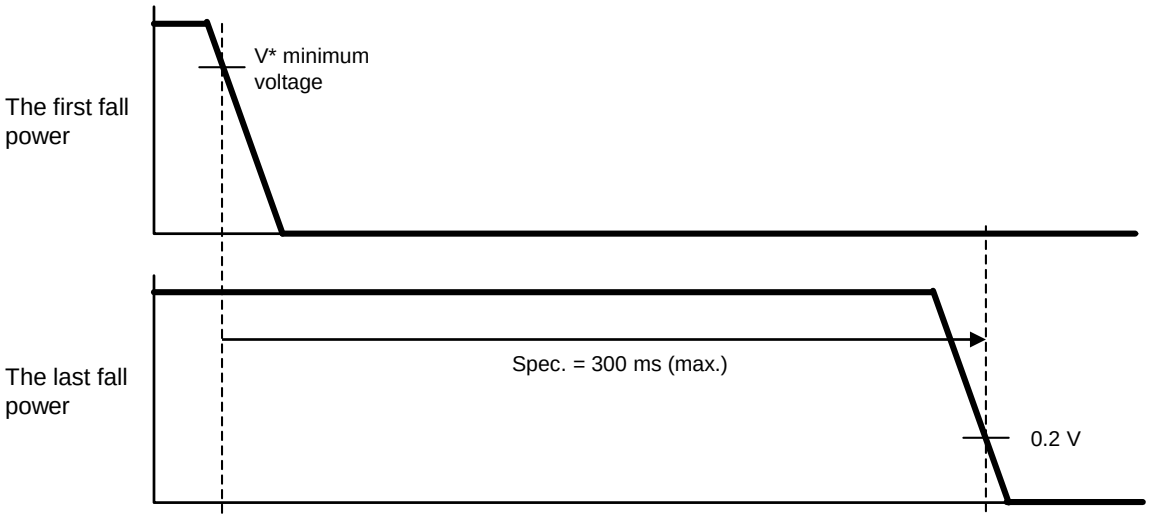
[Reference document]

None

3. Section 73.3 Sequence of Tuning On/Off Power Supplies, Page 73-12, 73.3.1 Sequence of Turning On/Off Power Supplies for [RZ/G2H] [RZ/G2M V1.3] [RZ/G2M V3.0] [RZ/G2N]. (3) Period for Power Fall for RZ/G2H, RZ/G2M V1.3, RZ/G2N

Current (from):

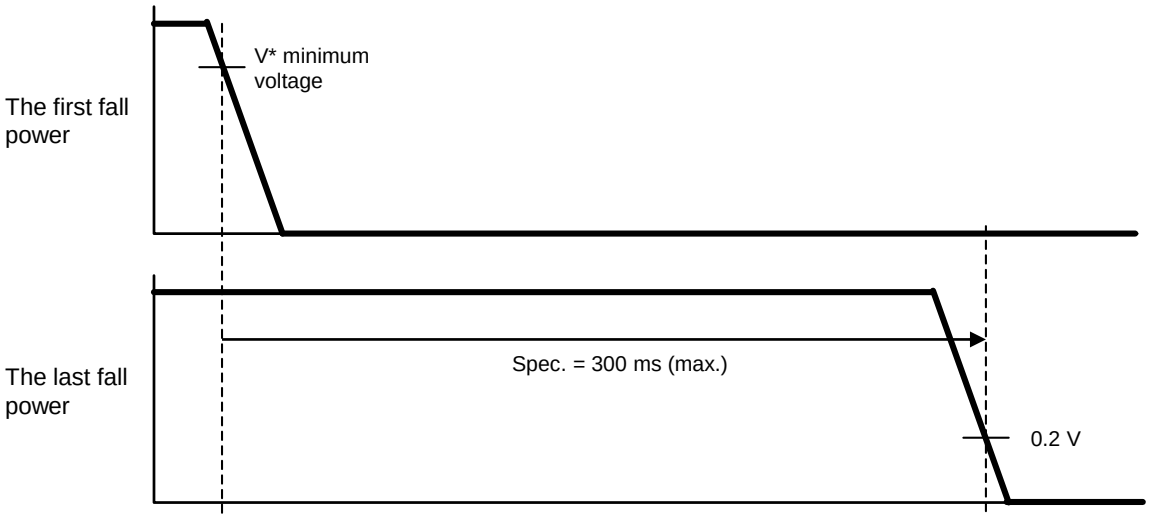
(3) Period for Power Fall for RZ/G2H, RZ/G2M V1.3, RZ/G2N



For all V*, power off state must be 0 V (GND), power rising must be started from 0 V, and end to 0 V respectively. (excluding DDR-SDRAM power-supply backup state)
Period from 0 V to 0.1V at power-on and from 0.2 V to 0 V at power-off should be shorten as much as possible.

Correction (to):

(3) Period for Power Fall for [RZ/G2H] [RZ/G2M V1.3] [RZ/G2M V3.0] [RZ/G2N]



For all V*, power off state must be 0 V (GND), power rising must be started from 0 V, and end to 0 V respectively. (excluding DDR-SDRAM power-supply backup state)
Period from 0 V to 0.1V at power-on and from 0.2 V to 0 V at power-off should be shorten as much as possible.

Figure 73.3.1.3 Period for Power Fall for [RZ/G2H] [RZ/G2M V1.3] [RZ/G2M V3.0] [RZ/G2N]

[Description]

Added figure number and figure title.

[Reason for Correction]

General error correction

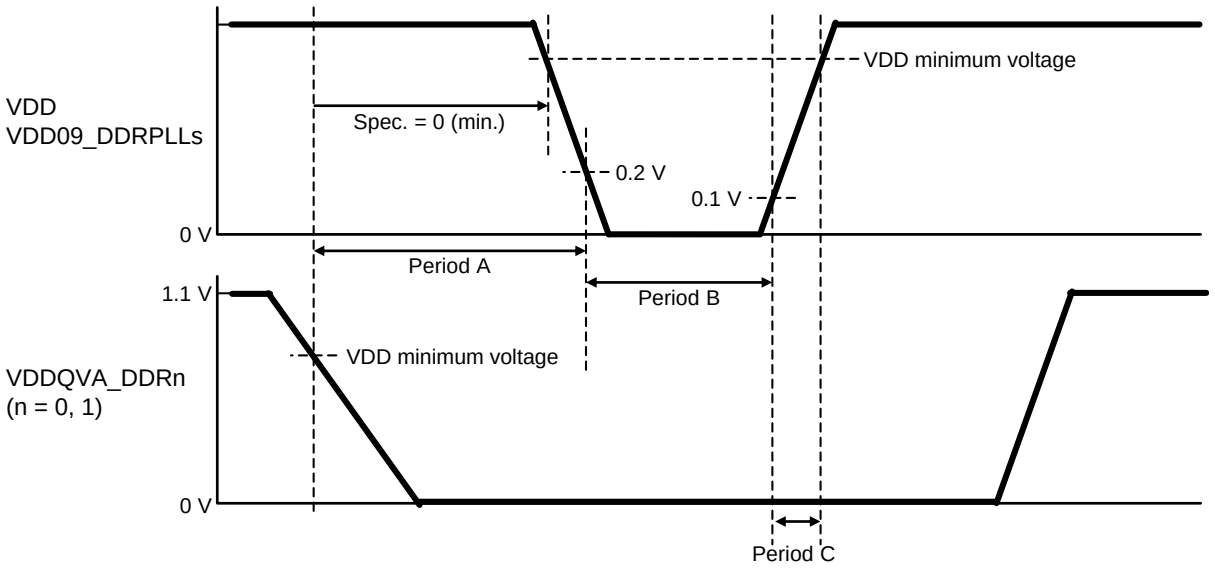
[Reference document]

None

4. Section 73.3 Sequence of Tuning On/Off Power Supplies, Page 73-13, 73.3.1 Sequence of Turning On/Off Power Supplies for [RZ/G2H] [RZ/G2M V1.3] [RZ/G2M V3.0] [RZ/G2N]. (4) VDD and VDD09_DDRPLLs vs VDDQVA_DDRn (n = 0, 1) for RZ/G2H, RZ/G2M V1.3, RZ/G2M V3.0, RZ/G2N

Current (from):

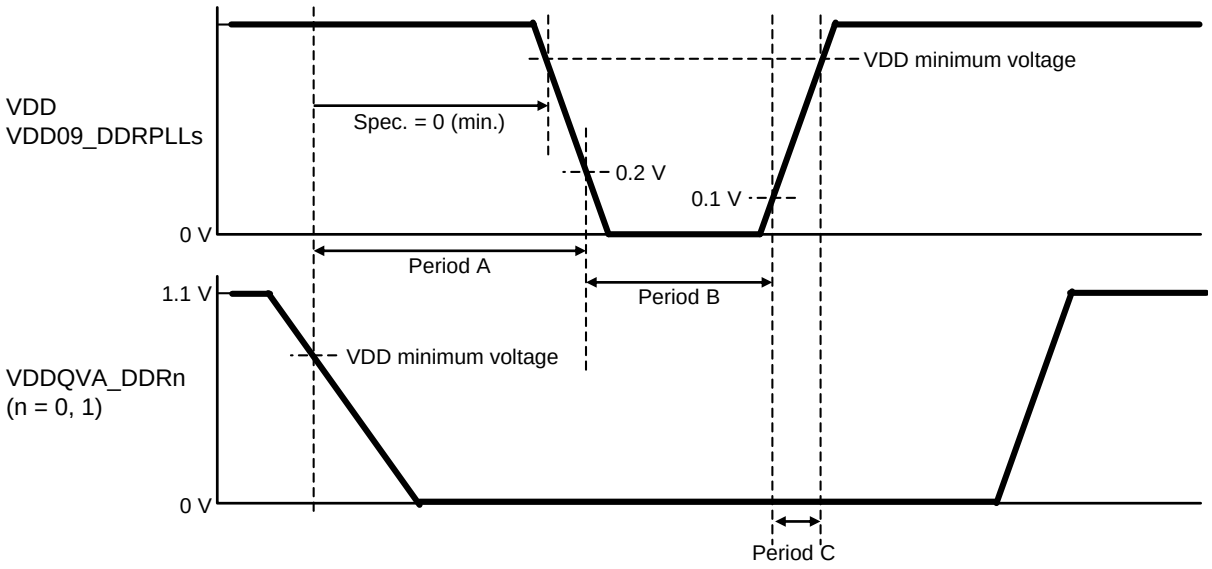
(4) VDD and VDD09_DDRPLLs vs VDDQVA_DDRn (n = 0, 1)



VDD and VDD09_DDRPLLs must be greater than VDDQVA_DDRn (n = 0, 1) for Period A.
VDDQVA_DDRn (n = 0, 1) must be off for Period B.
VDD and VDD09_DDRPLLs must be greater than VDDQVA_DDRn (n = 0, 1) for Period C.
VDD09_DDRPLLs are VDD09_DDRPLLnm (n = 0-3, m = CA, DQ01, DQ23)

Correction (to):

(4) VDD and VDD09_DDRPLLs vs VDDQVA_DDRn (n = 0, 1) [RZ/G2H] [RZ/G2M V1.3] [RZ/G2M V3.0] [RZ/G2N]



VDD and VDD09_DDRPLLs must be greater than VDDQVA_DDRn (n = 0, 1) for Period A.
VDDQVA_DDRn (n = 0, 1) must be off for Period B.
VDD and VDD09_DDRPLLs must be greater than VDDQVA_DDRn (n = 0, 1) for Period C.
VDD09_DDRPLLs are VDD09_DDRPLLnm (n = 0-3, m = CA, DQ01, DQ23)

Figure 73.3.1.4 VDD and VDD09_DDRPLLs vs VDDQVA_DDRn (n = 0, 1) [RZ/G2H] [RZ/G2M V1.3] [RZ/G2M V3.0] [RZ/G2N]

[Description]

Added figure number and figure title.

[Reason for Correction]

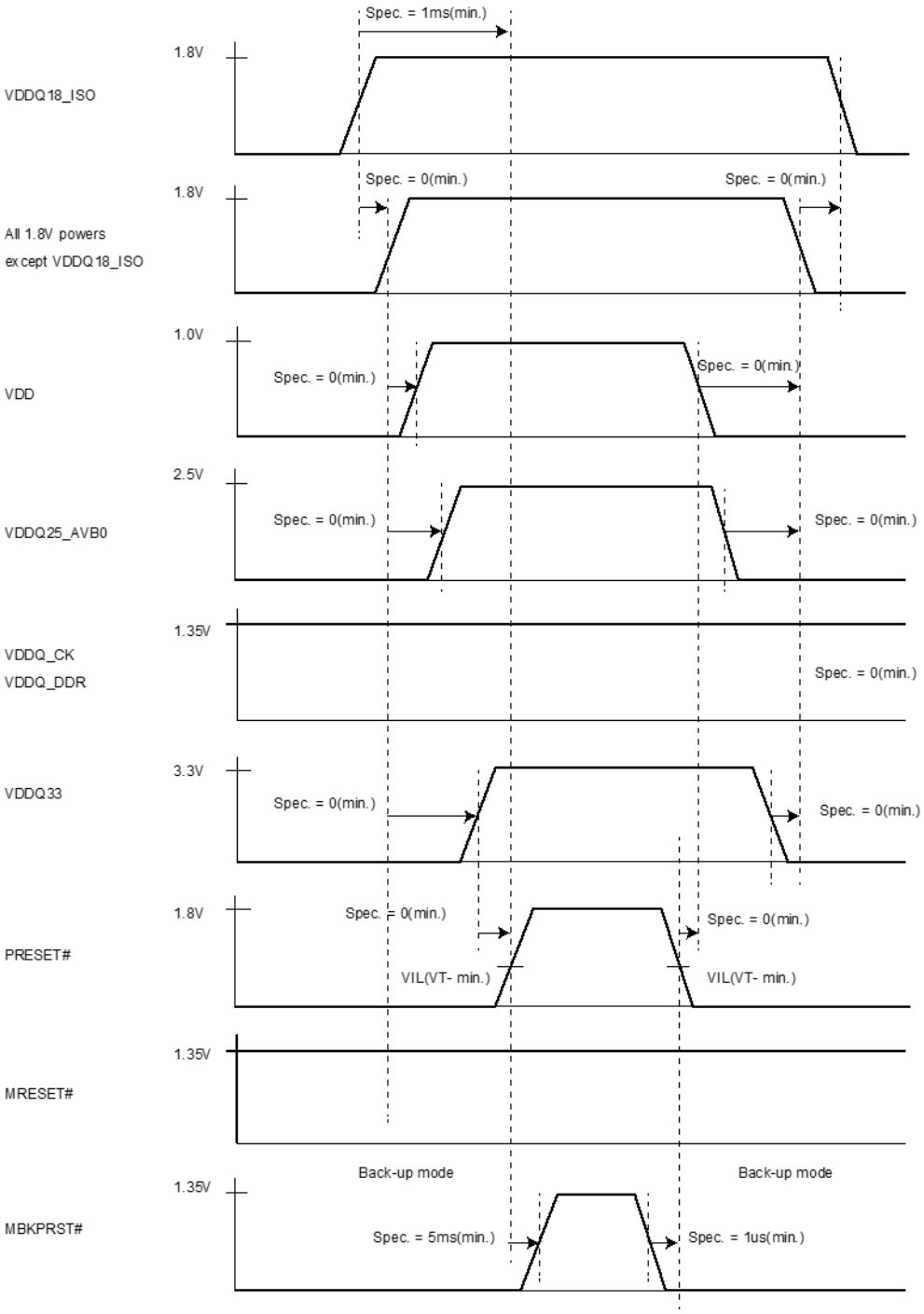
General error correction

[Reference document]

None

5. 73.3 Sequence of Turning On/Off Power Supplies, Page 73-14, 73.3.2 Sequence of Turning On/Off Power Supplies for [RZ/G2E]. (1) RZ/G2E power-up/down sequence with DDR backup. Notes of Figure are corrected.

Current (from):



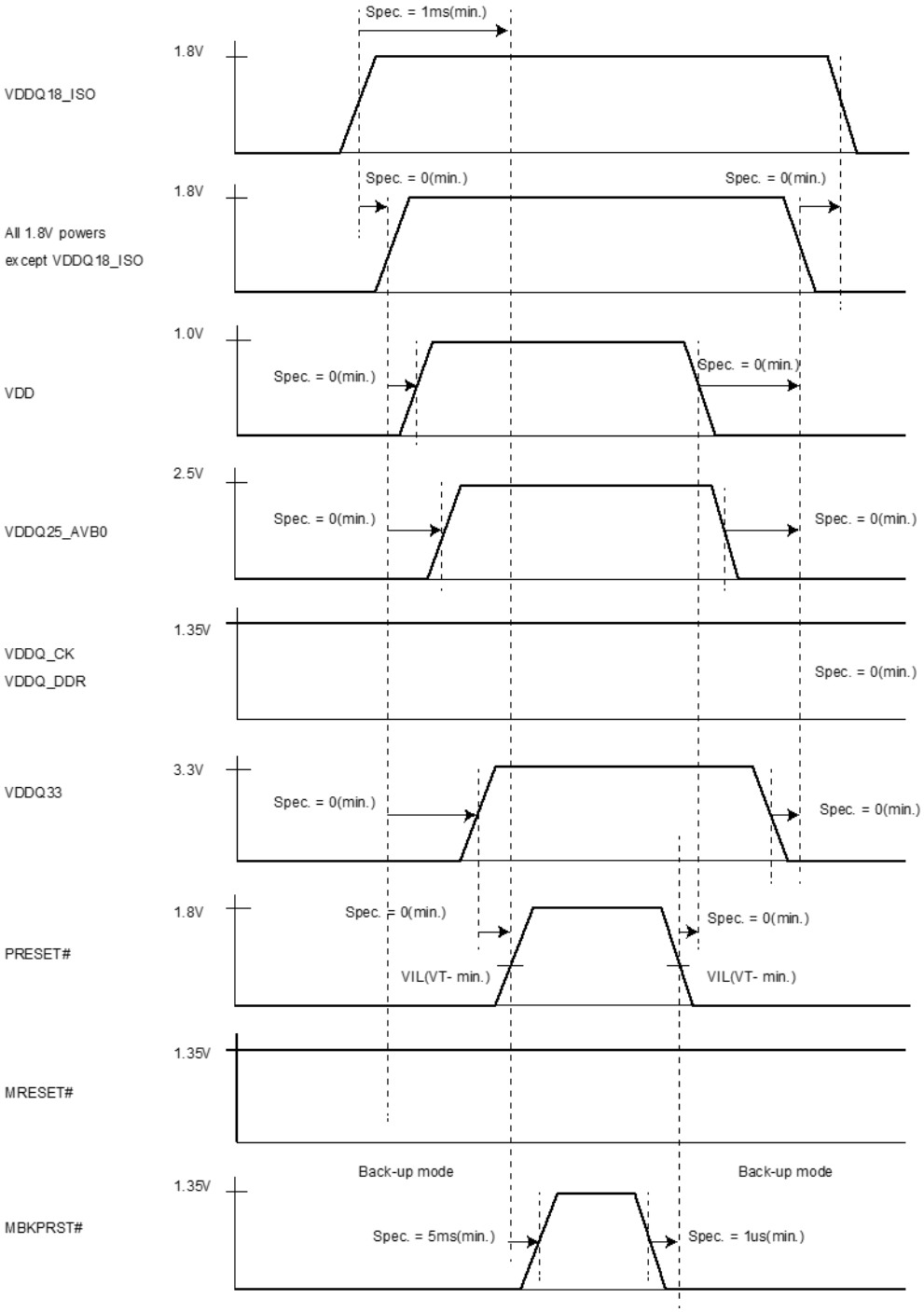
Note: Maximum time from first power rising to last power rising is 300ms.

Maximum time from first power failing to last power failing is 300ms.

Notes that the MBKPRST# must be asserted for 5 ms or more for the PRESET# tOSC specification at a power-on reset.

Even when DDR backup mode is used, the first power up sequence must keep the sequence "RZ/G2E power-up/down sequence without DDR backup"

Correction (to):



Note: Refer to Figure 73.3.4.1 for the maximum time from first power rising(falling) to last power rising(falling).

Note that at power-on reset, refer to the specifications shown in section 73.5 “Clock and Reset Timings”.

Even when DDR backup mode is used, the first power up sequence must keep the sequence “RZ/G2E power-up/down sequence without DDR backup”.

Figure 73.3.2.1 power-up/down sequence with DDR backup [RZ/G2E]

[Description]

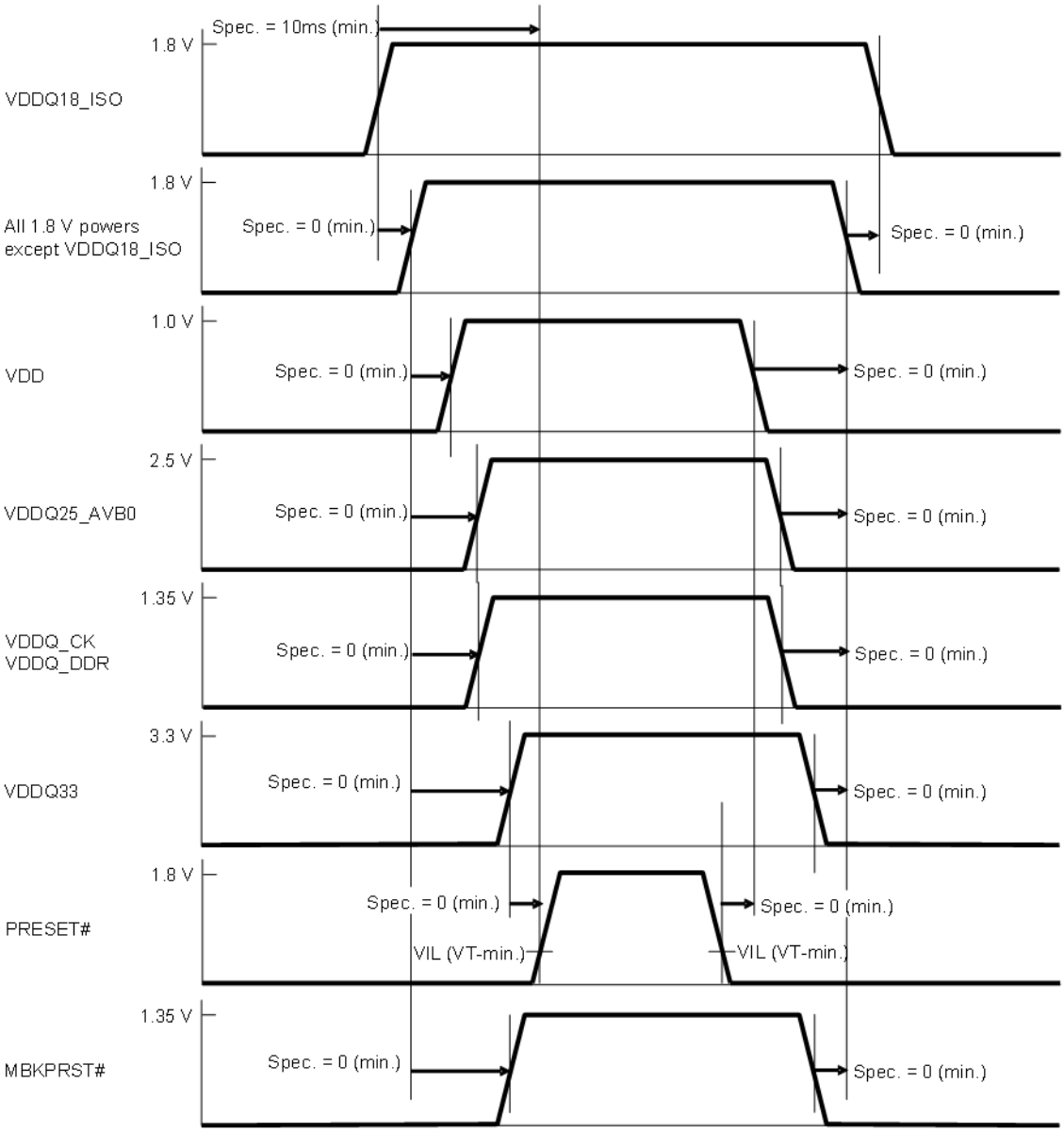
Change notes to refer to the section that defines the specification.

[Reason for Correction]

General error correction

6. 73.3 Sequence of Turning On/Off Power Supplies, Page 73-15, 73.3.2 Sequence of Turning On/Off Power Supplies for [RZ/G2E]. (2) RZ/G2E power-up/down sequence without DDR backup. Figure of Note are corrected.

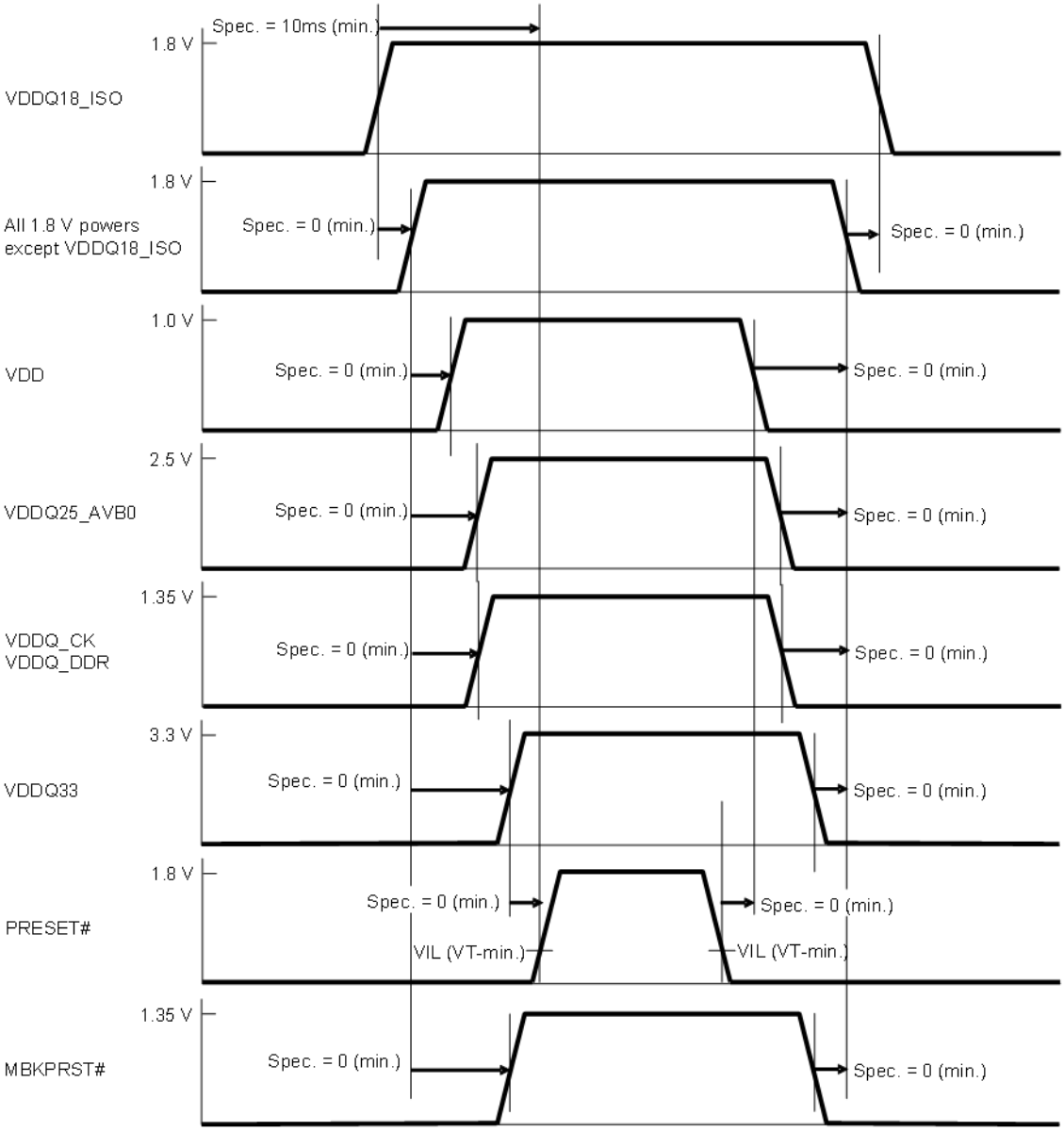
Current (from):



Notes: 1. Maximum time from first power rising to last power rising is 300ms.
Maximum time from first power failing to last power failing is 300ms.
Notes that the PRESET# must be asserted for 5 ms or more for the PRESET# tOSC specification at a power-on reset.

2. MBKPRST# input must track VDDQ_DDR/VDDQ_CK during VDDQ_DDR/VDDQ_CK power-up.

Correction (to):



Notes: 1. Refer to Figure 73.3.4.1 for the maximum time from first power rising(falling) to last power rising(falling).
Note that at power-on reset, refer to the specifications shown in section 73.5 “Clock and Reset Timings”.

2. MBKPRST# input must track VDDQ_DDR/VDDQ_CK during VDDQ_DDR/VDDQ_CK power-up.

Figure 73.3.2.2 power-up/down sequence without DDR backup [RZ/G2E]

[Description]

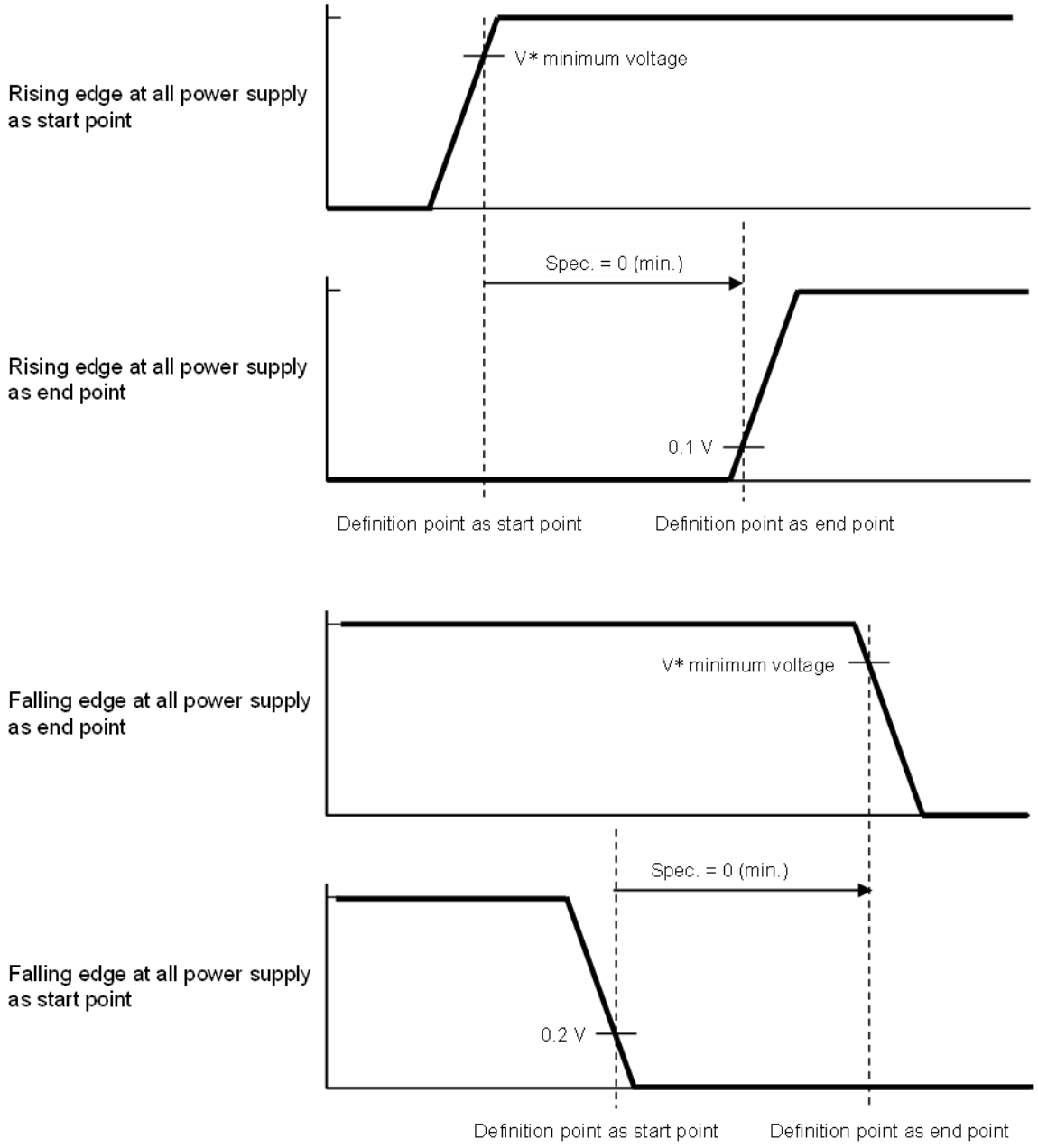
Change notes to refer to the section that defines the specification.

[Reason for Correction]

General error correction

7. 73.3 Sequence of Turning On/Off Power Supplies, Page 73-16, 73.3.3 Wave form definition for power sequence [RZ/G2E]

Current (from):



Correction (to):

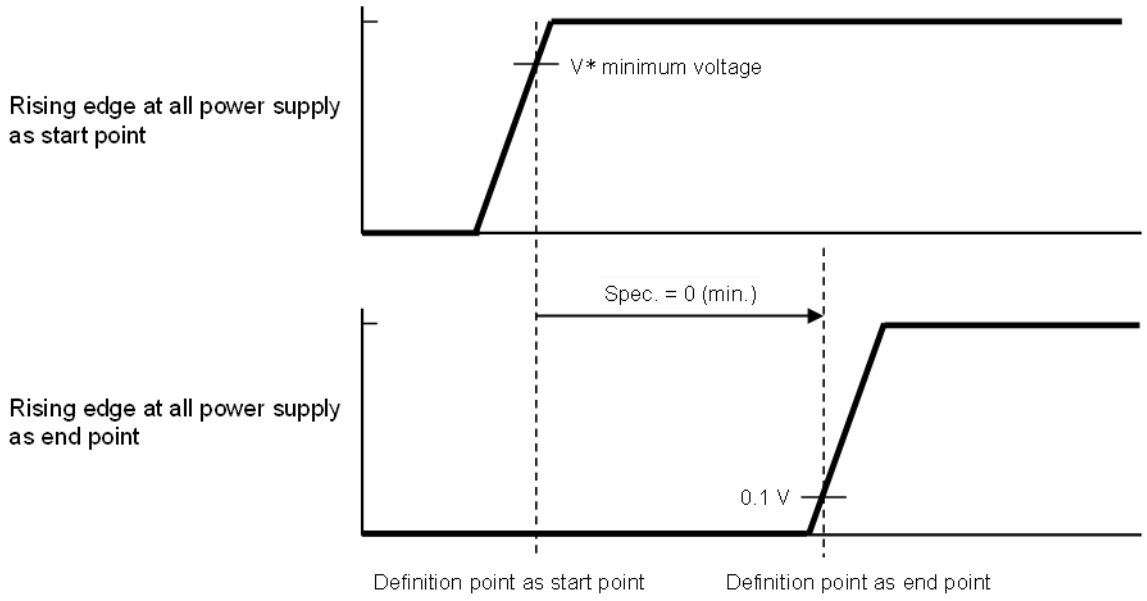


Figure 73.3.3.1 Period for Power Rise for [RZ/G2E]

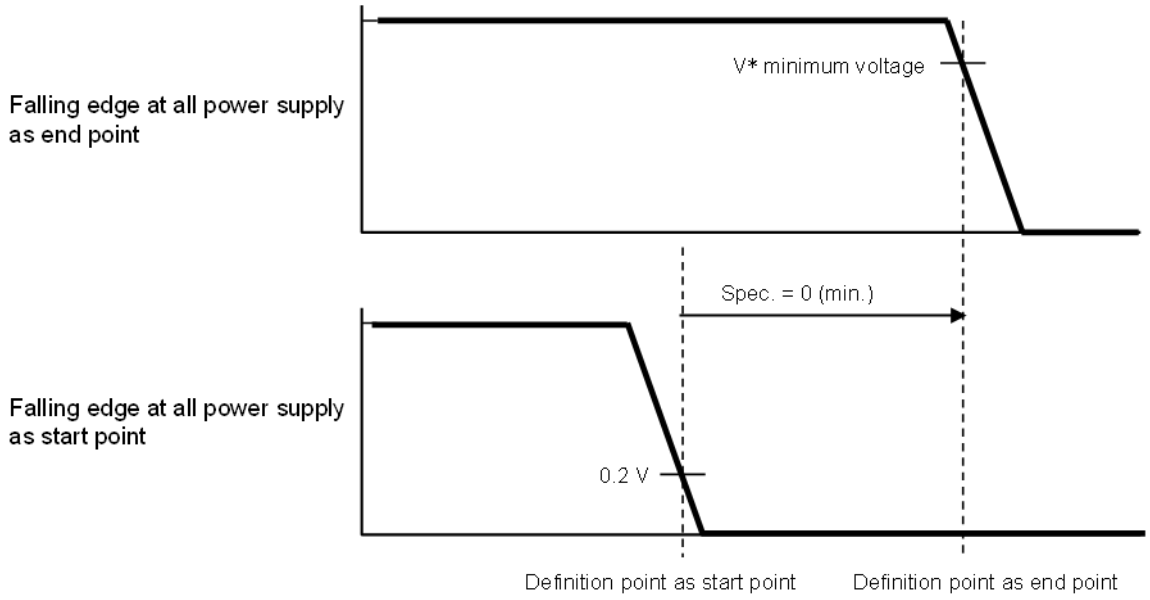


Figure 73.3.3.2 Period for Power Fall for [RZ/G2E]

[Description]

Added figure number and figure title.

[Reason for Correction]

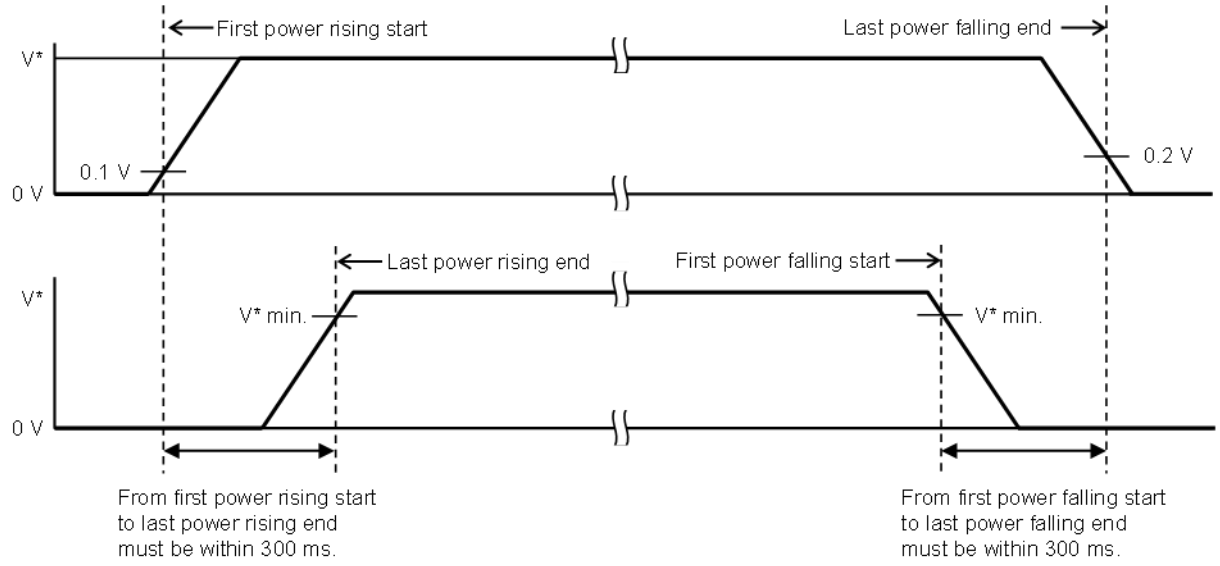
General error correction

[Reference document]

None

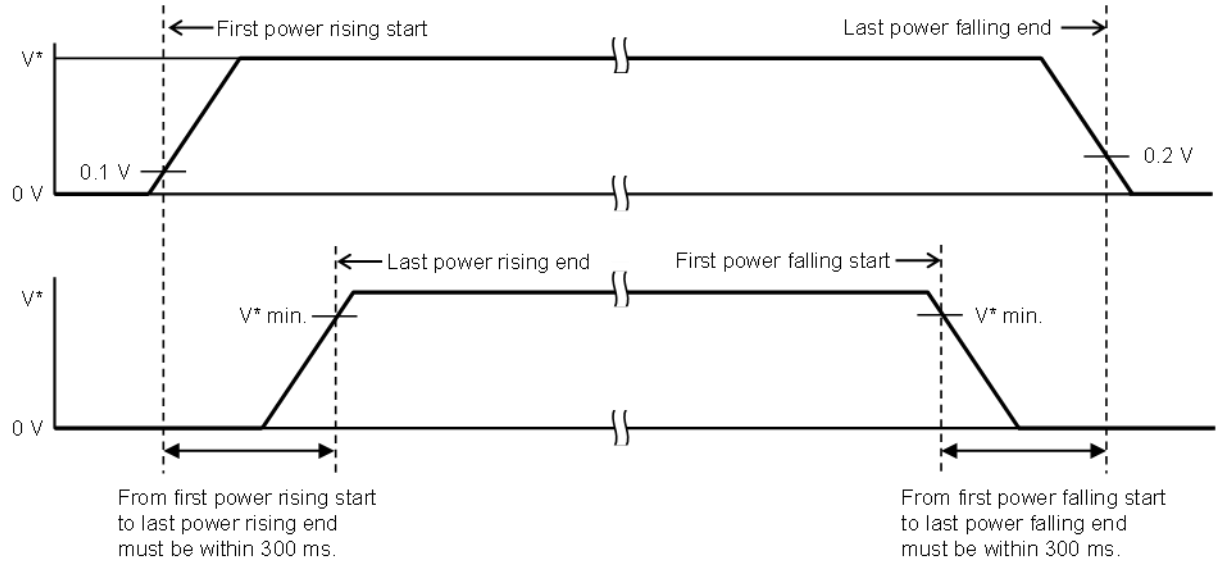
9. 73.3 Sequence of Turning On/Off Power Supplies, Page 73-17, 73.3.4 Power On and Power Off Wave Form [RZ/G2E]

Current (from):



Note: For all V*, power off state must be 0 V (GND), power rising must be started from 0 V and power falling must be ended to 0 V (excluding DDR-SDRAM power-supply backup state).
Periods from 0 V to 0.1 V at power-on and from 0.2 V to 0 V at power-off should be shortened as much as possible.

Current (to):



Note: For all V*, power off state must be 0 V (GND), power rising must be started from 0 V and power falling must be ended to 0 V (excluding DDR-SDRAM power-supply backup state).
Periods from 0 V to 0.1 V at power-on and from 0.2 V to 0 V at power-off should be shortened as much as possible.

Figure 73.3.4.1 Power On and Power Off Wave Form [RZ/G2E]

[Description]

Added figure number and figure title.

[Reason for Correction]

General error correction

[Reference document]

None

10. Section 73.6 EXTAL Clock Input / output Timing, Page 73-46, New section of EXTAL Crystal resonator Input characteristics.

Current (from):

— (Note define)

Correction (to):

73.6.3 EXTAL Crystal resonator Input characteristics [RZ/G2H] [RZ/G2M V1.3] [RZ/G2M V3.0]

Table 73.6.3 EXTAL Crystal resonator Input characteristic [RZ/G2H] [RZ/G2M V1.3] [RZ/G2M V3.0] [RZ/G2N]

Conditions: VDDQ18 = 1.8 V ± 0.1 V, GND = VSS = 0 V,
Tc = -40 to +115 °C [RZ/G2H, RZ/G2M V1.3], Ta = -40 to +85 °C [RZ/G2M V3.0, RZ/G2N],
Tj = -40 to +115 °C [RZ/G2M V3.0, RZ/G2N]
MD9 pin to High

Item		Symbol	Min.	Typ.	Max.	Unit	Remarks
Input Frequency Range	MD[14:13] = LL	fEXC	—	16.66	—	MHz	Frequency deviation : ±200 ppm or less
	MD[14:13] = LH		—	20.00	—		
	MD[14:13] = HL		—	25.00	—		
	MD]14:13] = HH		—	33.33	—		
Crystal oscillator stabilization time		T	—	—	5 *	ms	Refer Symbol T in Figure 73.5.1.

Note: * The oscillation stabilization time differs according to the matching with the external resonator circuit.
For proper operation of some external modules/devices/interfaces, a tighter frequency deviation might be needed. Input a fitting frequency deviation according to all external modules/devices/interfaces which are used.

[Description]

EXTAL Crystal resonator Input characteristics.

[Reason for Correction]

Extension

[Reference document]

None

11. Section 73.7 EXTAL Clock Input / output Timing, Page 73-47, New section of EXTAL Crystal resonator Input characteristics.

Current (from):

— (Note define)

Correction (to):

73.7.2 EXTAL Crystal resonator Input characteristics [RZ/G2E]

Table 73.7.2 EXTAL Crystal resonator Input characteristic [RZ/G2E]

Conditions: VDDQ18 = 1.8 V ± 0.1 V, GND = VSS = 0 V,
Ta = -40 to +85 °C, Tj = -40 to +115 °C,
MD9 pin to High

Item	Symbol	Min.	Typ.	Max.	Unit	Remarks
Input Frequency Range (with USB)	fEXC	—	48.00	—	MHz	Frequency deviation: ±100 ppm or less
Input Frequency Range (without USB)		—	48.00	—		Frequency deviation: ±200 ppm or less
Crystal oscillator stabilization time	T	—	—	5 *	ms	Refer Symbol T in Figure 73.5.1.

Note: * The oscillation stabilization time differs according to the matching with the external resonator circuit.
For proper operation of some external modules/devices/interfaces, a tighter frequency deviation might be needed. Input a fitting frequency deviation according to all external modules/devices/interfaces which are used.

[Description]

EXTAL Crystal resonator Input characteristics.

[Reason for Correction]

Extension

[Reference document]

None.

- End of Document -