Date: Apr. 23, 2024

RENESAS TECHNICAL UPDATE

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Renesas Electronics Corporation

Product Category	MPU/MCU		Document No.	TN-RZ*-A0131A/E	Rev.	1.00
Title	RZ/G2H, G2M V1.3, G2M V3.0, G2N and G2E Correction of section 36. Display Unit (DU)		Information Category	Technical Notification		
Applicable Product	RZ/G Series, 2nd Generation RZ/G2H RZ/G2M V1.3, V3.0 RZ/G2N RZ/G2E	Lot No. All lots	Reference Document	RZ/G Series, 2nd Generation User's Manual: Hardware Rev.1.11 (R01UH0808EJ0111)		

This technical update describes document correction of RZ/G Series, 2nd Generation product.

[Summary]

Correct the Block Diagram of section 36. Display Unit (DU) to show that FIFO can be selected from each DU channel.

[Priority level]

Importance: “Normal”

Urgency: “Normal”

[Products]

RZ/G2H

RZ/G2M V1.3, V3.0

RZ/G2N

RZ/G2E

[Section number and title]

Section 36. Display Unit (DU)

“This is empty adjustment page to compare next Current (from) and Correction (to) on facing page. “

(By using two pages view of PDF readers this enables previously and prospectively view on odd and even pages.)

[Correction]

1. Section 36. Display Unit (DU), Page 36-4 to 36-6, 36.1.2 Block Diagram, Correct block diagrams.

Current (from):

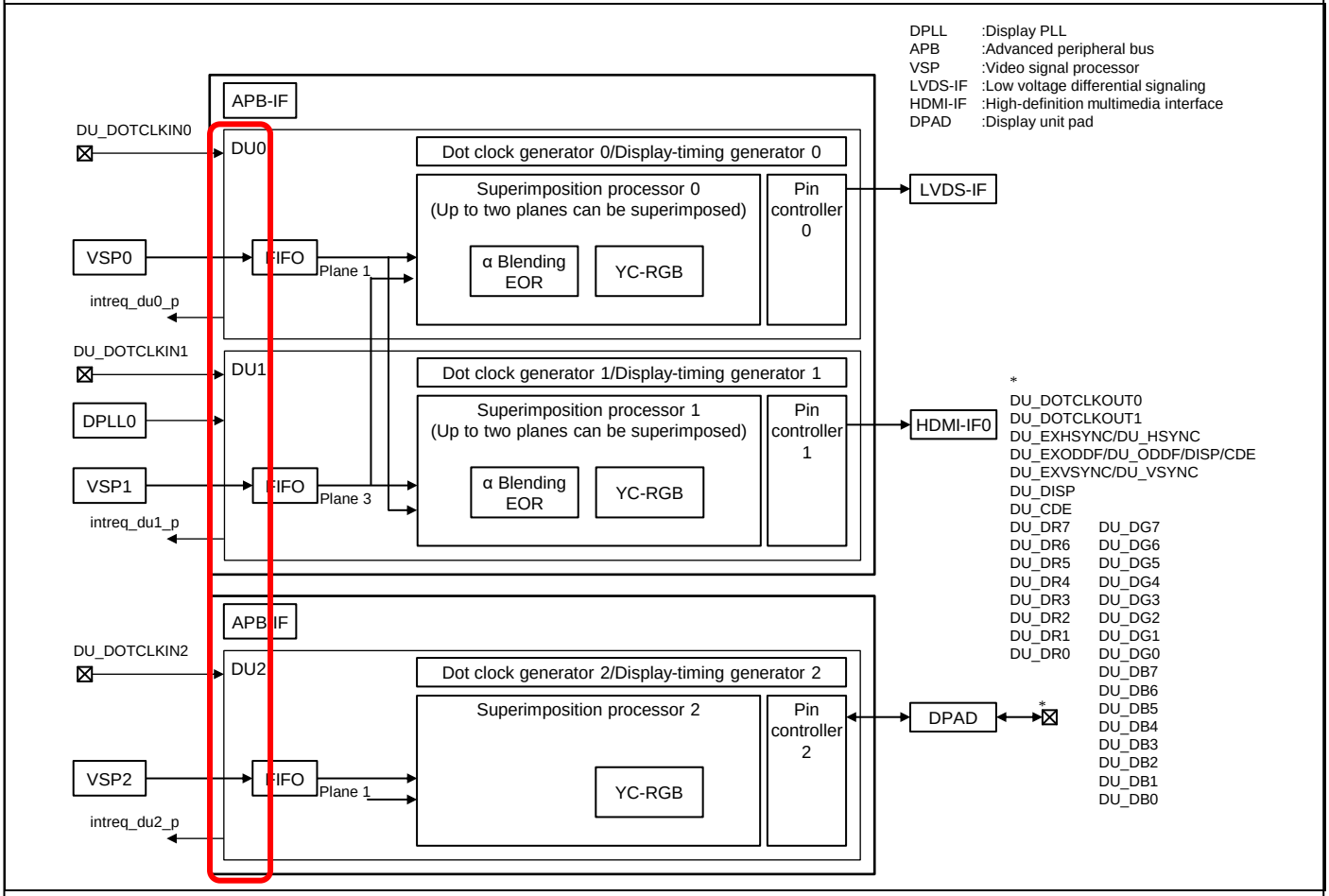


Figure 36.1 Block Diagram of the DU [RZ/G2M V1.3, RZ/G2M V3.0]

Correct (to):

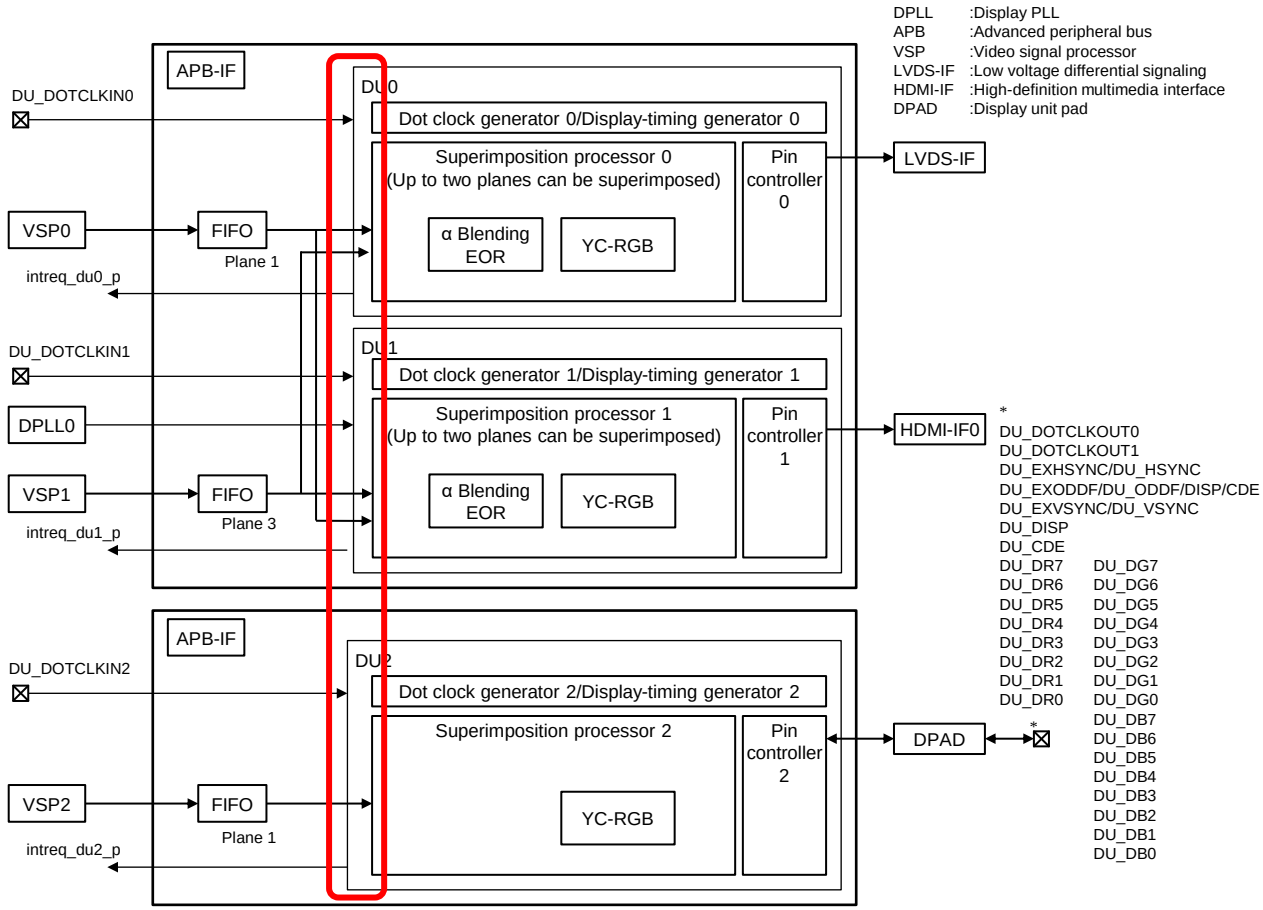


Figure 36.1 Block Diagram of the DU [RZ/G2M V1.3, RZ/G2M V3.0]

[Description]

In the RZ/G2M V1.3, G2M V3.0 system, where the images of VSPD0 and VSPD1 are α blended using DU0, DU1 is not used, but DU1 is also running because the FIFO connected to VSPD1 is in DU1. Since DU0 and DU1 interrupts were used, the interrupt processing changed due to the dot clock frequency difference between DU0 and DU1, and FPS decreased.

[Reason for Correction]

The FIFO can be selected from the DIDSR0 register, but in the current Block Diagram, the FIFO appears to be fixed in DU0 or DU1 and is recognized as not being selectable. DU2 is fixed, but it will be modified to align the notation. Remove unnecessary arrows.

Current (from):

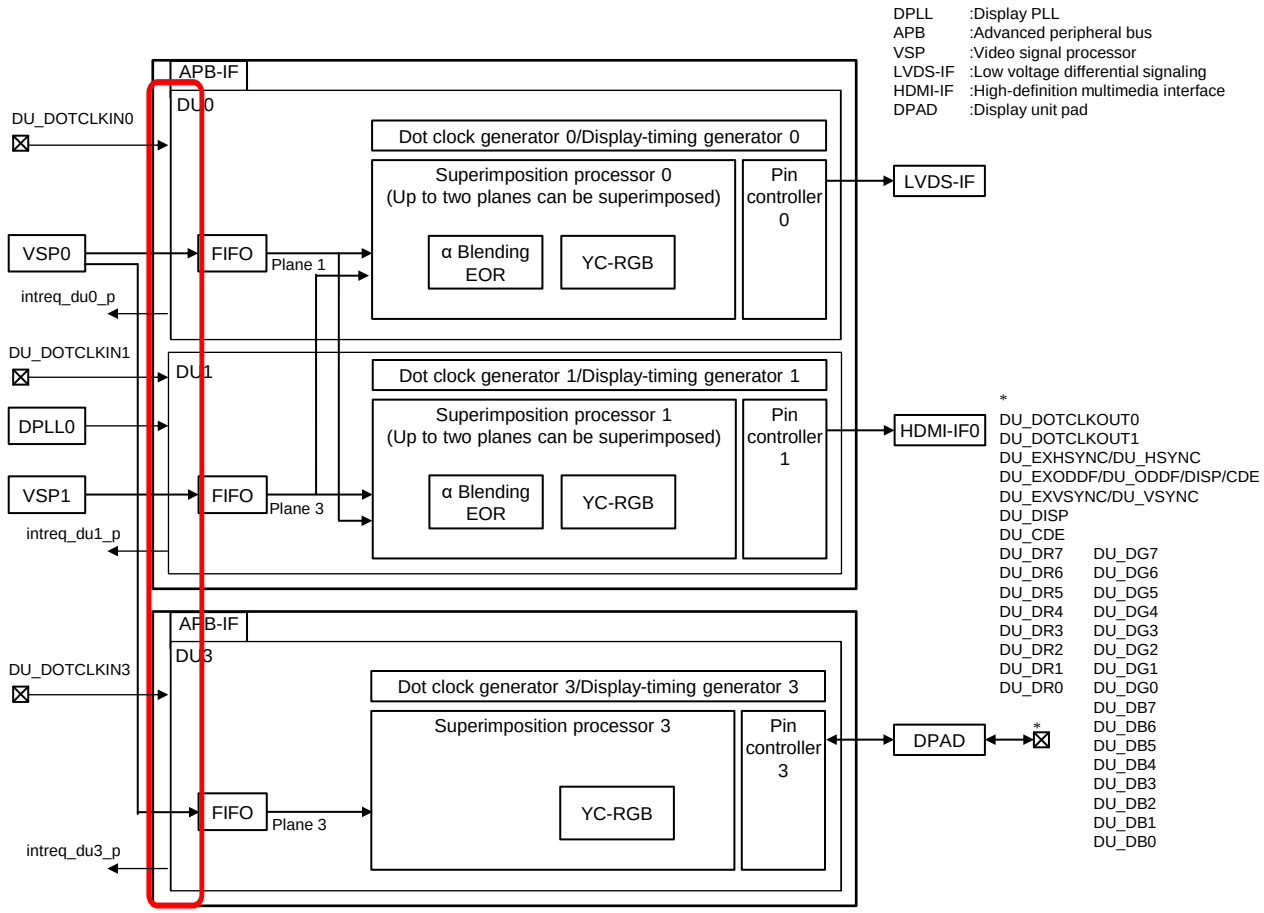


Figure 36.2 Block Diagram of the DU [RZ/G2H, RZ/G2N]

Correct (to):

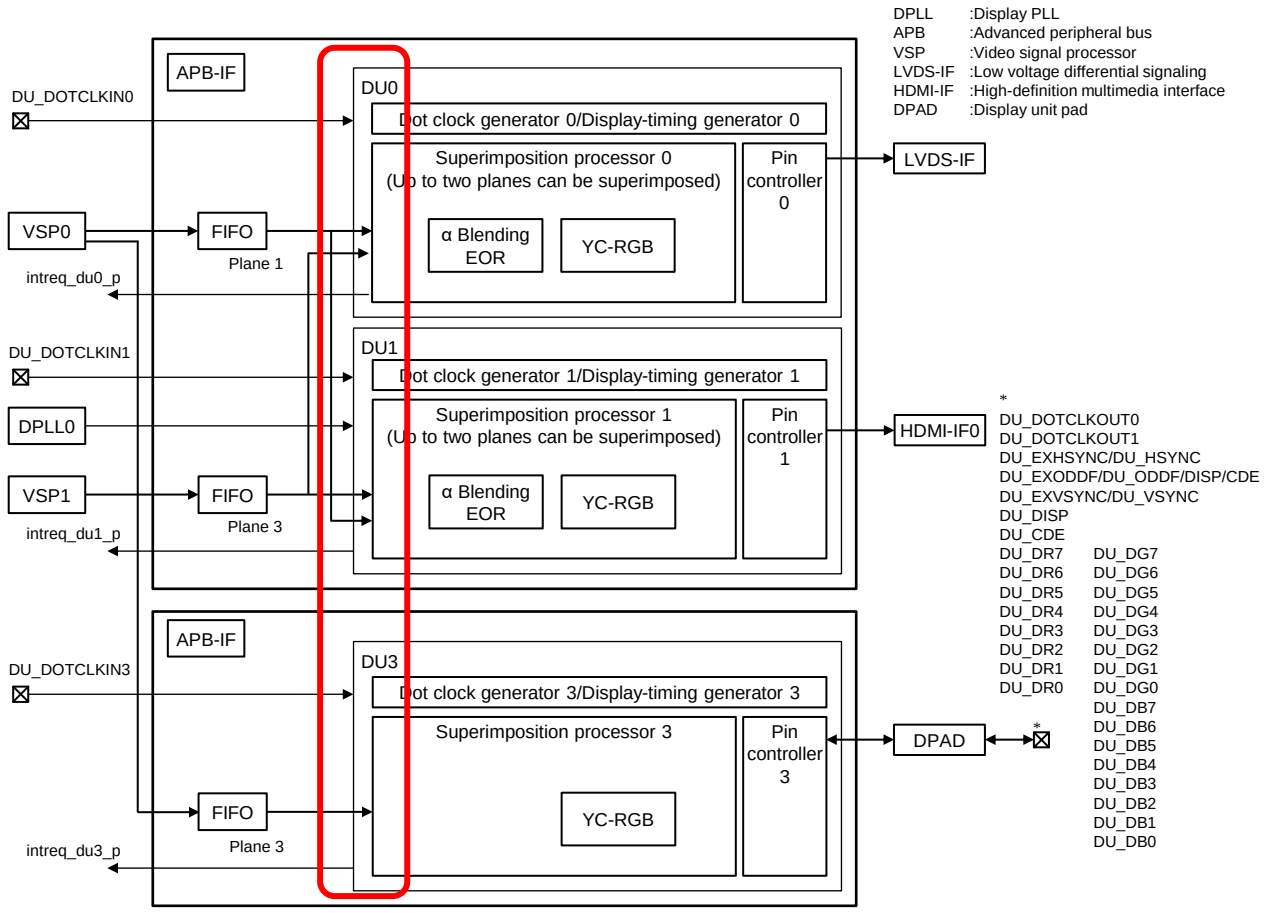


Figure 36.2 Block Diagram of the DU [RZ/G2H, RZ/G2N]

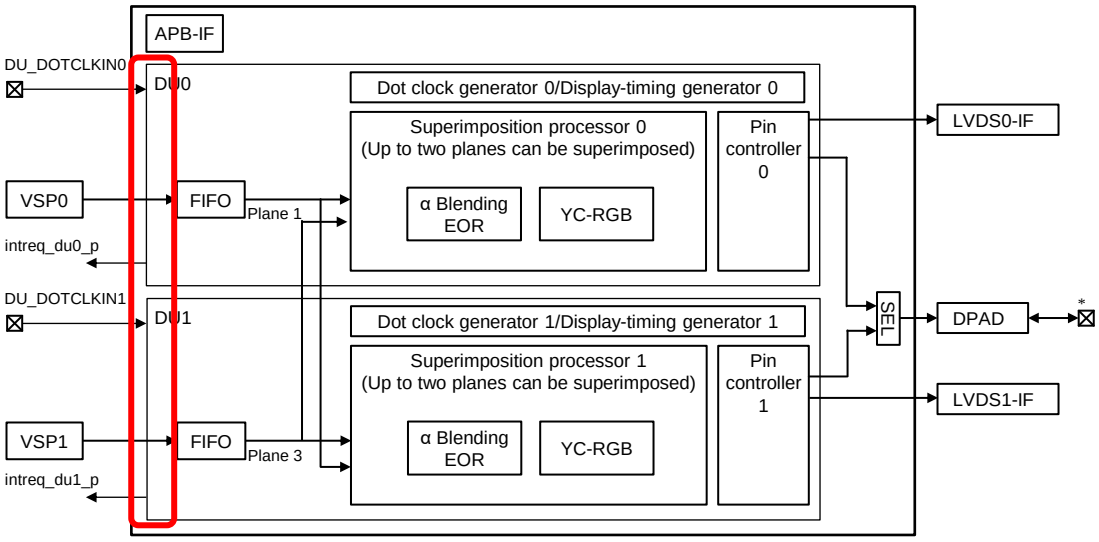
[Description]

In the RZ/G2H, G2N system, where the images of VSPD0 and VSPD1 are α blended using DU0, DU1 is not used, but DU1 is also running because the FIFO connected to VSPD1 is in DU1. Since DU0 and DU1 interrupts were used, the interrupt processing changed due to the dot clock frequency difference between DU0 and DU1, and FPS decreased.

[Reason for Correction]

The FIFO can be selected from the DIDSR0 register, but in the current Block Diagram, the FIFO appears to be fixed in DU0 or DU1 and is recognized as not being selectable. DU3 is fixed, but it will be modified to align the notation.

Current (from):



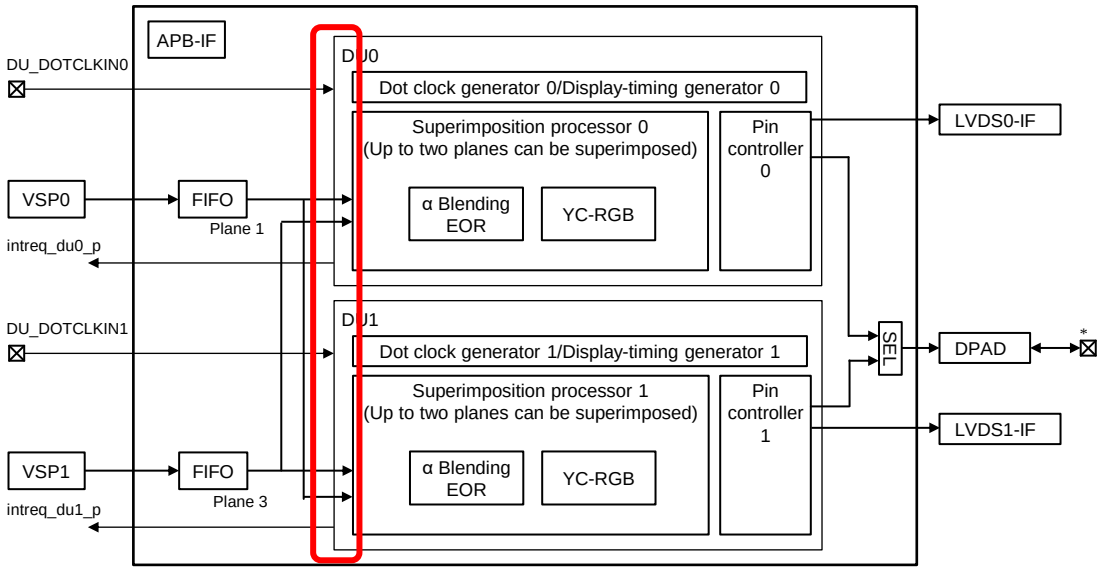
APB :Advanced peripheral bus
VSP :Video signal processor
LVDS-IF :Low voltage differential signaling
DPAD :Display unit pad

*
DU_DOTCLKOUT
DU_HSYNC
DU_VSYNC
DU_DISP
DU_CDE
DU_DISP_CDE

DU_DR7	DU_DG7	DU_DB7
DU_DR6	DU_DG6	DU_DB6
DU_DR5	DU_DG5	DU_DB5
DU_DR4	DU_DG4	DU_DB4
DU_DR3	DU_DG3	DU_DB3
DU_DR2	DU_DG2	DU_DB2
DU_DR1	DU_DG1	DU_DB1
DU_DR0	DU_DG0	DU_DB0

Figure 36.3 Block Diagram of the DU [RZ/G2E]

Correct (to):



APB :Advanced peripheral bus
VSP :Video signal processor
LVDS-IF :Low voltage differential signaling
DPAD :Display unit pad

*
DU_DOTCLKOUT
DU_HSYNC
DU_VSYNC
DU_DISP
DU_CDE
DU_DISP_CDE

DU_DR7	DU_DG7	DU_DB7
DU_DR6	DU_DG6	DU_DB6
DU_DR5	DU_DG5	DU_DB5
DU_DR4	DU_DG4	DU_DB4
DU_DR3	DU_DG3	DU_DB3
DU_DR2	DU_DG2	DU_DB2
DU_DR1	DU_DG1	DU_DB1
DU_DR0	DU_DG0	DU_DB0

Figure 36.3 Block Diagram of the DU [RZ/G2E]

[Description]

In the RZ/G2E system, where the images of VSPD0 and VSPD1 are α blended using DU0, DU1 is not used, but DU1 is also running because the FIFO connected to VSPD1 is in DU1. Since DU0 and DU1 interrupts were used, the interrupt processing changed due to the dot clock frequency difference between DU0 and DU1, and FPS decreased.

[Reason for Correction]

The FIFO can be selected from the DIDSR0 register, but in the current Block Diagram, the FIFO appears to be fixed in DU0 or DU1 and is recognized as not being selectable.

- End of Document -