Date: Apr. 23, 2024

RENESAS TECHNICAL UPDATE

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Renesas Electronics Corporation

Product Category	MPU/MCU		Document No.	TN-RZ*-A0130A/E	Rev.	1.00
Title	RZ/G2H, G2M V1.3, G2M V3.0, G2N and G2E Correction of section 33.Video Signal Processor (VSP2)		Information Category	Technical Notification		
Applicable Product	RZ/G Series, 2nd Generation RZ/G2H RZ/G2M V1.3, V3.0 RZ/G2N RZ/G2E	Lot No. All lots	Reference Document	RZ/G Series, 2nd Generation User's Manual: Hardware Rev.1.11 (R01UH0808EJ0111)		

This technical update describes document correction of RZ/G Series, 2nd Generation product.

[Summary]

Add the description in the “33.2.8.4 {mod} Routing Register (VI6_DPR_{mod}_ROUTE: {mod} = ILV_BRS, SRU, UDS, LUT, CLU, HST, HSI, BRU, SHP) “.

[Priority level]

Importance: “Normal”

Urgency: “Normal”

[Products]

RZ/G2H

RZ/G2M V1.3, V3.0

RZ/G2N

RZ/G2E

[Section number and title]

Section 33. VSP2

“This is empty adjustment page to compare next Current (from) and Correction (to) on facing page. “

(By using two pages view of PDF readers this enables previously and prospectively view on odd and even pages.)

[Correction]

1. Section 33. VSP2, Page 33-142, 33.2.8.4 {mod} Routing Register (VI6_DPR_{mod}_ROUTE: {mod} = ILV_BRS, SRU, UDS, LUT, CLU, HST, HSI, BRU, SHP).

Current (from):

33.2.8.4 {mod} Routing Register (VI6_DPR_{mod}_ROUTE: {mod} = ILV_BRS, SRU, UDS, LUT, CLU, HST, HSI, BRU, SHP)

RZ/G2H	RZ/G2M V1.3, RZ/G2M V3.0	RZ/G2N	RZ/G2E
√	√	√	√

Bit:	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
	—	—	—	BRS SEL	—	—	—	—	FXA[7:0]							
Initial value:	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
R/W:	R	R	R	R/W	R	R	R	R	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W

Bit:	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
	—	—	FP[5:0]						—	—	RT[5:0]					
Initial value:	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
R/W:	R	R	R/W	R/W	R/W	R/W	R/W	R/W	R	R	R/W	R/W	R/W	R/W	R/W	R/W

Bit	Bit Name	Initial Value	R/W	Description
31 to 29, 27 to 24, 15, 14, 7, 6	—	All 0	R	Reserved These bits are always read as 0. The write value should always be 0.
28	BRSSEL	B'0	R/W	Select ILV or BRS 0: ILV is selected 1: BRS is selected. BRS and ILV shares data path route. Setting VI6_DPR_ILV_BRS_ROUTE is needed in case of using ILV or BRS. This bit select ILV or BRS for VI6_DPR_ILV_BRS_ROUTE. Set 0 to this bit in case of using ILV. Set 1 to this bit in case of using BRS. This bit is available in only VI6_DPR_ILV_BRS_ROUTE.
23 to 16	FXA [7:0]	All 0	R/W	Fixed α Output Value for {mod} The {mod} does not support input/output of the α value. The α value input to the {SHP, SRU, LUT, CLU, HST and HSI} is discarded, and the fixed α value specified in these bits is always output from the {SHP, SRU, LUT, CLU, HST and HSI}. A value from 0 to 255 can be specified. These bits are valid for SHP, SRU, LUT, CLU, HST and HSI modules. For UDS, ILV, BRS and BRU modules, these bits are reserved.
13 to 8	FP [5:0]	All 0	R/W	{mod} Internal Operation Timing Setting Specify 0.
5 to 0	RT [5:0]	All 0	R/W	{mod}Target Node Value These bits specify the target node value for the {mod}. When using the {mod}, refer to Figure 33.31 to Figure 33.32 for settings. When not using the {mod}, specify 63.

Correct (to):

33.2.8.4 {mod} Routing Register (VI6_DPR_{mod}_ROUTE: {mod} = ILV_BRS, SRU, UDS, LUT, CLU, HST, HSI, BRU, SHP)

RZ/G2H	RZ/G2M V1.3, RZ/G2M V3.0	RZ/G2N	RZ/G2E
√	√	√	√

Bit:	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
	—	—	—	BRS SEL	—	—	—	—	FXA[7:0]							
Initial value:	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
R/W:	R	R	R	R/W	R	R	R	R	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W

Bit:	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
	—	—	FP[5:0]						—	—	RT[5:0]					
Initial value:	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
R/W:	R	R	R/W	R/W	R/W	R/W	R/W	R/W	R	R	R/W	R/W	R/W	R/W	R/W	R/W

Bit	Bit Name	Initial Value	R/W	Description
31 to 29, 27 to 24, 15, 14, 7, 6	—	All 0	R	Reserved These bits are always read as 0. The write value should always be 0.
28	BRSSEL	B'0	R/W	Select ILV or BRS 0: ILV is selected 1: BRS is selected. BRS and ILV shares data path route. Setting VI6_DPR_ILV_BRS_ROUTE is needed in case of using ILV or BRS. This bit select ILV or BRS for VI6_DPR_ILV_BRS_ROUTE. Set 0 to this bit in case of using ILV. Set 1 to this bit in case of using BRS. This bit is available in only VI6_DPR_ILV_BRS_ROUTE.
23 to 16	FXA [7:0]	All 0	R/W	Fixed α Output Value for {mod} In the case where {mod} is {SHP, SRU, LUT, CLU, HST and HSI}. The α value input to the {SHP, SRU, LUT, CLU, HST and HSI} is discarded, and the fixed α value specified in these bits is always output from the {SHP, SRU, LUT, CLU, HST and HSI}. A value from 0 to 255 can be specified. In the case where {mod} is {UIF(DISCOM), UDS, ILV, BRS and BRU} Reserved These bits are always read as 0. The write value should always be 0.
13 to 8	FP [5:0]	All 0	R/W	{mod} Internal Operation Timing Setting Specify 0.
5 to 0	RT [5:0]	All 0	R/W	{mod}Target Node Value These bits specify the target node value for the {mod}. When using the {mod}, refer to Figure 33.31 to Figure 33.32 for settings. When not using the {mod}, specify 63.

[Description]

Add the description in the “33.2.8.4 {mod} Routing Register (VI6_DPR_{mod}_ROUTE: {mod} = ILV_BRS, SRU, UDS, LUT, CLU, HST, HSI, BRU, SHP)“.

[Reason for Correction]

To correct description error.

- End of Document -