Date: Dec. 8, 2023

RENESAS TECHNICAL UPDATE

TOYOSU FORESIA, 3-2-24, Toyosu, Koto-ku, Tokyo 135-0061, Japan
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Product Category	MPU/MCU		Document No.	TN-RZ*-A0124A/E	Rev.	1.00
Title	RZ/G2H, G2M V1.3, G2M V3.0, G2N and G2E Additional specification for 73. Electrical Specification (RPC, SDHI and MMC Interface)		Information Category	Technical Notification		
Applicable Product	RZ/G Series, 2nd Generation RZ/G2H RZ/G2M V1.3, V3.0 RZ/G2N RZ/G2E	Lot No. All lots	Reference Document	RZ/G Series, 2nd Generation User's Manual: Hardware Rev.1.11 (R01UH0808EJ0111)		

This technical update describes document correction of RZ/G Series, 2nd Generation product.

[Summary]

Additional specification for 73. Electrical Specification (RPC, SDHI and MMC Interface)

[Priority level]

Importance: “Normal”

Urgency: “Normal”

[Products]

RZ/G2H

RZ/G2M V1.3, V3.0

RZ/G2N

RZ/G2E

[Section number and title]

Section 73.24 RPC Interface

Section 73.25 SD Host Interface (SDHI)

Section 73.26 MMC Interface

“This is empty adjustment page to compare next Current (from) and Correction (to) on facing page. “

(By using two pages view of PDF readers this enables previously and prospectively view on odd and even pages.)

[Correction]

1. Section 73.24. RPC Interface, Page 73-89 to 73-93, Table 73.24.1 to Table 73.24.3 Addition of input slew rate “tDSISR”, and Addition of Figure 73.24.5 RPC DDR Operation Timing (Input slew rate)

Current (from):

73.24 RPC Interface

Table 73.24.1 RPC Timing [RZ/G2H, RZ/G2M V1.3, RZ/G2M V3.0 and RZ/G2N]

Conditions: VDDQ18 = 1.8V ± 0.1 V, GND = VSS = 0 V,
Tc = −40 to +115 °C [RZ/G2M V1.3], Ta = −40 to + 85 °C [RZ/G2M V3.0, RZ/G2N],
Tj = −40 to + 115 °C [RZ/G2M V3.0, RZ/G2N],
CL = 15 pF

Item	Symbol	Min.	Typ.	Max.	Unit	Figures
SPCLK clock cycle time (HyperFlash)	tSPCYC	6.25	—	—	ns	Figure 73.24.1
SPCLK clock cycle time (QSPI Flash)		12.50	—	—	ns	
SPCLK high pulse width	tSPWH	0.45	—	0.55	tSPCYC	
SPCLK low pulse width	tSPWL	0.45	—	0.55	tSPCYC	
SPCLK rise time	tSPR	—	—	2.0	ns	
SPCLK fall time	tSPF	—	—	2.0	ns	
SPCLK skew	tSPSKEW	—	—	0.04	tSPCYC	
SSL to setup time	tLEAD	1 × tSPCYC – 3	—	8 × tSPCYC + 3	ns	Figure 73.24.2, Figure 73.24.3, Figure 73.24.4
SSL to hold time	tLAG	5.5 × tSPCYC – 3	—	8.5 × tSPCYC + 3	ns	
Data input valid setup time SDR	tVSS	—	—	0.5 × tSPCYC + 3	ns	Figure 73.24.2
Data input valid hold time SDR	tVHS	0	—	—	ns	
Data output setup time	tOS	0.5 × tSPCYC – 2	—	—	ns	
Data output hold time	tOH	0.5 × tSPCYC – 2	—	—	ns	
Data input valid setup time DDR	tVSD	—	—	6.5	ns	Figure 73.24.3
Data input valid hold time DDR	tVHD	0.32 × tSPCYC	—	—	ns	
Data to Data Strobe Skew	tDDSS	-0.65	—	0.65	ns	Figure 73.24.4
SPCLK to Data Strobe Skew	tCDSS	—	—	7.0	ns	
Output Data Setup time in DDR mode	tSDDR	0.25 × tSPCYC – 0.6	—	0.25 × tSPCYC + 0.6	ns	Figure 73.24.3, Figure 73.24.4
Output Data Hold time in DDR mode	tHDDR	0.25 × tSPCYC – 0.6	—	0.25 × tSPCYC + 0.6	ns	
RPC_RESET assert time	tRPCRA	0	—	—	ns	Figure 73.24.5
RPC_RESET negate time	tRPCRN	10	—	—	ns	Figure 73.24.5

Note: The RZ/G2M V1.3 does not support DDR operation with QSPI (1-/4-bit) and QSPIx2 (8-bit). Therefore, the following DDR related specifications with QSPI and QSPIx2 cannot be applied to the RZ/G2M V1.3.

Correct (to):

73.24 RPC Interface

Table 73.24.1 RPC Timing [RZ/G2H, RZ/G2M V1.3, RZ/G2M V3.0 and RZ/G2N]

Conditions: VDDQ18 = 1.8V ± 0.1 V, GND = VSS = 0 V,
Tc = −40 to +115 °C [RZ/G2M V1.3], Ta = −40 to + 85 °C [RZ/G2M V3.0, RZ/G2N],
Tj = −40 to + 115 °C [RZ/G2M V3.0, RZ/G2N],
CL = 15 pF

Item	Symbol	Min.	Typ.	Max.	Unit	Figures
SPCLK clock cycle time (HyperFlash)	tSPCYC	6.25	—	—	ns	Figure 73.24.1
SPCLK clock cycle time (QSPI Flash)		12.50	—	—	ns	
SPCLK high pulse width	tSPWH	0.45	—	0.55	tSPCYC	
SPCLK low pulse width	tSPWL	0.45	—	0.55	tSPCYC	
SPCLK rise time	tSPR	—	—	2.0	ns	
SPCLK fall time	tSPF	—	—	2.0	ns	
SPCLK skew	tSPSKEW	—	—	0.04	tSPCYC	
SSL to setup time	tLEAD	1 × tSPCYC – 3	—	8 × tSPCYC + 3	ns	Figure 73.24.2, Figure 73.24.3, Figure 73.24.4
SSL to hold time	tLAG	5.5 × tSPCYC – 3	—	8.5 × tSPCYC + 3	ns	
Data input valid setup time SDR	tVSS	—	—	0.5 × tSPCYC + 3	ns	Figure 73.24.2
Data input valid hold time SDR	tVHS	0	—	—	ns	
Data output setup time	tOS	0.5 × tSPCYC – 2	—	—	ns	
Data output hold time	tOH	0.5 × tSPCYC – 2	—	—	ns	
Data input valid setup time DDR	tVSD	—	—	6.5	ns	Figure 73.24.3
Data input valid hold time DDR	tVHD	0.32 × tSPCYC	—	—	ns	
Data to Data Strobe Skew	tDDSS	-0.65	—	0.65	ns	Figure 73.24.4
SPCLK to Data Strobe Skew	tCDSS	—	—	7.0	ns	
Output Data Setup time in DDR mode	tSDDR	0.25 × tSPCYC – 0.6	—	0.25 × tSPCYC + 0.6	ns	Figure 73.24.3, Figure 73.24.4
Output Data Hold time in DDR mode	tHDDR	0.25 × tSPCYC – 0.6	—	0.25 × tSPCYC + 0.6	ns	
Input Slew rate with Data Strobe usage	tDSISR	0.94	—	—	V/ns	Figure 73.24.5
RPC_RESET assert time	tRPCRA	0	—	—	ns	Figure 73.24.6
RPC_RESET negate time	tRPCRN	10	—	—	ns	Figure 73.24.6

Note: The RZ/G2M V1.3 does not support DDR operation with QSPI (1-/4-bit) and QSPIx2 (8-bit). Therefore, the following DDR related specifications with QSPI and QSPIx2 cannot be applied to the RZ/G2M V1.3.

[Description]

Add input slew rate spec.

[Reason for Correction]

Prevention of deterioration of characteristics.

Current (from):

Table 73.24.2 RPC Timing [RZ/G2E]

Conditions: VDDQ_QSPI = 1.8V ± 0.1 V, GND = VSS = 0 V,
Ta = −40 to + 85 °C
Tj = −40 to + 115 °C
CL = 15 pF

Item	Symbol	Min.	Typ.	Max.	Unit	Figures
SPCLK clock cycle time (HyperFlash)	tSPCYC	6.66	—	—	ns	Figure 73.24.1
SPCLK clock cycle time (QSPI Flash)		12.50	—	—	ns	
SPCLK high pulse width	tSPWH	0.45	—	0.55	tSPCYC	
SPCLK low pulse width	tSPWL	0.45	—	0.55	tSPCYC	
SPCLK rise time	tSPR	—	—	2.0	ns	
SPCLK fall time	tSPF	—	—	2.0	ns	
SPCLK skew	tSPSKEW	—	—	0.04	tSPCYC	
SSL to setup time	tLEAD	1 × tSPCYC – 3	—	8 × tSPCYC + 3	ns	Figure 73.24.2, Figure 73.24.3, Figure 73.24.4
SSL to hold time	tLAG	5.5 × tSPCYC – 3	—	8.5 × tSPCYC + 3	ns	
Data input valid setup time SDR	tVSS	—	—	0.5 × tSPCYC + 3	ns	Figure 73.24.2
Data input valid hold time SDR	tVHS	0	—	—	ns	
Data output setup time	tOS	0.5 × tSPCYC – 2	—	—	ns	
Data output hold time	tOH	0.5 × tSPCYC – 2	—	—	ns	
Data input valid setup time DDR	tVSD	—	—	6.5	ns	Figure 73.24.3
Data input valid hold time DDR	tVHD	0.32 × tSPCYC	—	—	ns	
Data to Data Strobe Skew	tDDSS	-0.65	—	0.65	ns	Figure 73.24.4
SPCLK to Data Strobe Skew	tCDSS	—	—	7.0	ns	
Output Data Setup time in DDR mode	tSDDR	0.25 × tSPCYC – 0.6	—	0.25 × tSPCYC + 0.6	ns	Figure 73.24.3, Figure 73.24.4
Output Data Hold time in DDR mode	tHDDR	0.25 × tSPCYC – 0.6	—	0.25 × tSPCYC + 0.6	ns	
RPC_RESET assert time	tRPCRA	0	—	—	ns	Figure 73.24.5
RPC_RESET negate time	tRPCRN	10	—	—	ns	Figure 73.24.5

Correct (to):

Table 73.24.2 RPC Timing [RZ/G2E]

Conditions: VDDQ_QSPI = 1.8V ± 0.1 V, GND = VSS = 0 V,
Ta = −40 to + 85 °C
Tj = −40 to + 115 °C
CL = 15 pF

Item	Symbol	Min.	Typ.	Max.	Unit	Figures
SPCLK clock cycle time (HyperFlash)	tSPCYC	6.66	—	—	ns	Figure 73.24.1
SPCLK clock cycle time (QSPI Flash)		12.50	—	—	ns	
SPCLK high pulse width	tSPWH	0.45	—	0.55	tSPCYC	
SPCLK low pulse width	tSPWL	0.45	—	0.55	tSPCYC	
SPCLK rise time	tSPR	—	—	2.0	ns	
SPCLK fall time	tSPF	—	—	2.0	ns	
SPCLK skew	tSPSKEW	—	—	0.04	tSPCYC	
SSL to setup time	tLEAD	1 × tSPCYC – 3	—	8 × tSPCYC + 3	ns	Figure 73.24.2, Figure 73.24.3, Figure 73.24.4
SSL to hold time	tLAG	5.5 × tSPCYC – 3	—	8.5 × tSPCYC + 3	ns	
Data input valid setup time SDR	tVSS	—	—	0.5 × tSPCYC + 3	ns	Figure 73.24.2
Data input valid hold time SDR	tVHS	0	—	—	ns	
Data output setup time	tOS	0.5 × tSPCYC – 2	—	—	ns	
Data output hold time	tOH	0.5 × tSPCYC – 2	—	—	ns	
Data input valid setup time DDR	tVSD	—	—	6.5	ns	Figure 73.24.3
Data input valid hold time DDR	tVHD	0.32 × tSPCYC	—	—	ns	
Data to Data Strobe Skew	tDDSS	-0.65	—	0.65	ns	Figure 73.24.4
SPCLK to Data Strobe Skew	tCDSS	—	—	7.0	ns	
Output Data Setup time in DDR mode	tSDDR	0.25 × tSPCYC – 0.6	—	0.25 × tSPCYC + 0.6	ns	Figure 73.24.3, Figure 73.24.4
Output Data Hold time in DDR mode	tHDDR	0.25 × tSPCYC – 0.6	—	0.25 × tSPCYC + 0.6	ns	
Input Slew rate with Data Strobe usage	tDSISR	0.94	—	—	V/ns	Figure 73.24.5
RPC_RESET assert time	tRPCRA	0	—	—	ns	Figure 73.24.6
RPC_RESET negate time	tRPCRN	10	—	—	ns	Figure 73.24.6

[Description]

Add input slew rate spec.

[Reason for Correction]

Prevention of deterioration of characteristics.

Current (from):

Table 73.24.3 RPC Timing [RZ/G2E]

Conditions: VDDQ_QSPI = 3.3 V ± 0.3 V, GND = VSS = 0 V, Ta = -40 to +85 °C, Tj = -40 to + 115 °C, CL = 15 pF

Item	Symbol	Min.	Typ.	Max.	Unit	Figures
SPCLK clock cycle time (HyperFlash)	tSPCYC	10.00	—	—	ns	Figure 73.24.1
SPCLK clock cycle time (QSPI Flash)		12.50	—	—	ns	
SPCLK high pulse width	tSPWH	0.45	—	0.55	tSPCYC	
SPCLK low pulse width	tSPWL	0.45	—	0.55	tSPCYC	
SPCLK rise time	tSPR	—	—	2.0	ns	
SPCLK fall time	tSPF	—	—	2.0	ns	
SPCLK skew	tSPSKEW	—	—	0.04	tSPCYC	
SSL to setup time	tLEAD	1 × tSPCYC – 3	—	8 × tSPCYC + 3	ns	Figure 73.24.2, Figure 73.24.3, Figure 73.24.4
SSL to hold time	tLAG	5.5 × tSPCYC – 3	—	8.5 × tSPCYC + 3	ns	
Data input valid setup time SDR	tVSS	—	—	0.5 × tSPCYC + 3	ns	Figure 73.24.2
Data input valid hold time SDR	tVHS	0	—	—	ns	
Data output setup time	tOS	0.5 × tSPCYC – 2	—	—	ns	
Data output hold time	tOH	0.5 × tSPCYC – 2	—	—	ns	
Data input valid setup time DDR	tVSD	—	—	6.5	ns	Figure 73.24.3
Data input valid hold time DDR	tVHD	0.32 × tSPCYC	—	—	ns	
Data to Data Strobe Skew	tDDSS	-0.65	—	0.65	ns	Figure 73.24.4
SPCLK to Data Strobe Skew	tCDSS	—	—	7.0	ns	
Output Data Setup time in DDR mode	tSDDR	0.25 × tSPCYC – 0.6	—	0.25 × tSPCYC + 0.6	ns	Figure 73.24.3, Figure 73.24.4
Output Data Hold time in DDR mode	tHDDR	0.25 × tSPCYC – 0.6	—	0.25 × tSPCYC + 0.6	ns	
RPC_RESET assert time	tRPCRA	0	—	—	ns	Figure 73.24.5
RPC_RESET negate time	tRPCRN	10	—	—	ns	Figure 73.24.5

Correct (to):

Table 73.24.3 RPC Timing [RZ/G2E]

Conditions: VDDQ_QSPI = 3.3 V ± 0.3 V, GND = VSS = 0 V, Ta = -40 to +85 °C, Tj = -40 to + 115 °C, CL = 15 pF

Item	Symbol	Min.	Typ.	Max.	Unit	Figures
SPCLK clock cycle time (HyperFlash)	tSPCYC	10.00	—	—	ns	Figure 73.24.1
SPCLK clock cycle time (QSPI Flash)		12.50	—	—	ns	
SPCLK high pulse width	tSPWH	0.45	—	0.55	tSPCYC	
SPCLK low pulse width	tSPWL	0.45	—	0.55	tSPCYC	
SPCLK rise time	tSPR	—	—	2.0	ns	
SPCLK fall time	tSPF	—	—	2.0	ns	
SPCLK skew	tSPSKEW	—	—	0.04	tSPCYC	
SSL to setup time	tLEAD	1 × tSPCYC – 3	—	8 × tSPCYC + 3	ns	Figure 73.24.2, Figure 73.24.3, Figure 73.24.4
SSL to hold time	tLAG	5.5 × tSPCYC – 3	—	8.5 × tSPCYC + 3	ns	
Data input valid setup time SDR	tVSS	—	—	0.5 × tSPCYC + 3	ns	Figure 73.24.2
Data input valid hold time SDR	tVHS	0	—	—	ns	
Data output setup time	tOS	0.5 × tSPCYC – 2	—	—	ns	
Data output hold time	tOH	0.5 × tSPCYC – 2	—	—	ns	
Data input valid setup time DDR	tVSD	—	—	6.5	ns	Figure 73.24.3
Data input valid hold time DDR	tVHD	0.32 × tSPCYC	—	—	ns	
Data to Data Strobe Skew	tDDSS	-0.65	—	0.65	ns	Figure 73.24.4
SPCLK to Data Strobe Skew	tCDSS	—	—	7.0	ns	
Output Data Setup time in DDR mode	tSDDR	0.25 × tSPCYC – 0.6	—	0.25 × tSPCYC + 0.6	ns	Figure 73.24.3, Figure 73.24.4
Output Data Hold time in DDR mode	tHDDR	0.25 × tSPCYC – 0.6	—	0.25 × tSPCYC + 0.6	ns	
Input Slew rate with Data Strobe usage	tDSISR	0.94	—	—	V/ns	Figure 73.24.5
RPC_RESET assert time	tRPCRA	0	—	—	ns	Figure 73.24.6
RPC_RESET negate time	tRPCRN	10	—	—	ns	Figure 73.24.6

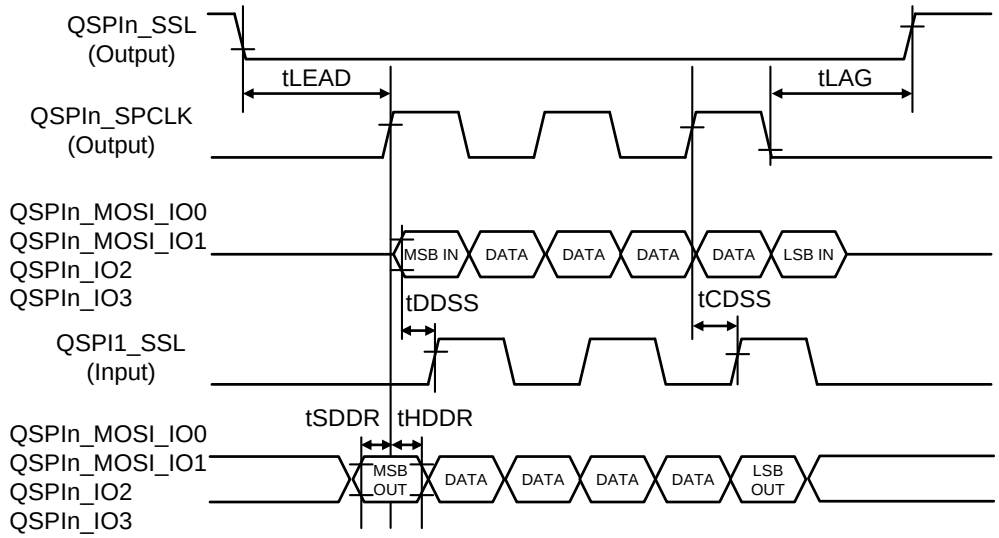
[Description]

Add input slew rate spec.

[Reason for Correction]

Prevention of deterioration of characteristics.

Current (from):



Note: DATA is RPC related data pins (QSPIn_*IOm (n = 0, 1 / m = 0, 1, 2, 3)).

Figure 73.24.4 RPC DDR Operation Timing (HyperFlash)

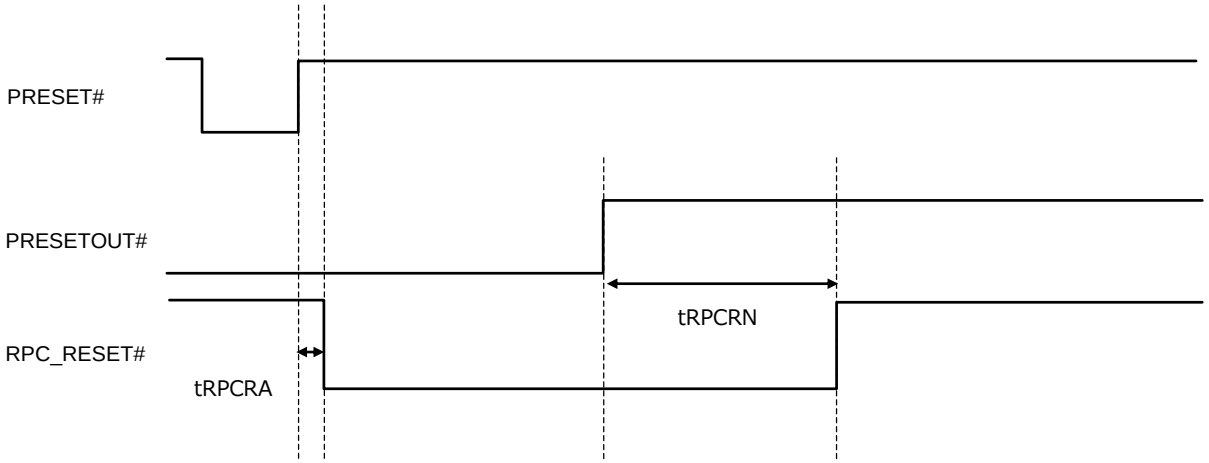
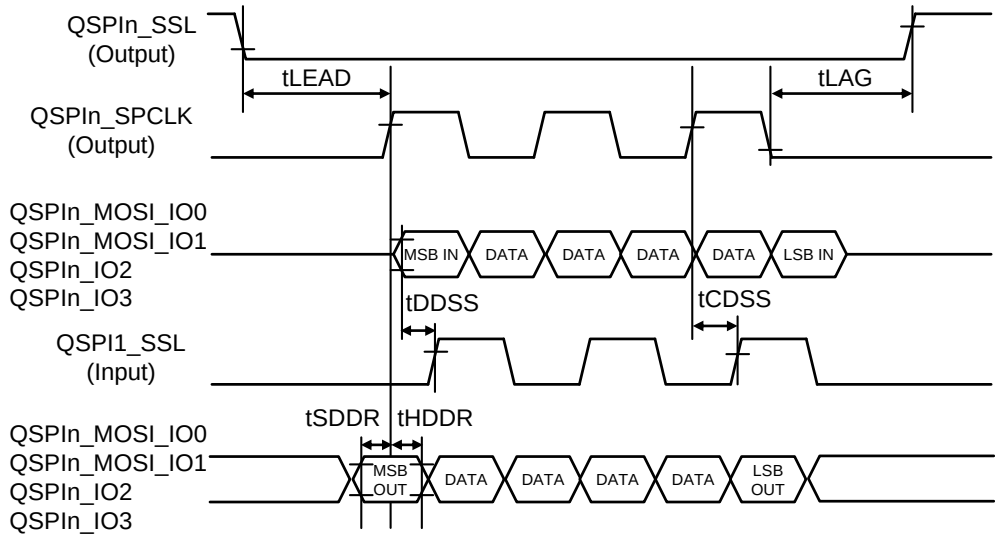


Figure 73.24.5 RPC_RESET# Operation Timing

Correct (to):



Note: DATA is RPC related data pins (QSPIn_*IOm (n = 0, 1 / m = 0, 1, 2, 3)).

Figure 73.24.4 RPC DDR Operation Timing (HyperFlash)

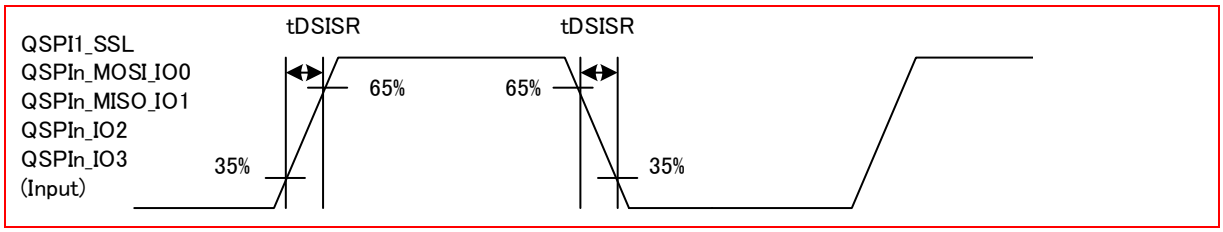


Figure 73.24.5 RPC DDR Operation Timing (Input Slew rate)

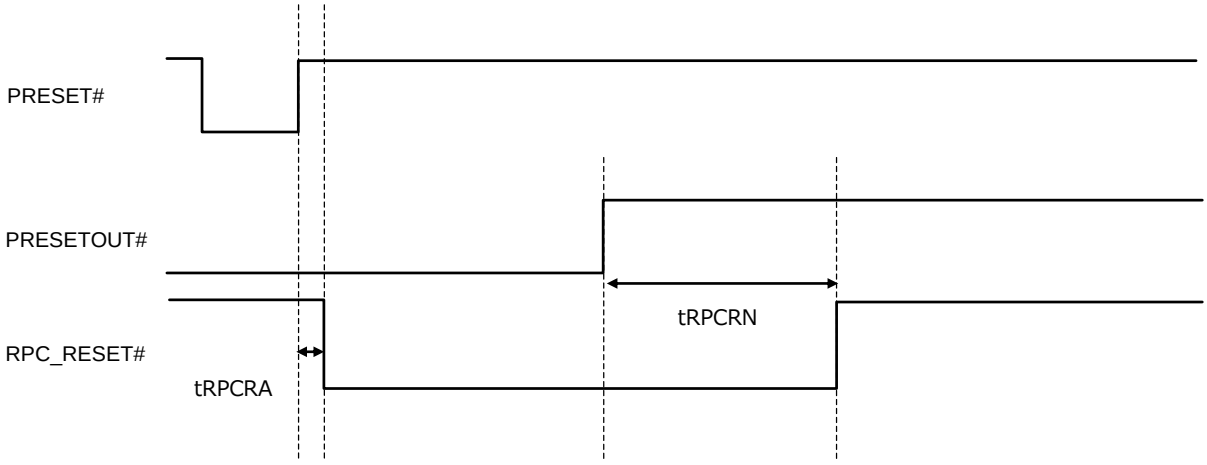


Figure 73.24.6 RPC_RESET# Operation Timing

[Description]

Add input slew rate spec.

[Reason for Correction]

Prevention of deterioration of characteristics.

[Correction]

2. Section 73.25. SDHI Host Interface (SDHI), Page 73-94, Figure 73.25.1, changed reference voltage level.

Current (from):

73.25.1 SDHI (3.3V) Electrical Characteristics

Table 73.25.1 SDHI Signal Timing (Default mode)

Conditions: VDDQVA_SDn (n = 0 to 3) = 3.3 V ± 0.2 V, GND = VSS = 0 V,
Tc = −40 to +115 °C [RZ/G2H, RZ/G2M V1.3], Ta = -40 to +85 °C [RZ/G2M V3.0, RZ/G2N],
Tj = -40 to +115 °C [RZ/G2M V3.0, RZ/G2N],
VDDQ_SDn (n = 0, 1, 3) = 3.3V ± 0.3 V, GND = VSS = 0 V,
Ta = −40 to + 85 °C [RZ/G2E], Tj = −40 to + 115 °C [RZ/G2E],
CL = 40 pF

Item	Symbol	Min.	Typ.	Max.	Unit	Figures
SDCLK clock cycle time	t_{SDCYC}	40.0	—	—	ns	Figure 73.25.1
SDCMD output data delay time	t_{SDCMD_S}	—	—	10.0	ns	
	t_{SDCMD_H}	6.0	—	—	ns	
SDDAT output data delay time	t_{SDDAD_S}	—	—	10.0	ns	
	t_{SDDAD_H}	6.0	—	—	ns	
SDCMD input data setup time	t_{SDCMS}	3.0	—	—	ns	
SDCMD input data hold time	t_{SDCMH}	2.0	—	—	ns	
SDDAT input data setup time	t_{SDDAS}	3.0	—	—	ns	
SDDAT input data hold time	t_{SDDAH}	2.0	—	—	ns	

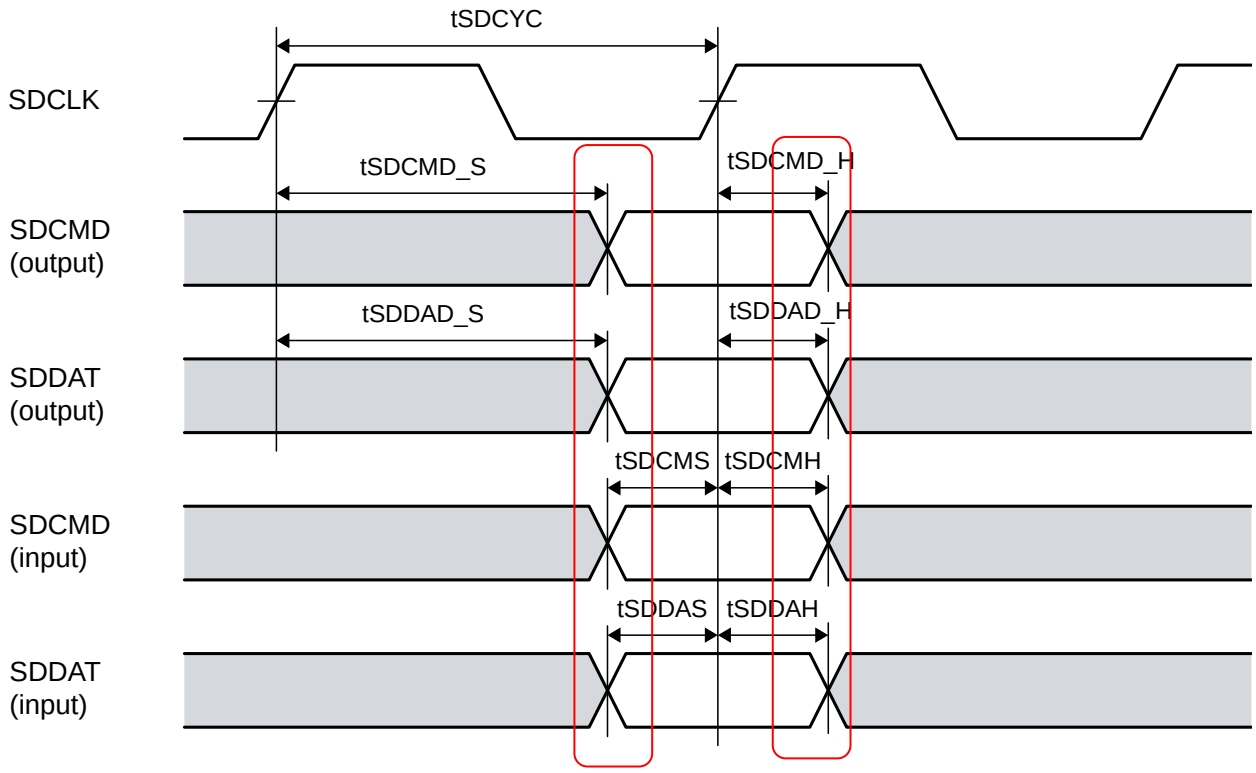


Figure 73.25.1 SDHI Signal Timing (Default mode)

Correction (to):

73.25.1 SDHI (3.3V) Electrical Characteristics

Table 73.25.1 SDHI Signal Timing (Default mode)

Conditions: VDDQVA_SDn (n = 0 to 3) = 3.3 V ± 0.2 V, GND = VSS = 0 V,
Tc = −40 to +115 °C [RZ/G2H, RZ/G2M V1.3], Ta = -40 to +85 °C [RZ/G2M V3.0, RZ/G2N],
Tj = -40 to +115 °C [RZ/G2M V3.0, RZ/G2N],
VDDQ_SDn (n = 0, 1, 3) = 3.3V ± 0.3 V, GND = VSS = 0 V,
Ta = −40 to + 85 °C [RZ/G2E], Tj = −40 to + 115 °C [RZ/G2E],
CL = 40 pF

Item	Symbol	Min.	Typ.	Max.	Unit	Figures
SDCLK clock cycle time	t_{SDCYC}	40.0	—	—	ns	Figure 73.25.1
SDCMD output data delay time	t_{SDCMD_S}	—	—	10.0	ns	
	t_{SDCMD_H}	6.0	—	—	ns	
SDDAT output data delay time	t_{SDDAD_S}	—	—	10.0	ns	
	t_{SDDAD_H}	6.0	—	—	ns	
SDCMD input data setup time	t_{SDCMS}	3.0	—	—	ns	
SDCMD input data hold time	t_{SDCMH}	2.0	—	—	ns	
SDDAT input data setup time	t_{SDDAS}	3.0	—	—	ns	
SDDAT input data hold time	t_{SDDAH}	2.0	—	—	ns	

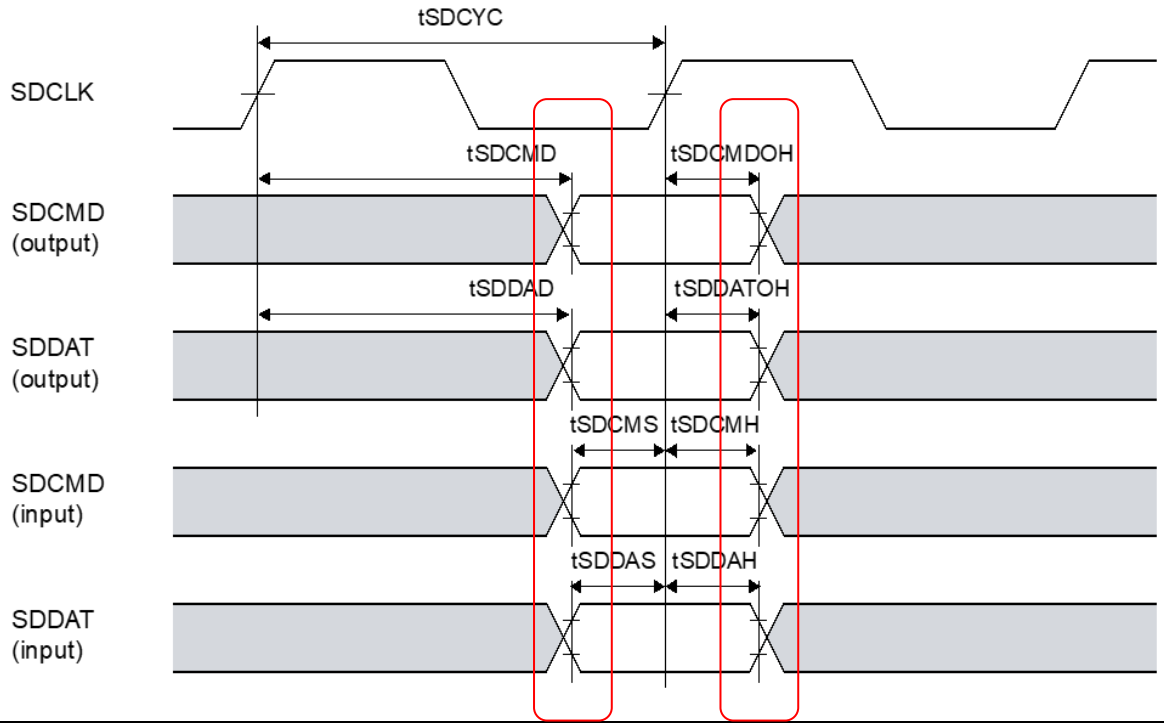


Figure 73.25.1 SDHI Signal Timing (Default mode)

[Description]

Change the reference voltage level.

[Reason for Correction]

Prevention of deterioration of characteristics.

[Correction]

3. Section 73.26. MMC Interface Page 73-99, Table 73.26.2 and Figure 73.26.2 MMC Signal Timing, added output hold time specification.

Current (from):

73.26.2 MMC (1.8V) Electrical Characteristics [RZ/G2H, RZ/G2M V1.3, RZ/G2M V3.0, RZ/G2N and RZ/G2E]

Table 73.26.2 MMC Signal Timing (High Speed mode)

Conditions: VDDQVA_SDn (n = 2, 3) = 1.8 V ± 0.1 V [RZ/G2H, RZ/G2M V1.3, RZ/G2M V3.0, RZ/G2N], VDDQ_SD3 = 1.8 V ± 0.1 V [RZ/G2E], GND = VSS = 0 V,
Tc = −40 to +115 °C [RZ/G2H, RZ/G2M V1.3],
Ta = -40 to +85 °C [RZ/G2M V3.0, RZ/G2N, RZ/G2E],
Tj = -40 to +115 °C [RZ/G2M V3.0, RZ/G2N, RZ/G2E],
CL = 30 pF [RZ/G2H, RZ/G2M V1.3, RZ/G2M V3.0, RZ/G2N and RZ/G2E],
GND = VSS = 0 V

Item	Symbol	Min.	Typ.	Max.	Unit	Figures
MMCCLK clock cycle time	t_{MMCCYC}	20.0	—	—	ns	Figure 73.26.2
MMCCMD output data delay time	t_{MMCCMD}	3.0	—	0.5 × t_{MMCCYC} + 3.0	ns	
MMCDAT output data delay time	t_{MMCDAD}	3.0	—	0.5 × t_{MMCCYC} + 3.0	ns	
MMCCMD input data setup time	t_{MMCCMS}	3.0	—	—	ns	
MMCCMD input data hold time	t_{MMCCMH}	2.0	—	—	ns	
MMCDAT input data setup time	t_{MMCDAS}	3.0	—	—	ns	
MMCDAT input data hold time	t_{MMCDAH}	2.0	—	—	ns	

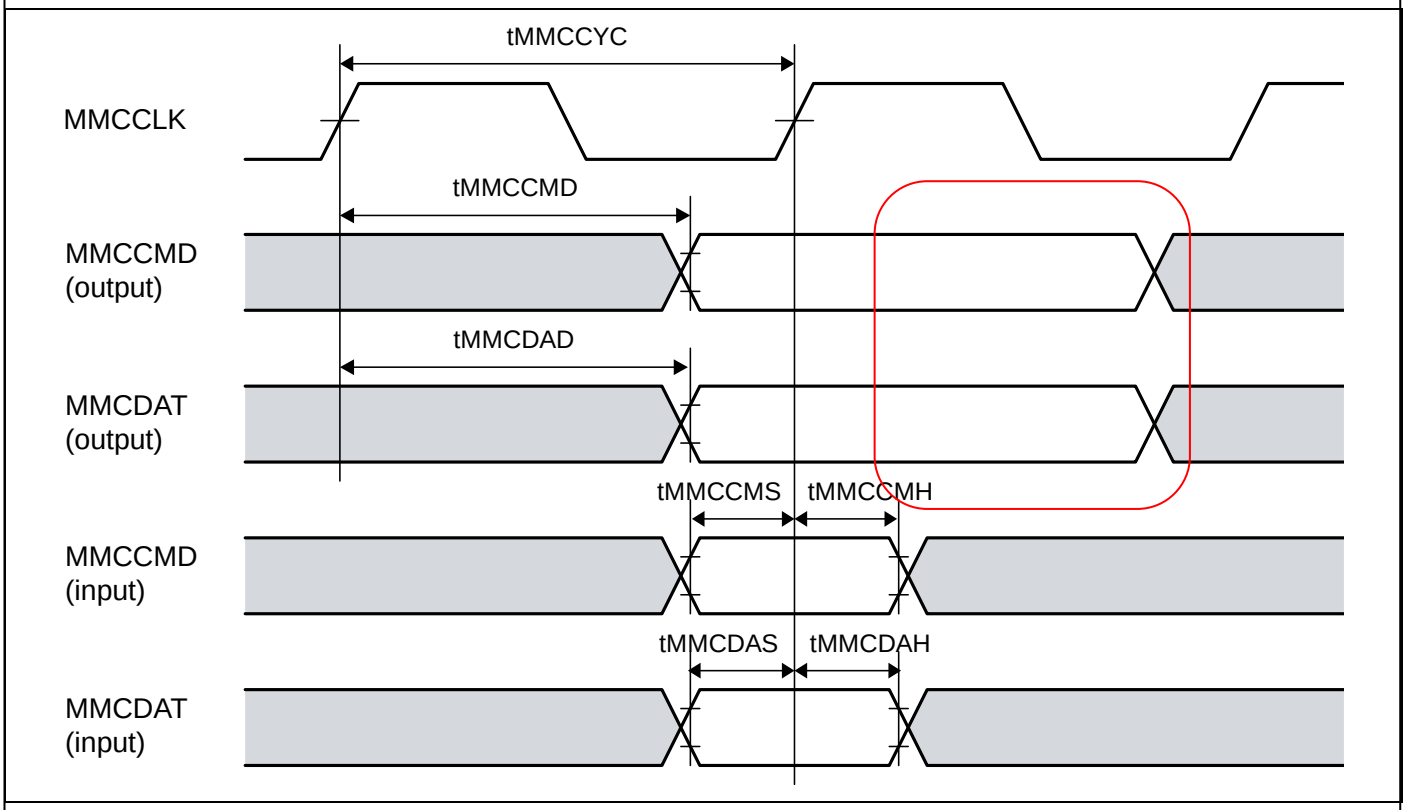


Figure 73.26.2 MMC Signal Timing

Correction (to):

73.26.2 MMC (1.8V) Electrical Characteristics [RZ/G2H, RZ/G2M V1.3, RZ/G2M V3.0, RZ/G2N and RZ/G2E]

Table 73.26.2 MMC Signal Timing (High Speed mode)

Conditions: VDDQVA_SDn (n = 2, 3) = 1.8 V ± 0.1 V [RZ/G2H, RZ/G2M V1.3, RZ/G2M V3.0, RZ/G2N], VDDQ_SD3 = 1.8 V ± 0.1 V [RZ/G2E], GND = VSS = 0 V,
Tc = −40 to +115 °C [RZ/G2H, RZ/G2M V1.3],
Ta = -40 to +85 °C [RZ/G2M V3.0, RZ/G2N, RZ/G2E],
Tj = -40 to +115 °C [RZ/G2M V3.0, RZ/G2N, RZ/G2E],
CL = 30 pF [RZ/G2H, RZ/G2M V1.3, RZ/G2M V3.0, RZ/G2N and RZ/G2E],
GND = VSS = 0 V

Item	Symbol	Min.	Typ.	Max.	Unit	Figures
MMCCLK clock cycle time	t_{MMCCYC}	20.0	—	—	ns	Figure 73.26.2
MMCCMD output data delay time	t_{MMCCMD}	3.0	—	0.5 × t_{MMCCYC} + 3.0	ns	
MMCCMD output data hold time	$t_{MMCCMDOH}$	3.0	—	—	ns	
MMCDAT output data delay time	t_{MMCDAD}	3.0	—	0.5 × t_{MMCCYC} + 3.0	ns	
MMCDAT output data hold time	$t_{MMCDATOH}$	3.0	—	—	ns	
MMCCMD input data setup time	t_{MMCCMS}	3.0	—	—	ns	
MMCCMD input data hold time	t_{MMCCMH}	2.0	—	—	ns	
MMCDAT input data setup time	t_{MMCDAS}	3.0	—	—	ns	
MMCDAT input data hold time	t_{MMCDAH}	2.0	—	—	ns	

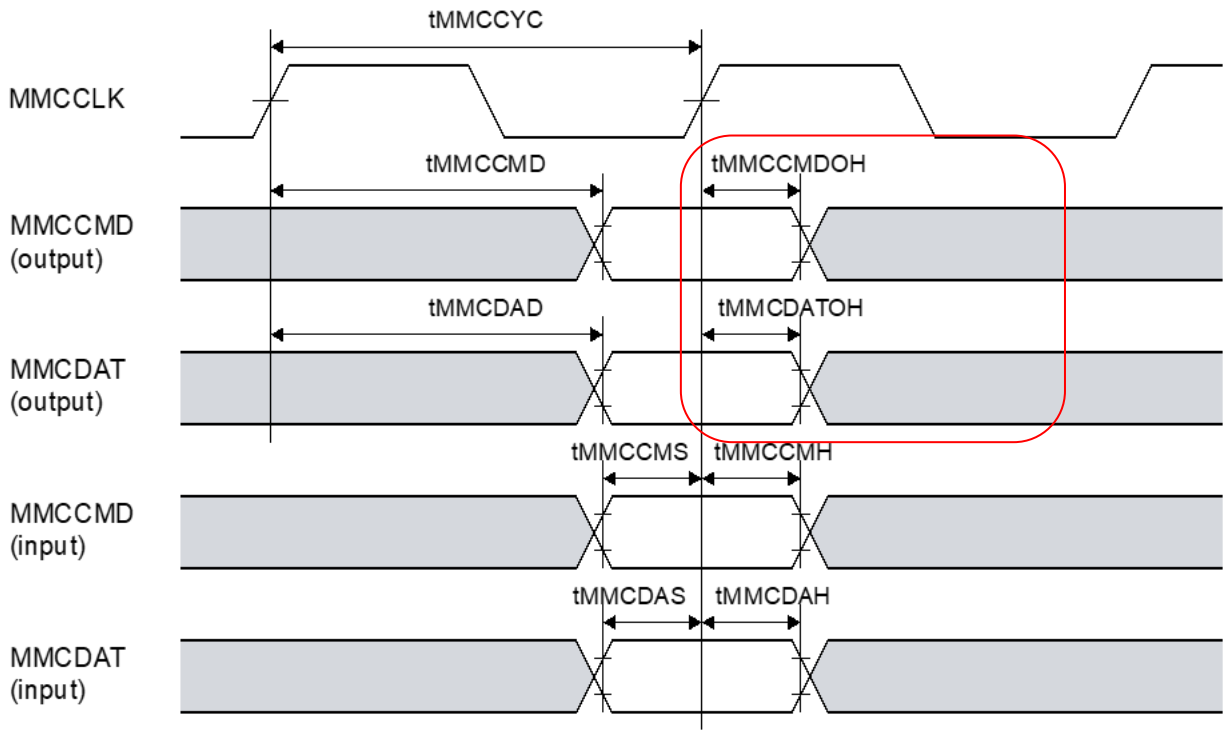


Figure 73.26.2 MMC Signal Timing

[Description]

Add output hold time.

[Reason for Correction]

Clarification of specification.

[Correction]

4. Section 73.26. MMC Interface Page 73-101, Table 73.26.4 MMC Signal Timing (HS400 mode), correction and addition.

Current (from):

Table 73.26.4 MMC Signal Timing (HS400 mode) [RZ/G2H, RZ/G2M V1.3, RZ/G2M V3.0, RZ/G2N and RZ/G2E]

Conditions: VDDQVA_SDn (n = 2, 3) = 1.8 V ± 0.1 V[RZ/G2H, RZ/G2M V1.3, RZ/G2M V3.0, RZ/G2N], VDDQ_SD3 = 1.8 V ± 0.1 V [RZ/G2E], GND = VSS = 0 V,
Tc = −40 to +115 °C [RZ/G2H, RZ/G2M V1.3],
Ta = -40 to +85 °C [RZ/G2M V3.0, RZ/G2N, RZ/G2E],
Tj = -40 to +115 °C [RZ/G2M V3.0, RZ/G2N, RZ/G2E], CL = 10 pF

Item	Symbol	Min.	Typ.	Max.	Unit	Remarks	Figures
MMCCLK clock cycle time	tMMCCYC	5.0	—	—	ns		Figure 73.26.4
MMCDS data strobe cycle time	tMMCDCYC	5.0	—	—	ns		
MMCDS minimum pulse with	tDSW	2.0	—	—	ns		
MMCDAT input data setup time	tMMCDIDS	—	—	0.6	ns	eMMC0-1 [RZ/G2H, RZ/G2M V3.0, RZ/G2N, RZ/G2E]	
						eMMC0 [RZ/G2M V1.3]	
				0.5	ns	eMMC1 [RZ/G2M V1.3]	
MMCDAT input data hold time	tMMCDIDH	1.5	—	—	ns		
MMCDAT output data setup time	tMMCDWDS	0.6	—	—	ns		
MMCDAT output data hold time	tMMCDWDH	0.6	—	—	ns		

The MMCCMD input timing for HS400 mode is the same as CMD timing for HS200 mode.

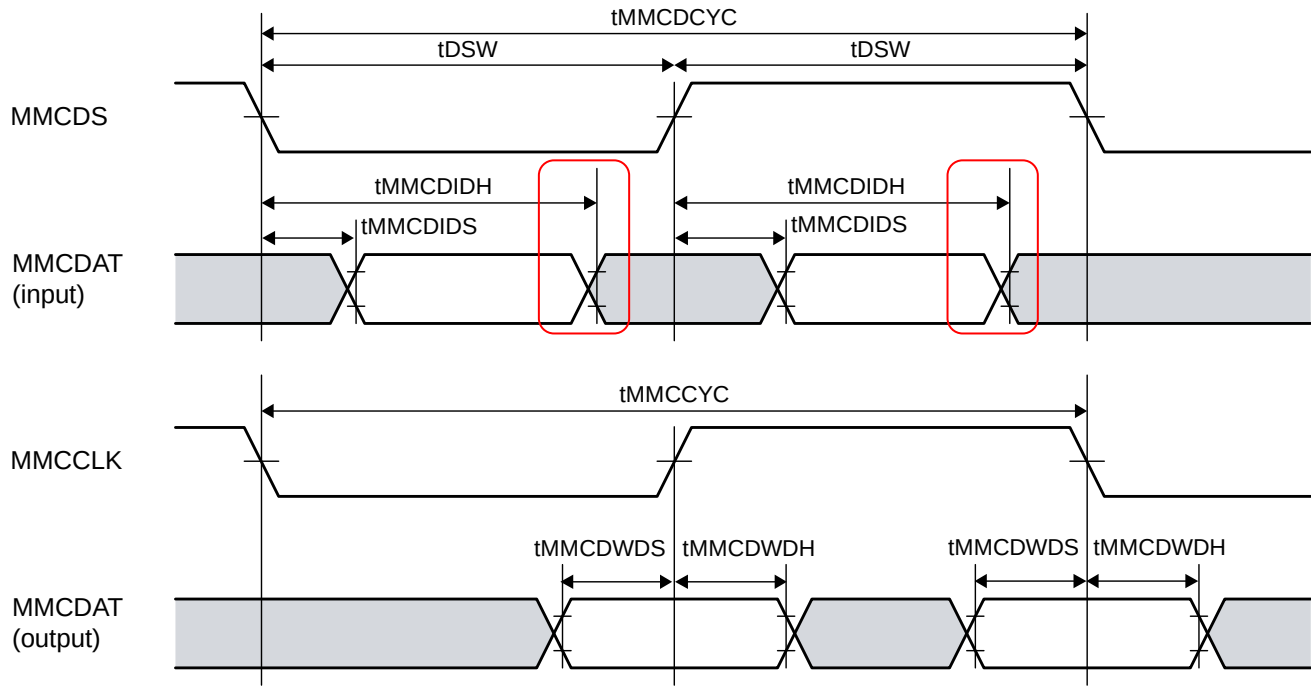


Figure 73.26.4 MMC Signal Timing (HS400 mode)

Correction (to):

Table 73.26.4 MMC Signal Timing (HS400 mode) [RZ/G2H, RZ/G2M V1.3, RZ/G2M V3.0, RZ/G2N and RZ/G2E]

Conditions: VDDQVA_SDn (n = 2, 3) = 1.8 V ± 0.1 V[RZ/G2H, RZ/G2M V1.3, RZ/G2M V3.0, RZ/G2N], VDDQ_SD3 = 1.8 V ± 0.1 V [RZ/G2E], GND = VSS = 0 V,
Tc = −40 to +115 °C [RZ/G2H, RZ/G2M V1.3],
Ta = -40 to +85 °C [RZ/G2M V3.0, RZ/G2N, RZ/G2E],
Tj = -40 to +115 °C [RZ/G2M V3.0, RZ/G2N, RZ/G2E], CL = 10 pF

Item	Symbol	Min.	Typ.	Max.	Unit	Remarks	Figures
MMCCLK clock cycle time	tMMCCYC	5.0	—	—	ns		Figure 73.26.4
MMCDS data strobe cycle time	tMMCDCYC	5.0	—	—	ns		
MMCDS minimum pulse with	tDSW	2.0	—	—	ns		
Input Slew rate with MMCDS/MMCDAT	tDSISR	1.125	—	—	V/ns		Figure 73.26.5
MMCDAT input data setup time	tMMCDIDS	—	—	0.6	ns	eMMC0-1 [RZ/G2H, RZ/G2M V3.0, RZ/G2N, RZ/G2E] eMMC0 [RZ/G2M V1.3]	Figure 73.26.4
				0.5	ns	eMMC1 [RZ/G2M V1.3]	
MMCDAT input data hold time	tMMCDIDH	0.5 × tMMCCYC – 1.0	—	—	ns		
MMCDAT output data setup time	tMMCDWDS	0.6	—	—	ns		
MMCDAT output data hold time	tMMCDWDH	0.6	—	—	ns		

The MMCCMD input timing for HS400 mode is the same as CMD timing for HS200 mode.

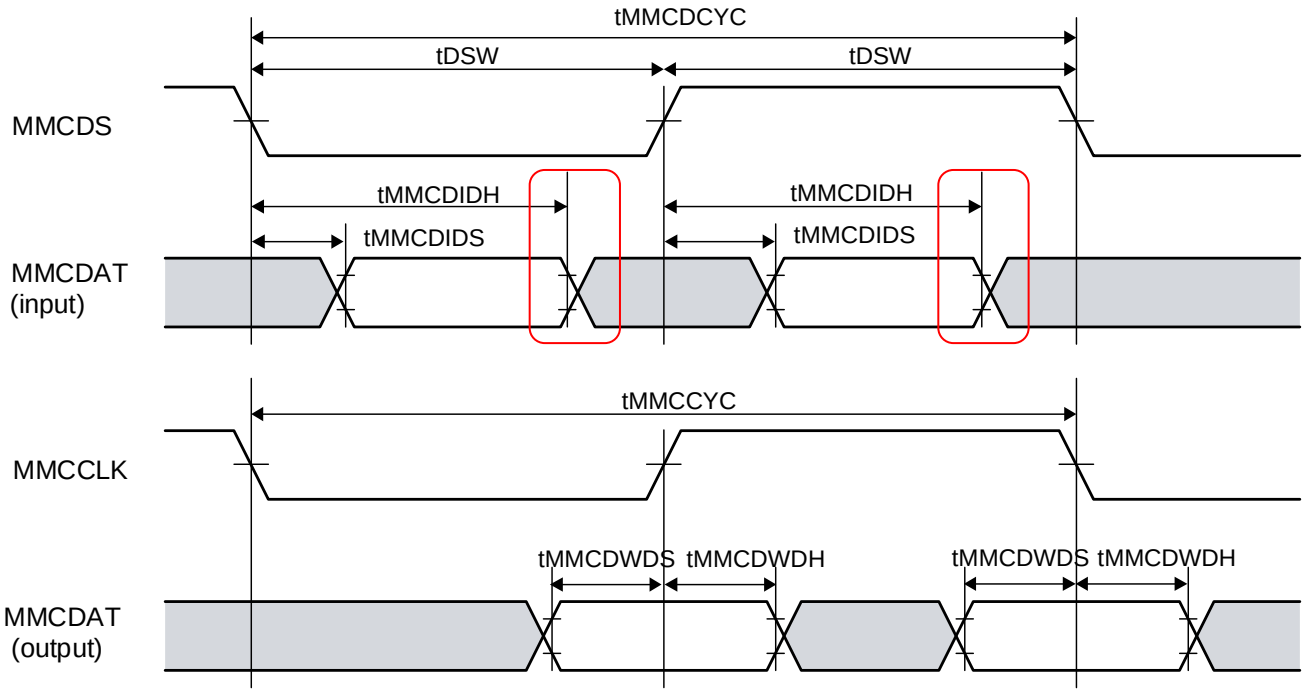


Figure 73.26.4 MMC Signal Timing (HS400 mode)

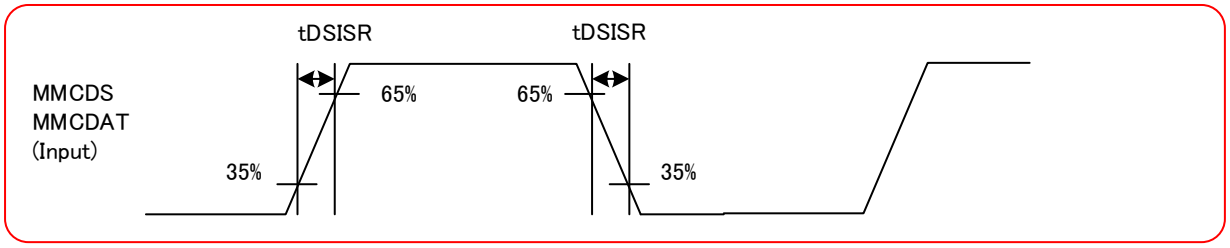


Figure 73.26.5 MMC Operation Timing (HS400 mode) (Input Slew rate)

[Description]

Add input slew rate spec, Change formula, Correct and add the timing chart.

[Reason for Correction]

Prevention of deterioration of characteristics, Clarification of specification.

- End of Document -