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RENESAS TECHNICAL UPDATE

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Product Category	MPU/MCU		Document No.	TN-RZ*-A0123A/E	Rev.	1.00
Title	RZ/G2H, G2M V1.3, G2M V3.0, G2N and G2E Addition of section 30.Video Input Module (VIN)		Information Category	Technical Notification		
Applicable Product	RZ/G Series, 2nd Generation RZ/G2H RZ/G2M V1.3, V3.0 RZ/G2N RZ/G2E	Lot No. All lots	Reference Document	RZ/G Series, 2nd Generation User's Manual: Hardware Rev.1.11 (R01UH0808EJ0111)		

This technical update describes document correction of RZ/G Series, 2nd Generation product.

[Summary]

Added notes to pin configuration of VINx data enable(control) on the Table 30.7. (x:4, 5)

[Priority level]

Importance: “Normal”

Urgency: “Normal”

[Products]

RZ/G2H

RZ/G2M V1.3, V3.0

RZ/G2N

RZ/G2E

[Section number and title]

Section 30. Video Input Module (VIN)

“This is empty adjustment page to compare next Current (from) and Correction (to) on facing page. “

(By using two pages view of PDF readers this enables previously and prospectively view on odd and even pages.)

[Correction]

1. Page 30-15, 30-16, 30.1.3 External Pins, VI4_CLKENB and VI5_CLKENB, note description is added.

Current (from):

30.1.3 External Pins

Table 30.7 Pin Configuration

				Second Generation RZ/G Series Products				
Pin Name	**Function**	**I/O**	**Description**	**RZ/G2H**	**RZ/G2M V1.3 RZ/G2M V3.0**	**RZ/G2N**	**RZ/G2E**
VIN4 video clock (clock)	VI4_CLK	Input	External video clock in the ITU-R BT.601, ITU-R BT.656, ITU-R BT.1358, or ITU-R BT.709 interface	√	√	√	√
VIN4 field signal (control)	VI4_FIELD	Input	Field signal in the ITU-R BT.601 or ITU-R BT.709 interface Fix this pin high or low when the pin is not used.	√	√	√	√
VIN4 vertical sync signal (control)	VI4_VSYNC#	Input	Vertical sync signal in the ITU-R BT.601, ITU-R BT.1358, or ITU-R BT.709 interface Fix this pin high or low when the pin is not used.	√	√	√	√
VIN4 horizontal sync signal (control)	VI4_HSYNC#	Input	Horizontal sync signal in the ITU-R BT.601, ITU-R BT.1358, or ITU-R BT.709 interface Fix this pin high or low when the pin is not used.	√	√	√	√
VIN4 data enable (control)	VI4_CLKENB	Input	Data enable signal in the ITU-R BT.601, ITU-R BT.1358, or ITU-R BT.709 interface Fix this pin high or low when the pin is not used. If the signal is not present in the ITU-R BT.601, ITU-R BT.1358, or ITU-R BT.709 interface, connect the pin to a horizontal sync signal.	√	√	√	√
VIN4 video data (video data)	VI4_DATA23 to VI4_DATA 0	Input	Data signals in the ITU-R BT.601, ITU-R BT.656, ITU-R BT.1358, or ITU-R BT.709 interface Fix these pins high or low respectively when these pins are not used in whole or in part.	√	√	√	√
VIN5 video clock (clock)	VI5_CLK	Input	External video clock in the ITU-R BT.601, ITU-R BT.656, ITU-R BT.1358, or ITU-R BT.709 interface	√	√	√	√
VIN5 field signal (control)	VI5_FIELD	Input	Field signal in the ITU-R BT.601 or ITU-R BT.709 interface Fix this pin high or low when the pin is not used.	√	√	√	√

Correct (to):

30.1.4 External Pins

Table 30.7 Pin Configuration

				Second Generation RZ/G Series Products				
Pin Name	**Function**	**I/O**	**Description**	**RZ/G2H**	**RZ/G2M V1.3**	**RZ/G2M V3.0**	**RZ/G2N**	**RZ/G2E**
VIN4 video clock (clock)	VI4_CLK	Input	External video clock in the ITU-R BT.601, ITU-R BT.656, ITU-R BT.1358, or ITU-R BT.709 interface	√	√		√	√
VIN4 field signal (control)	VI4_FIELD	Input	Field signal in the ITU-R BT.601 or ITU-R BT.709 interface Fix this pin high or low when the pin is not used.	√	√		√	√
VIN4 vertical sync signal (control)	VI4_VSYNC#	Input	Vertical sync signal in the ITU-R BT.601, ITU-R BT.1358, or ITU-R BT.709 interface Fix this pin high or low when the pin is not used.	√	√		√	√
VIN4 horizontal sync signal (control)	VI4_HSYNC#	Input	Horizontal sync signal in the ITU-R BT.601, ITU-R BT.1358, or ITU-R BT.709 interface Fix this pin high or low when the pin is not used.	√	√		√	√
VIN4 data enable (control)	VI4_CLKENB	Input	Data enable signal in the ITU-R BT.601, ITU-R BT.1358, or ITU-R BT.709 interface Fix this pin high or low when the pin is not used. If the signal is not present in the ITU-R BT.601, ITU-R BT.1358, or ITU-R BT.709 interface, connect the pin to a horizontal sync signal. Note: When connecting data enable signal to this pin, horizontal sync signal should be negated after 8 cycles of last valid data input. This is from the restriction as tVCMcyc specified for the electrical characteristics.	√	√		√	√
VIN4 video data (video data)	VI4_DATA23 to VI4_DATA 0	Input	Data signals in the ITU-R BT.601, ITU-R BT.656, ITU-R BT.1358, or ITU-R BT.709 interface Fix these pins high or low respectively when these pins are not used in whole or in part.	√	√		√	√
VIN5 video clock (clock)	VI5_CLK	Input	External video clock in the ITU-R BT.601, ITU-R BT.656, ITU-R BT.1358, or ITU-R BT.709 interface	√	√		√	√

Current (from):

VIN5 vertical sync signal (control)	VI5_VSYNC#	Input	Vertical sync signal in the ITU-R BT.601, ITU-R BT.1358, or ITU-R BT.709 interface Fix this pin high or low when the pin is not used.	√	√	√	√
VIN5 horizontal sync signal (control)	VI5_HSYNC#	Input	Horizontal sync signal in the ITU-R BT.601, ITU-R BT.1358, or ITU-R BT.709 interface Fix this pin high or low when the pin is not used.	√	√	√	√
VIN5 data enable (control)	VI5_CLKENB	Input	Data enable signal in the ITU-R BT.601, ITU-R BT.1358, or ITU-R BT.709 interface Fix this pin high or low when the pin is not used. If the signal is not present in the ITU-R BT.601, ITU-R BT.1358, or ITU-R BT.709 interface, connect the pin to a horizontal sync signal.	√	√	√	√
VIN5 video data (video data)	VI5_DATA15 to VI5_DATA 0	Input	Data signals in the ITU-R BT.601, ITU-R BT.656, ITU-R BT.1358, or ITU-R BT.709 interface Fix these pins high or low respectively when these pins are not used in whole or in part.	√	√	√	√

Correction (to):

VIN5 field signal (control)	VI5_FIELD	Input	Field signal in the ITU-R BT.601 or ITU-R BT.709 interface Fix this pin high or low when the pin is not used.	√	√	√	√
VIN5 vertical sync signal (control)	VI5_VSYNC#	Input	Vertical sync signal in the ITU-R BT.601, ITU-R BT.1358, or ITU-R BT.709 interface Fix this pin high or low when the pin is not used.	√	√	√	√
VIN5 horizontal sync signal (control)	VI5_HSYNC#	Input	Horizontal sync signal in the ITU-R BT.601, ITU-R BT.1358, or ITU-R BT.709 interface Fix this pin high or low when the pin is not used.	√	√	√	√
VIN5 data enable (control)	VI5_CLKENB	Input	Data enable signal in the ITU-R BT.601, ITU-R BT.1358, or ITU-R BT.709 interface Fix this pin high or low when the pin is not used. If the signal is not present in the ITU-R BT.601, ITU-R BT.1358, or ITU-R BT.709 interface, connect the pin to a horizontal sync signal. Note: When connecting data enable signal to this pin, horizontal sync signal should be negated after 8 cycles of last valid data input. This is from the restriction as tVCMcyc specified for the electrical characteristics.	√	√	√	√
VIN5 video data (video data)	VI5_DATA15 to VI5_DATA 0	Input	Data signals in the ITU-R BT.601, ITU-R BT.656, ITU-R BT.1358, or ITU-R BT.709 interface Fix these pins high or low respectively when these pins are not used in whole or in part.	√	√	√	√

[Description]

Added note to Pin name “VIN4, VIN5 data enable (control)” (Function name “VI4_CLKENB, VI5_CLKENB”) in Table 30.7 “Pin Configuration”.

[Reason for Correction]

Limited by the electrical characteristics of the video sync signal.

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