Date: Dec. 11, 2023

RENESAS TECHNICAL UPDATE

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Product Category	MPU/MCU		Document No.	TN-RZ*-A0128A/E	Rev.	1.00
Title	RZ/G2H, G2M, G2N and G2E Correction of section 37. LVDS Interface		Information Category	Technical Notification		
Applicable Product	RZ/G Series, 2nd Generation RZ/G2H, RZ/G2M V1.3, V3.0 RZ/G2N, RZ/G2E	Lot No. All lots	Reference Document	RZ/G Series, 2nd Generation User's Manual: Hardware Rev.1.11 (R01UH0808EJ0111)		

This technical update describes document correction of RZ/G Series, 2nd Generation product.

[Summary]

Correction of the LVDS max frequency and the LVDS setting flow in RZ/G2E.

[Priority level]

Importance: “Normal”

Urgency: “Normal”

[Products]

RZ/G2H

RZ/G2M V1.3, V3.0

RZ/G2N

RZ/G2E

[Section number and title]

Section 37. LVDS

“This is empty adjustment page to compare next Current (from) and Correction (to) on facing page. “

(By using two pages view of PDF readers this enables previously and prospectively view on odd and even pages.)

[Correction]

1. Page 37-1, 37.1.1 Features, Description of Operating frequency is corrected.

Current (from):

37. LVDS Interface

RZ/G2H RZ/G2M V1.3 RZ/G2M V3.0 RZ/G2N RZ/G2E

37.1 Overview

The LVDS-IF (low voltage differential signaling) module converts an RGB signal output by the DU module to the LVDS format and outputs those signals.

The LVDS-IF interface supports 8 output data formats with the conversion formats selected by register settings. The output control signals can also be selected freely.

The LVDS-IF supports the Dual-link output by using vertical stripe output function. [RZ/G2E]

37.1.1 Features

This module has the following features.

- Output pins: Five differential output pairs (4 data and 1 clock) that conform to the TIA/EIA-644 standard.
- Number of channels:

RZ/G2H, RZ/G2M V1.3, RZ/G2M V3.0, RZ/G2N: 1ch

RZ/G2E: 2ch

- Operating frequency: dot clock frequency is from 31MHz to 148.5 MHz [RZ/G2H, RZ/G2M V1.3, RZ/G2M V3.0, RZ/G2N]

Operating frequency: dot clock frequency is from 5 MHz to 148.5 MHz [RZ/G2E]

- Supports eight output data formats
- Supports the Dual-link output by using vertical stripe output function. [RZ/G2E]

Correction (to):

37. LVDS Interface

RZ/G2H
RZ/G2M V1.3 RZ/G2M V3.0
RZ/G2N RZ/G2E

37.1 Overview

The LVDS-IF (low voltage differential signaling) module converts an RGB signal output by the DU module to the LVDS format and outputs those signals.

The LVDS-IF interface supports 8 output data formats with the conversion formats selected by register settings. The output control signals can also be selected freely.

The LVDS-IF supports the Dual-link output by using vertical stripe output function. [RZ/G2E]

37.1.1 Features

This module has the following features.

- Output pins: Five differential output pairs (4 data and 1 clock) that conform to the TIA/EIA-644 standard.
- Number of channels:

RZ/G2H, RZ/G2M V1.3, RZ/G2M V3.0, RZ/G2N: 1ch

RZ/G2E: 2ch

- Operating frequency: dot clock frequency is from 31MHz to 150 MHz. [RZ/G2H, RZ/G2M V1.3, RZ/G2M V3.0, RZ/G2N]

Operating frequency: dot clock frequency is from 5 MHz to 150 MHz. [RZ/G2E]

- Supports eight output data formats
- Supports the Dual-link output by using vertical stripe output function. [RZ/G2E]

[Description]

Correction of typo in features.

[Reason for Correction]

Typo mistake in previous version.

2. Page 37-10, 37.2.3 PLL Control Register (LVDPLLCR / LVD1PLLCR), Operating frequency is corrected.

Current (from):

37.2.3 PLL Control Register (LVDPLLCR / LVD1PLLCR)

RZ/G2H	RZ/G2M V1.3, RZ/G2M V3.0	RZ/G2N	RZ/G2E
√	√	√	√

LVDPLLCR [RZ/G2H, RZ/G2M V1.3, RZ/G2M V3.0, RZ/G2N, RZ/G2E]

LVD1PLLCR [RZ/G2E]

[RZ/G2H, RZ/G2M V1.3, RZ/G2M V3.0, RZ/G2N]

Bit:	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
	—	—	—	—	—	—	—	—	—	—	—	—	—	PLLDIVCNT[18:16]		
Initial value:	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
R/W:	R	R	R	R	R	R	R	R	R	R	R	R	R	R/W	R/W	R/W

Bit:	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
	PLLDIVCNT [15:0]															
Initial value:	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
R/W:	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W

Bit	Bit Name	Initial Value	R/W	Description
31 to 19	—	All 0	R	Reserved [RZ/G2H, RZ/G2M V1.3, RZ/G2M V3.0, RZ/G2N] These bits are always read as 0. The write value should always be 0.
18 to 0	PLLDIVCNT	All 0	R/W	PLL Setting [RZ/G2H, RZ/G2M V1.3, RZ/G2M V3.0, RZ/G2N] Sets the PLL multiplication rate. H'0 14CB: 31 MHz <= dot clock < 42 MHz H'0 0A45: 42 MHz <= dot clock < 85 MHz H'0 06C3: 85 MHz <= dot clock < ~~128 MHz~~ H'0 46C1: 128 MHz <= dot clock <= 148.5 MHz Other settings are prohibited.

Current (to):

37.2.3 PLL Control Register (LVDPLLCR / LVD1PLLCR)

RZ/G2H	RZ/G2M V1.3, RZ/G2M V3.0	RZ/G2N	RZ/G2E
√	√	√	√

LVDPLLCR [RZ/G2H, RZ/G2M V1.3, RZ/G2M V3.0, RZ/G2N, RZ/G2E]

LVD1PLLCR [RZ/G2E]

[RZ/G2H, RZ/G2M V1.3, RZ/G2M V3.0, RZ/G2N]

Bit:	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
	—	—	—	—	—	—	—	—	—	—	—	—	—	PLLDIVCNT[18:16]		
Initial value:	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
R/W:	R	R	R	R	R	R	R	R	R	R	R	R	R	R/W	R/W	R/W

Bit:	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
	PLLDIVCNT [15:0]															
Initial value:	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
R/W:	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W

Bit	Bit Name	Initial Value	R/W	Description
31 to 19	—	All 0	R	Reserved [RZ/G2H, RZ/G2M V1.3, RZ/G2M V3.0, RZ/G2N] These bits are always read as 0. The write value should always be 0.
18 to 0	PLLDIVCNT	All 0	R/W	PLL Setting [RZ/G2H, RZ/G2M V1.3, RZ/G2M V3.0, RZ/G2N] Sets the PLL multiplication rate. H'0 14CB: 31 MHz <= dot clock < 42 MHz H'0 0A45: 42 MHz <= dot clock < 85 MHz H'0 06C3: 85 MHz <= dot clock < ~~128 MHz~~ H'0 46C1: 128 MHz <= dot clock <= 150 MHz Other settings are prohibited.

[Description]

Correction of typo in Description.

[Reason for Correction]

Typo mistake in previous version.

[Correction]

3. Page 37-26, 37.3.5 Dot clock Settings, Correction of typo in register bit name of DIDSR.

Current (from):

37.3.5 Dot clock Settings

[RZ/G2H, RZ/G2M V1.3, RZ/G2M V3.0, RZ/G2N]

The LVDS-IF module dot clock frequency is determined by the clock source selected and the divisor settings. This section describes how this frequency is set.

The individual settings are made with the DU (Display Unit) registers. Refer to the corresponding sections for details on the registers, notes, and other information on these settings.

- Clock source selection
  The clock source can be selected to be either the internal clock or an external input (DU_DOTCLKIN*).
  This is set with the DCLKSEL bit in the DU external synchronization control register (ESCR0).
- Divisor setting
  This setting specifies the divisor applied to the clock source.

This is set with the FRQSEL field in the DU external synchronization control register (ESCR0).

[RZ/G2E]

This section describes how this frequency of the LVDS-IF module and the digital output from pin (DPAD) set. Figure 37.6 shows the path for dot clock.

Setting output clock form the LVDS-IF to the DU:

- Clock source of the PLL selection
  The clock source of the PLL can be selected to be either the EXTAL, an external input (DU_DOTCLKIN0/1) or LV0 ϕ /1ϕ clock form CPG. (LVDPLLCR.CKSEL / LVD1PLLCR.CKSEL)
- Frequency of the PLL setting (See Section 37.3.6 PLL Setting)
- 1/N divisor setting (LVDDIV / LVD1DIV)

When the LVDS-IF enable:

- Select 7 divider in the LVDS-IF.
  (LVDS0: LVDPLLCR.OCKSEL = B’0 and LVDPLLCR.CLKOUT = B’1LVDS1: LVD1PLLCR.OCKSEL = B’0 and LVD1PLLCR.CLKOUT = B’1)
- Select the LVDS output clock in the DU0/1.
  (DIDSR0.LVCS0/1 = B’1, ESCR0/1.DCLKSEL = B’0 and ESCR0/1.FRQSEL = B’0*)

Note: * However, when outputting from the LVDS0-IF as section (2) Display of Different Images on Monitors of the Same Size of 35.3.8 Dual Display Output, the output dot clock should be set to be division by two of the input dot clock. (ESCR0.FRQSEL = B’1)

Correct (to):

37.3.5 Dot clock Settings

[RZ/G2H, RZ/G2M V1.3, RZ/G2M V3.0, RZ/G2N]

The LVDS-IF module dot clock frequency is determined by the clock source selected and the divisor settings. This section describes how this frequency is set.

The individual settings are made with the DU (Display Unit) registers. Refer to the corresponding sections for details on the registers, notes, and other information on these settings.

- Clock source selection
  The clock source can be selected to be either the internal clock or an external input (DU_DOTCLKIN*).
  This is set with the DCLKSEL bit in the DU external synchronization control register (ESCR0).
- Divisor setting
  This setting specifies the divisor applied to the clock source.

This is set with the FRQSEL field in the DU external synchronization control register (ESCR0).

[RZ/G2E]

This section describes how this frequency of the LVDS-IF module and the digital output from pin (DPAD) set. Figure 37.6 shows the path for dot clock.

Setting output clock form the LVDS-IF to the DU:

- Clock source of the PLL selection
  The clock source of the PLL can be selected to be either the EXTAL, an external input (DU_DOTCLKIN0/1) or LV0 ϕ /1ϕ clock form CPG. (LVDPLLCR.CKSEL / LVD1PLLCR.CKSEL)
- Frequency of the PLL setting (See Section 37.3.6 PLL Setting)
- 1/N divisor setting (LVDDIV / LVD1DIV)

When the LVDS-IF enable:

- Select 7 divider in the LVDS-IF.
  (LVDS0: LVDPLLCR.OCKSEL = B’0 and LVDPLLCR.CLKOUT = B’1LVDS1: LVD1PLLCR.OCKSEL = B’0 and LVD1PLLCR.CLKOUT = B’1)
- Select the LVDS output clock in the DU0/1.
  (DIDSR0.LDCS0/1 = B’1, ESCR0/1.DCLKSEL = B’0 and ESCR0/1.FRQSEL = B’0*)

Note: * However, when outputting from the LVDS0-IF as section (2) Display of Different Images on Monitors of the Same Size of 35.3.8 Dual Display Output, the output dot clock should be set to be division by two of the input dot clock. (ESCR0.FRQSEL = B’1)

[Description]

Correction of typo in register bit name.

[Reason for Correction]

Typo mistake in previous version.

4. Page 37-30, 37.3.7 Setting Procedure, Item number is corrected.

Current (from):

37.3.7 Setting Procedure

The procedure for using the LVDS-IF module is shown below.

Startup Procedure: Example of ch0

1. Clear the DU and LVDS-IF module standby states using CPG module stop control register.*1
2. Set the DU registers.*2
3. Set the LVDS-IF registers other than LVDCR0.PLLON [RZ/G2H, RZ/G2M V1.3, RZ/G2M V3.0, RZ/G2N], PWD, LVRES, and LVDCR1.CHnSTBY.*3
4. Set LVDCR1.CHnSTBY to B'11 to turn on the LVDS IO.
5. Set LVDCR0.PLLON to B'1 to turn on the PLL. [RZ/G2H, RZ/G2M V1.3, RZ/G2M V3.0, RZ/G2N]
6. Set LVDCR0.PWD to B'1 to turn on the LVDS Normal mode. [RZ/G2H, RZ/G2M V1.3, RZ/G2M V3.0, RZ/G2N]
7. Set LVDCR0.LVEN to B'1 to turn on the LVDS PHY. [RZ/G2E]
8. When all of the following conditions have been met, set LVDCR0.LVRES to B'1.
   At least 100 µs has elapsed since LVDCR0.PLLON and LVDCR0.PWD were set to 1. [RZ/G2H, RZ/G2M V1.3, RZ/G2M V3.0, RZ/G2N]
9. Signals will be output from the LVDS pins after LVDCR0.LVRES is set to B'1. *4

Turning the Display On or Off

Display Off

1. Set LVDCR0.LVRES to B'0 to turn the display off.
2. Set LVDCR0.LVEN to B'0 to turn the LVDS PHY. [RZ/G2E]
3. Set LVDCR0.PWD to B'0 to turn the LVDS Power Down mode.
4. Set LVDCR0.PLLON to B'0 to turn the LVDS-IF PLL circuit off.
5. Set LVDCR1.CHnSTBY to B'0 to turn the LVDS IO off.
6. Set CPG software reset register *5to B'1 to reset LVDS-IF module.

Display On

6. Set CPG software reset clearing register *5to B'1 to clear reset of LVDS-IF module.
7. Re-perform the above procedure [Startup Procedure]

Notes: 1. For the DU and LVDS-IF modules, the initial state is the module standby state. When starting the module immediately after a reset, the module standby state must be cleared.

2. Here, it is possible to proceed as long as the dot clock signal is output. (The LVDS-IF PLL must be started.) Other items may be set while waiting for the conditions of step 6 to be met. [RZ/G2H, RZ/G2M V1.3, RZ/G2M V3.0, RZ/G2N]

   The Clock including the PLL must set before setting the DU registers. (See setup sequence in 37.3.6 PLL Setting.) Also, It is necessary to set the divider (LVDDIV/ LVD1DIV) after the PLL output stable. [RZ/G2E]

3. This refers to settings other than those that are concerned with LVDS-IF startup. These items may be set while waiting for the conditions of step 6 to be met. [RZ/G2H, RZ/G2M V1.3, RZ/G2M V3.0, RZ/G2N]
4. When the vertical stripe output, set LVDCR0.LVRES after set LVD1CR0.LVRES. [RZ/G2E]
5. When display on in the LVDS0-IF, it is necessary to reset (SRCR7[27]) and reset clearing (SRSTCLR7[27]) LVDS0-IF module.

   When display on in the LVDS1-IF, it is necessary to reset (SRCR7[26]) and reset clearing (SRSTCLR7[26]) LVDS0-IF module.

   When display on in the dual output operates, it is necessary to reset (SRCR7[27] and SRCR7[26]) and reset clearing (SRSTCLR7 [27] and SRSTCLR7 [26]) LVDS0-IF and LVDS1-IF module. [RZ/G2E]

Correction (to):

37.3.7 Setting Procedure

The procedure for using the LVDS-IF module is shown below.

Startup Procedure: Example of ch0

1. Clear the DU and LVDS-IF module standby states using CPG module stop control register.*1
2. Set the DU registers.*2
3. Set the LVDS-IF registers other than LVDCR0.PLLON [RZ/G2H, RZ/G2M V1.3, RZ/G2M V3.0, RZ/G2N], PWD, LVRES, and LVDCR1.CHnSTBY.*3
4. Set LVDCR1.CHnSTBY to B'11 to turn on the LVDS IO.
5. Set LVDCR0.PLLON to B'1 to turn on the PLL. [RZ/G2H, RZ/G2M V1.3, RZ/G2M V3.0, RZ/G2N]
6. Set LVDCR0.PWD to B'1 to turn on the LVDS Normal mode. [RZ/G2H, RZ/G2M V1.3, RZ/G2M V3.0, RZ/G2N]
7. Set LVDCR0.LVEN to B'1 to turn on the LVDS PHY. [RZ/G2E]
8. When all of the following conditions have been met, set LVDCR0.LVRES to B'1.
   At least 100 µs has elapsed since LVDCR0.PLLON and LVDCR0.PWD were set to 1. [RZ/G2H, RZ/G2M V1.3, RZ/G2M V3.0, RZ/G2N]
9. Signals will be output from the LVDS pins after LVDCR0.LVRES is set to B'1. *4

Turning the Display On or Off

Display Off

1. Set LVDCR0.LVRES to B'0 to turn the display off.
2. Set LVDCR0.LVEN to B'0 to turn the LVDS PHY. [RZ/G2E]
3. Set LVDCR0.PWD to B'0 to turn the LVDS Power Down mode.
4. Set LVDCR0.PLLON to B'0 to turn the LVDS-IF PLL circuit off.
5. Set LVDCR1.CHnSTBY to B'0 to turn the LVDS IO off.
6. Set CPG software reset register *5to B'1 to reset LVDS-IF module.

Display On

1. Set CPG software reset clearing register *5to B'1 to clear reset of LVDS-IF module.
2. Re-perform the above procedure [Startup Procedure]

Notes: 1. For the DU and LVDS-IF modules, the initial state is the module standby state. When starting the module immediately after a reset, the module standby state must be cleared.

2. Here, it is possible to proceed as long as the dot clock signal is output. (The LVDS-IF PLL must be started.) Other items may be set while waiting for the conditions of step 6 to be met. [RZ/G2H, RZ/G2M V1.3, RZ/G2M V3.0, RZ/G2N]

   The Clock including the PLL must set before setting the DU registers. (See setup sequence in 37.3.6 PLL Setting.) Also, It is necessary to set the divider (LVDDIV/ LVD1DIV) after the PLL output stable. [RZ/G2E]

3. This refers to settings other than those that are concerned with LVDS-IF startup. These items may be set while waiting for the conditions of step 6 to be met. [RZ/G2H, RZ/G2M V1.3, RZ/G2M V3.0, RZ/G2N]
4. When the vertical stripe output, set LVDCR0.LVRES after set LVD1CR0.LVRES. [RZ/G2E]
5. When display on in the LVDS0-IF, it is necessary to reset (SRCR7[27]) and reset clearing (SRSTCLR7[27]) LVDS0-IF module.

   When display on in the LVDS1-IF, it is necessary to reset (SRCR7[26]) and reset clearing (SRSTCLR7[26]) LVDS0-IF module.

   When display on in the dual output operates, it is necessary to reset (SRCR7[27] and SRCR7[26]) and reset clearing (SRSTCLR7 [27] and SRSTCLR7 [26]) LVDS0-IF and LVDS1-IF module. [RZ/G2E]

[Description]

Correction of typo in the item number.

[Reason for Correction]

Typo mistake in previous version.

“This is empty adjustment page to compare next Current (from) and Correction (to) on facing page. “

(By using two pages view of PDF readers this enables previously and prospectively view on odd and even pages.)

[Correction]

5. Page 37-32, 37.3.7 Setting Procedure, Items number corrected.

Current (from):

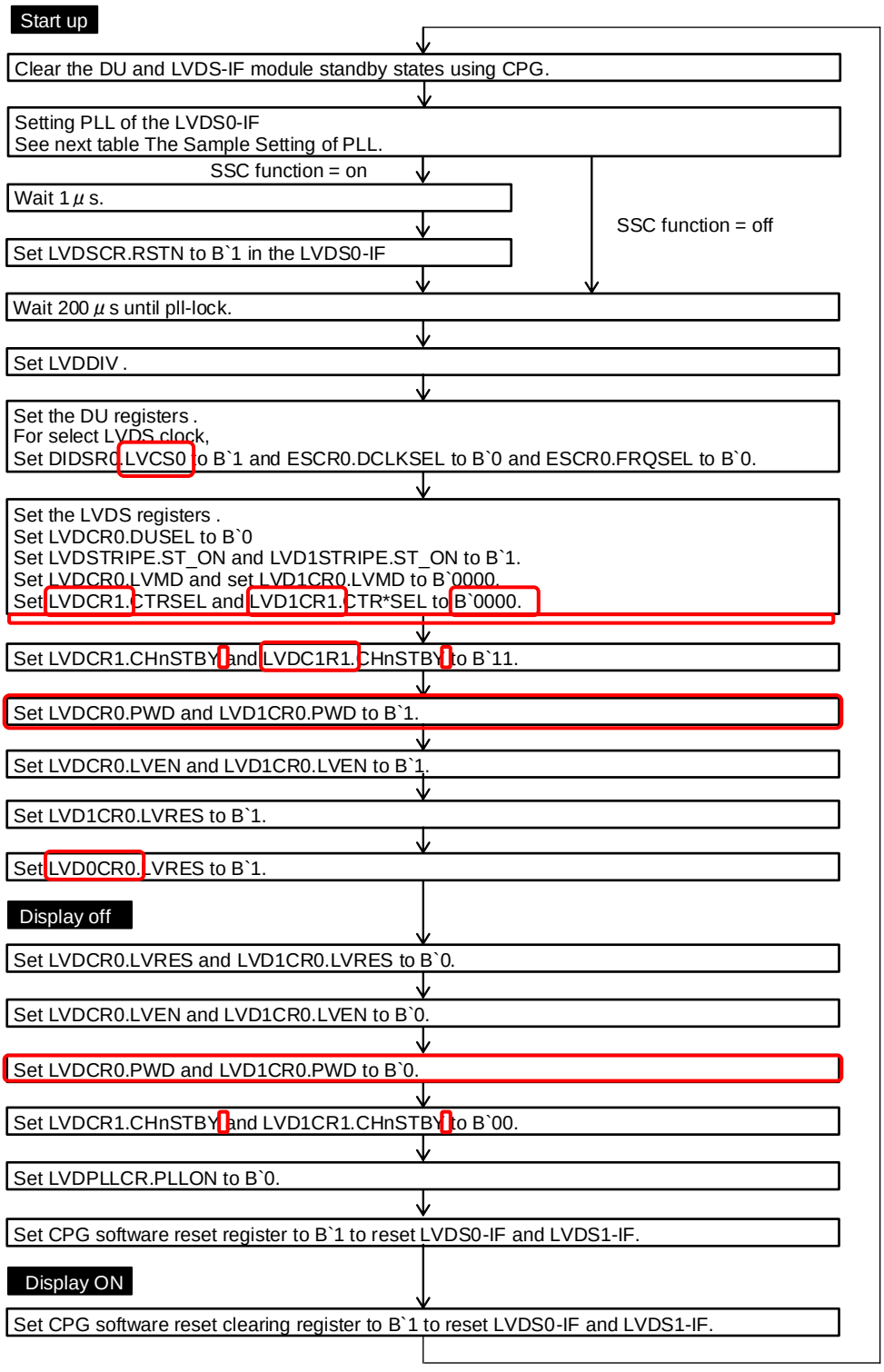

Figure 37.8 The sample setting of the vertical stripe output [RZ/G2E]

Correction (to):

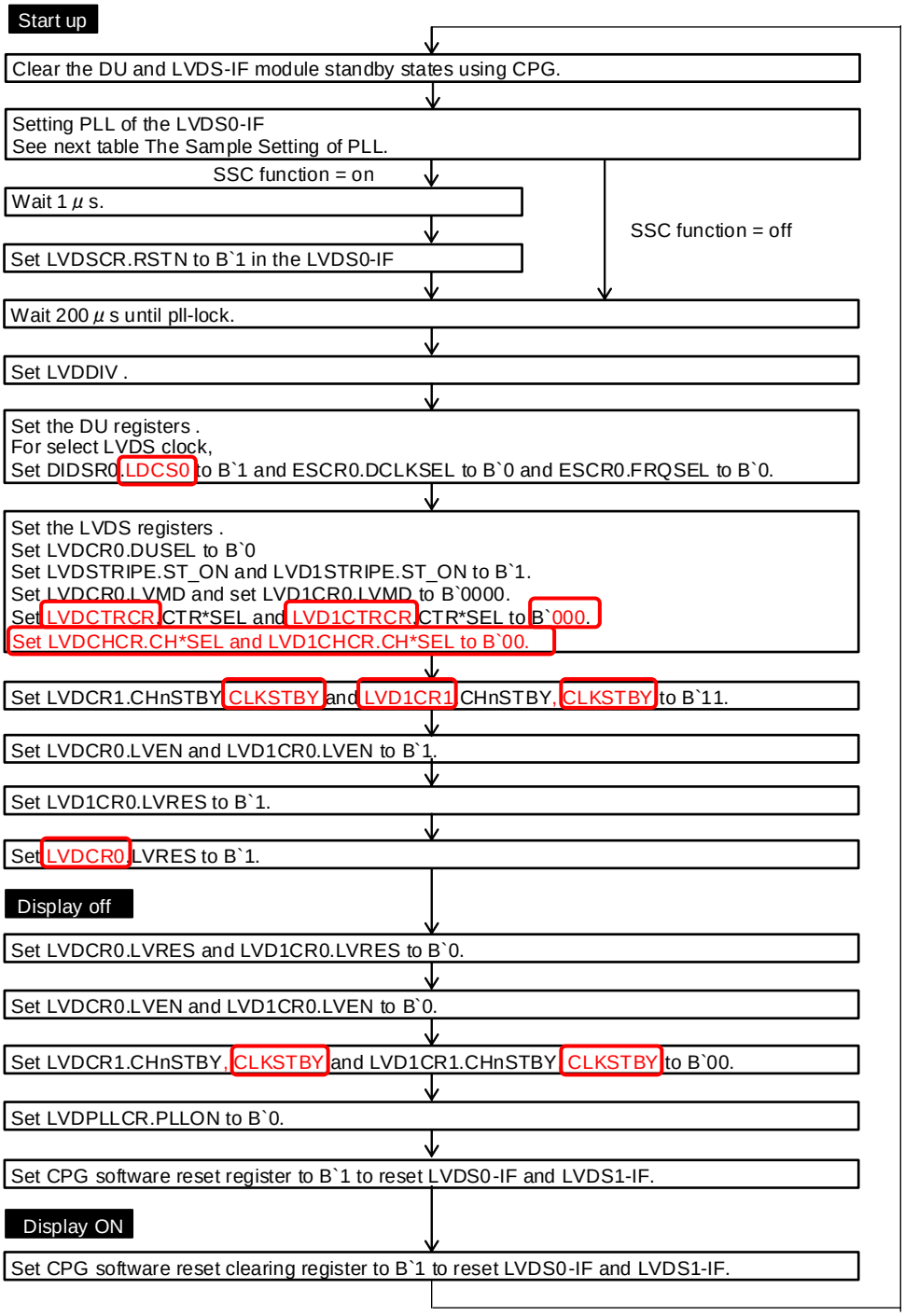

Figure37.8 The sample setting of the vertical stripe output [RZ/G2E]

[Description]

Correction of typo in register bit name.

[Reason for Correction]

Typo mistake in previous version.

6. Page 37-35, 37.4 Usage Notes, Operating frequency is corrected.

Current (from):

37.4 Usage Notes

RZ/G2H
RZ/G2M V1.3 RZ/G2M V3.0
RZ/G2N RZ/G2E

The following notes must be observed when using the LVDS-IF module.

Incorrect operation and damage to the device itself may occur if these notes are not followed.

- Since the LVDS-IF module includes logic that operates from the dot clock signal output by the DU module, incorrect operation may occur if the DU registers are not set appropriately. Also, do not change any DU register values during LVDS-IF operation. (If dot clock output is not stable, the LVDS-IF PLL is unlocked, and thus operation cannot be guaranteed.) There are two DU registers related to dot clock: Display unit System Control Register (DSYSR0) and External Synchronization Control Register (ESCR0). These registers must not be changed during LVDS-IF operation. [RZ/G2H, RZ/G2M V1.3, RZ/G2M V3.0, RZ/G2N]

- Set the dot clock signal, input to the LVDS-IF module to a frequency within the LVDS-IF module's guaranteed operating range (5[RZ/G2E]/ 31[RZ/G2H, RZ/G2M V1.3, RZ/G2M V3.0, RZ/G2N] to 148.5 MHz).

- Application systems should be implemented in a failsafe manner, such as by connecting the LVDS outputs to a failsafe receiver or by connecting terminators, so that no problems in or damage to the application can occur if the LVDS pins become unstable (for example, the differential outputs going to the same level).

Correction (to):

37.4 Usage Notes

RZ/G2H
RZ/G2M V1.3 RZ/G2M V3.0
RZ/G2N RZ/G2E

The following notes must be observed when using the LVDS-IF module.

Incorrect operation and damage to the device itself may occur if these notes are not followed.

- Since the LVDS-IF module includes logic that operates from the dot clock signal output by the DU module, incorrect operation may occur if the DU registers are not set appropriately. Also, do not change any DU register values during LVDS-IF operation. (If dot clock output is not stable, the LVDS-IF PLL is unlocked, and thus operation cannot be guaranteed.) There are two DU registers related to dot clock: Display unit System Control Register (DSYSR0) and External Synchronization Control Register (ESCR0). These registers must not be changed during LVDS-IF operation. [RZ/G2H, RZ/G2M V1.3, RZ/G2M V3.0, RZ/G2N]
- Set the dot clock signal input to the LVDS-IF module to a frequency within the LVDS-IF module's guaranteed operating range (5[RZ/G2E]/ 31[RZ/G2H, RZ/G2M V1.3, RZ/G2M V3.0, RZ/G2N] to 150 MHz).
- Application systems should be implemented in a failsafe manner, such as by connecting the LVDS outputs to a failsafe receiver or by connecting terminators, so that no problems in or damage to the application can occur if the LVDS pins become unstable (for example, the differential outputs going to the same level).

[Description]

Correction of typo in Usage Notes.

[Reason for Correction]

Typo mistake in previous version.

- End of Document -