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RENESAS TECHNICAL UPDATE

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Renesas Electronics Corporation

Product Category	MPU/MCU		Document No.	TN-RZ*-A0135A/E	Rev.	1.00
Title	RZ/G2E Additional Explanations for Pin Multiplex		Information Category	Technical Notification		
Applicable Product	RZ/G Series, 2nd Generation RZ/G2E	Lot No. All lots	Reference Document	RZ/G Series, 2nd Generation User's Manual: Hardware Rev.1.11 Dedicated document for Pin Multiplex of RZ/G2E (EPMP-IMB-20-0060)		

This technical update describes document correction of RZ/G Series, 2nd Generation product.

[Summary]

Additional explanations for “RZ/G Series, 2nd Generation User's Manual: Rev.1.11 Dedicated document for Pin Multiplex of RZ/G2E.

Note: The pin function list reflected the changes of this technical update is attached to this document.

[Priority level]

Importance: “Normal”

Urgency: “Normal”

[Products]

RZ/G2E

[Section number and title]

Dedicated document for Pin Multiplexing [RZ/G2E]

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“This is empty adjustment page to compare next Current (from) and Correction (to) on facing page. “

(By using two pages view of PDF readers this enables previously and prospectively view on odd and even pages.)

[Correction]

1. (Dedicated section). Pin Multiplexing [RZ/G2E],

Notes:

(*1) : When MBKPRST# is at low level, MCKE0 takes on low level and MRESET# high level.

(*2) : after negating PRESET#, pin state is L output and then change to High output.
regarding transition timing, please refer to the Reset section of H/W manual.

(*3) : Use these GPIOs as input only

(*4) : Function is selected based on MD21, MD20, MD11, MDT[1:0]

(*5) : Same with MD[4:1]=serial flash except QSPI.

(*6) : IO should be 1.8V

(*7) : Pull up/down state changes from pull up to pull down at reset. Not suitable for GPIO output usage.

(*8) : Reset state is output and not GPIO. Not suitable for GPIO usage.

(*9) : In case of MD[4:1]=B'001x or B'101x (x: don't care), pin states of the QSPI1_SPCLK and QSPI1_SSL are as follows;
- During RPC_RESET# is low level, QSPI1_SPCLK is low output and QSPI1_SSL is high output.
- During RPC_RESET# is high level, QSPI1_SPCLK is high output and QSPI1_SSL is Hi-Z.

pulldown*(only) : pull-down on/off is controllable in PFC register. Initial state is pulldown on

pullup* : pull-up/down,on/off is controlable in PFC register. Initial state is pullup on

pullup*(only) : pull-up on/off is controlable in PFC register. Initial state is pullup on

* : pull-up/down ,on/off is controlable in PFC register. Initial state is pull off

*(pu only) : pull-up on/off is controlable in PFC register. Initial state is pullup off

- : no pullup/pulldown

(*10) : In the case of an error from on chip Boor ROM, error log is output by using the SCIF pins.

(*11) : The pin condition starts with the pin setting according to the boot device selected by the mode pin.

- During RPC_RESET# is high level, QSPI1_SPCLK is high output and QSPI1_SSL is Hi-Z.

Function0		Debug (TMOND T)	Pin condition at PRESET#=L		Pin condition at PRESET#=H Pin condition after power-on reset deasert(LBSC) MD[4:1]=0000		Pin condition after power-on reset deasert MD[4:1]=serial flash		Pin condition after power-on reset deasert MD[4:1]=eMMC, download mode(*5)	
Pin Name	IO	IO	Pin name	condition	Pin name	condition	Pin name	condition	Pin name	condition
VDDD_USB30	P									
VDDQ18_USB30	P									
USB3HS0_DP	IO									
USB3HS0_DM	IO									
USB3HS0_RREF	IO									
USB0_DP0	IO									
USB0_DM0	IO									
USB0_RREF	IO									
VDDQ18_USB20	P									
AVDD_USB	P									
VDDQ33_USB2	P									

Current (to):

Notes:
(*1) : When MBKPRST# is at low level, MCKE0 takes on low level and MRESET# high level.
(*2) : after negating PRESET#, pin state is L output and then change to High output.
regarding transition timing, please refer to the Reset section of H/W manual.
(*3) : Use these GPIOs as input only
(*4) : Function is selected based on MD21, MD20, MD11, MDT[1:0]
(*5) : Same with MD[4:1]=serial flash except QSPI.
(*6) : IO should be 1.8V
(*7) : Pull up/down state changes from pull up to pull down at reset. Not suitable for GPIO output usage.
(*8) : Reset state is output and not GPIO. Not suitable for GPIO usage.
(*9) : In case of MD[4:1]=B'001x or B'101x (x: don't care), pin states of the QSPI1_SPCLK and QSPI1_SSL are as follows;
- During RPC_RESET# is low level, QSPI1_SPCLK is low output and QSPI1_SSL is high output.
- During RPC_RESET# is high level, QSPI1_SPCLK is high output and QSPI1_SSL is Hi-Z.

pulldown*(only) : pull-down on/off is controllable in PFC register. Initial state is pulldown on
pullup* : pull-up/down,on/off is controlable in PFC register. Initial state is pullup on
pullup*(only) : pull-up on/off is controlable in PFC register. Initial state is pullup on
* : pull-up/down ,on/off is controlable in PFC register. Initial state is pull off
*(pu only) : pull-up on/off is controlable in PFC register. Initial state is pullup off
- : no pullup/pulldown

(*10) : In the case of an error from on chip Boor ROM, error log is output by using the SCIF pins.
(*11) : The pin condition starts with the pin setting according to the boot device selected by the mode pin.
(*12) The USB data pins have their own pull pull-up/down control function.
Affected pins are as follows: USB3HS0_DP, USB3HS0_DM and USB USB0_DP DP0, USB USB0_DM 0. For more information, see Chapters 60.2, 60.7 to 60.8 and Chapters 61.2 to 61.3.
The processing of the USB-Data pins on the PCB must be designed in accordance with the PCB guidelines described in "Design Guidelines for Serial Interface Printed Circuit Boards with RZ/G2E".
Please contact Renesas Electronics Corporation for details about the Design Guidelines.

#Function0		Debug (TMONDT) (*6)		Pin condition at PRESET#=L		Pin condition at PRESET#=H Pin condition after power-on reset deasert(LBSC) MD[4:1]=0000		Pin condition after power-on reset deasert MD[4:1]=serial flash		Pin condition after power-on reset deasert MD[4:1]=eMMC, download mode(*5)	
Pin Name	IO	Pin Name	IO	Pin name	condition	Pin name	condition	Pin name	condition	Pin name	condition
VDDD_USB30	P										
VDDQ18_USB30	P										
USB3HS0_DP	IO									(*12)	
USB3HS0_DM	IO									(*12)	
USB3HS0_RREF	IO										
USB0_DP0	IO									(*12)	
USB0_DM0	IO									(*12)	
USB0_RREF	IO										
VDDQ18_USB20	P										

[Description]

Note (*12) for the USB data pins is added.

[Reason for Correction]

General error correction.

To avoid misunderstanding about IP pins internal pull-up/pull-down control.

End of Document -