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RENESAS TECHNICAL UPDATE

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Product Category	MPU/MCU		Document No.	TN-RZ*-A0113A/E	Rev.	1.00
Title	RZ/G1H, G1M, G1N and G1E Correction of section 15. External Bus Controller for DDR3-SDRAM (DBSC3)		Information Category	Technical Notification		
Applicable Product	RZ/G Series, RZ/G1H, RZ/G1M, RZ/G1N, RZ/G1E	Lot No. All lots	Reference Document	RZ/G Series, User's Manual: Hardware Rev.1.00 (R01UH0543EJ0100)		

This technical update describes document correction of RZ/G Series product.

[Summary]

Document correction for section 15. External Bus Controller for DDR3-SDRAM (DBSC3).

[Priority level]

Importance: “Normal”

Urgency: “Normal”

[Products]

RZ/G1H,

RZ/G1M,

RZ/G1N,

RZ/G1E

[Section number and title]

Section 15. External Bus Controller for DDR3-SDRAM (DBSC3)

“This is empty adjustment page to compare next Current (from) and Correction (to) on facing page. “

(By using two pages view of PDF readers this enables previously and prospectively view on odd and even pages.)

[Correction]

1. Section 15.8 M0(/1) RESET# pin level during DDR power-up, new section is added.

Current (from):

— (none)

Correction (to):

RZ/G1H RZ/G1N
RZ/G1M RZ/G1E

15.9 M0(/1)RESET# pin level during DDR power-up

The pin level of M0(/1)RESET# is undefined during DDR power-up as shown in Figure 15.29

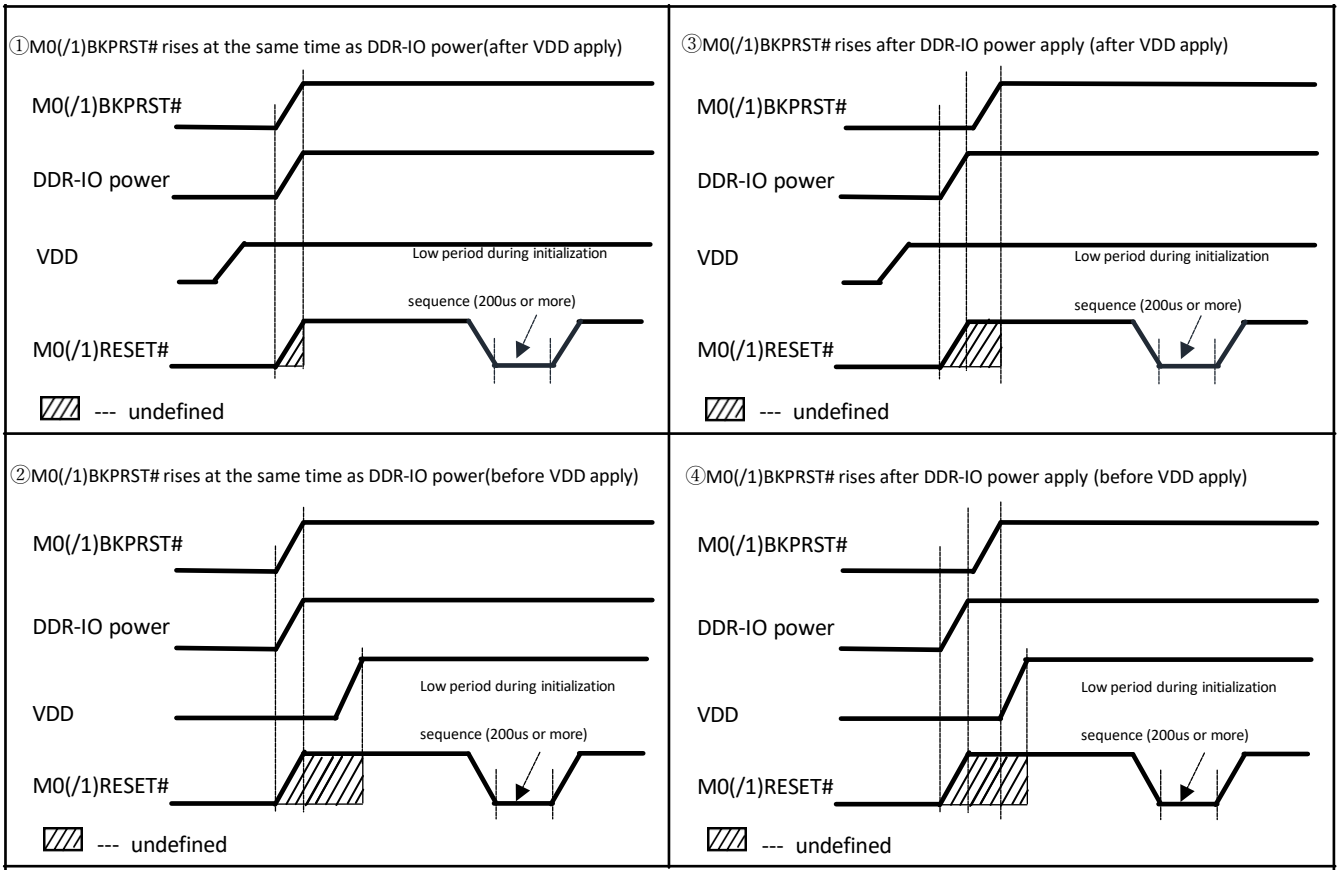

Figure 15.29 M0(/1)RESET# pin level during DDR power-up

[Description]

M0(/1)RESET# pin level during DDR power-up.

[Reason for Correction]

Caution for M0(/1)RESET# pin level during DDR power-up.

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