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RENESAS TECHNICAL UPDATE

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Product Category	MPU/MCU		Document No.	TN-RX*-A0252A/E	Rev.	1.00
Title	RX66N Group, RX72M Group, and RX72N Group, Expansion of the Lower Limit of the Power Supply Voltage Supplied to the Battery Backup Power Supply Pin		Information Category	Technical Notification		
Applicable Product	RX66N Group, RX72M Group, RX72N Group	Lot No. All	Reference Document	User's Manual: Hardware for applicable products (see the table at the last page)		

This document describes an extension of the lower limit of the power supply voltage supplied to the battery backup power supply pin for the applicable products.
Page and table numbers are based on the RX66N Group. Refer to the table on the last page for the corresponding page and table numbers in the other groups.

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The description for power supply voltage in Table 1.1, Outline of Specifications (11/11) is changed as follows.

Before correction

Table 1.1 Outline of Specifications (11/11)

Classification	Module/Function	Description
		Omitted.
Power supply voltage		VCC = AVCC0 = AVCC1 = VCC_USB = 2.7 to 3.6 V, 2.7 ≤ VREFH0 ≤ AVCC0, V_{BATT} = 2.0 to 3.6 V
		Omitted.

After correction

Table 1.1 Outline of Specifications (11/11)

Classification	Module/Function	Description
		Omitted.
Power supply voltage		VCC = AVCC0 = AVCC1 = VCC_USB = 2.7 to 3.6 V, 2.7 ≤ VREFH0 ≤ AVCC0, V_{BATT} = 1.62 to 3.6 V*4
		Omitted.

Omitted.

Note 4. The low CL crystal unit cannot be used when the V_{BATT} voltage is less than 2.0 V.

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The specification for V_{BATT} power supply voltage and the description of Note 4 in Table 61.2, Recommended Operating Conditions (1) are changed as follows.

Before correction

Table 61.2 Recommended Operating Conditions (1)

Item	Symbol	Min.	Typ.	Max.	Unit
Omitted.					
V_{BATT} power supply voltage	V_{BATT}	2.0	—	3.6	V
Omitted.					
Input voltage (5V tolerant ports: P11 to P17, P20, P21, P30 to P33, P67, and PC0 to PC3)*4	V_{in}	–0.3	—	VCC + 3.6 (up to 5.5)	V
Omitted.					

Omitted.

Note 4. For P30 to P32, input as follows when the V_{BATT} power supply is selected.
V_{in} Min. = –0.3, Max. = V_{BATT} + 0.3 (V_{BATT} = 2.0 to 3.6 V)

After correction

Table 61.2 Recommended Operating Conditions (1)

Item	Symbol	Min.	Typ.	Max.	Unit
Omitted.					
V_{BATT} power supply voltage	V_{BATT}	1.62*2	—	3.6	V
Omitted.					
Input voltage (5V tolerant ports: P11 to P17, P20, P21, P30 to P33, P67, and PC0 to PC3)*5	V_{in}	–0.3	—	VCC + 3.6 (up to 5.5)	V
Omitted.					

Omitted.

Note 2. The low CL crystal unit cannot be used when the V_{BATT} voltage is less than 2.0 V.

Omitted.

Note 5. For P30 to P32, input as follows when the V_{BATT} power supply is selected.
V_{in} Min. = –0.3, Max. = V_{BATT} + 0.3 (V_{BATT} = 1.62 to 3.6 V)

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The description of Note 3 in Table 61.4, DC Characteristics (1) is changed as follows.

Before correction

Note 3. For P30 to P32, input as follows when the V_{BATT} power supply is selected.
V_{IH} Min. = V_{BATT} × 0.8, V_{IL} Max. = V_{BATT} × 0.2 (V_{BATT} = 2.0 to 3.6 V)

After correction

Note 3. For P30 to P32, input as follows when the V_{BATT} power supply is selected.
V_{IH} Min. = V_{BATT} × 0.8, V_{IL} Max. = V_{BATT} × 0.2 (V_{BATT} = 1.62 to 3.6 V)

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The characteristics of RTC operating current when a standard CL crystal is in use under the condition of V_{BATT} = 1.62 V are added to Table 61.6, DC Characteristics (3) as follows.

Before correction

Table 61.6 DC Characteristics (3)

Conditions: VCC = AVCC0 = AVCC1 = VCC_USB = 2.7 to 3.6 V, 2.7 V ≤ VREFH0 ≤ AVCC0,
VSS = AVSS0 = AVSS1 = VREFL0 = VSS_USB = 0 V,
$T_a = T_{opr}$

Item			Symbol	D version		G version		Unit	Test Conditions
				Typ.	Max.	Typ.	Max.		
Supply current*1	Omitted.		I_{CC}*3	Omitted.					
	When the RTC is operating while VCC is not supplied (Only the RTC and sub-clock oscillator operate with the battery backup function)	When a low C_L crystal is in use		0.9	—	0.9	—	μA	V_{BATT} = 2.0 V, VCC = 0 V
				1.6	—	1.6	—		V_{BATT} = 3.3 V, VCC = 0 V
		When a standard C_L crystal is in use		1.7	—	1.7	—		V_{BATT} = 2.0 V, VCC = 0 V
				3.3	—	3.3	—		V_{BATT} = 3.3 V, VCC = 0 V
	Omitted.								

After correction

Table 61.6 DC Characteristics (3)

Conditions: VCC = AVCC0 = AVCC1 = VCC_USB = 2.7 to 3.6 V, 2.7 V ≤ VREFH0 ≤ AVCC0,
VSS = AVSS0 = AVSS1 = VREFL0 = VSS_USB = 0 V,
$T_a = T_{opr}$

Item			Symbol	D version		G version		Unit	Test Conditions
				Typ.	Max.	Typ.	Max.		
Supply current*1	Omitted.		I_{CC}*3	Omitted.					
	When the RTC is operating while VCC is not supplied (Only the RTC and sub-clock oscillator operate with the battery backup function)	When a low C_L crystal is in use		0.9	—	0.9	—	μA	V_{BATT} = 2.0 V, VCC = 0 V
				1.6	—	1.6	—		V_{BATT} = 3.3 V, VCC = 0 V
		When a standard C_L crystal is in use		1.6	—	1.6	—		V_{BATT} = 1.62 V, VCC = 0 V
				1.7	—	1.7	—		V_{BATT} = 2.0 V, VCC = 0 V
				3.3	—	3.3	—		V_{BATT} = 3.3 V, VCC = 0 V
	Omitted.								

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The V_{BATT} voltage in Conditions of Table 61.20, Sub-Clock Timing is changed as follows.

Before correction

Table 61.20 Sub-Clock Timing

Conditions: VCC = AVCC0 = AVCC1 = VCC_USB = 2.7 to 3.6 V, 2.7 V ≤ VREFH0 ≤ AVCC0,
VSS = AVSS0 = AVSS1 = VREFL0 = VSS_USB = 0 V,
V_{BATT} = 2.0 to 3.6 V, $T_a = T_{opr}$

After correction

Table 61.20 Sub-Clock Timing

Conditions: VCC = AVCC0 = AVCC1 = VCC_USB = 2.7 to 3.6 V, 2.7 V ≤ VREFH0 ≤ AVCC0,
VSS = AVSS0 = AVSS1 = VREFL0 = VSS_USB = 0 V,
V_{BATT} = 1.62 to 3.6 V, $T_a = T_{opr}$

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The V_{BATT} voltage in Conditions of Table 61.21, CLKOUT Pin Output Timing is changed as follows.

Before correction

Table 61.21 CLKOUT Pin Output Timing

Conditions: VCC = AVCC0 = AVCC1 = VCC_USB = 2.7 to 3.6 V, 2.7 V ≤ VREFH0 ≤ AVCC0,
VSS = AVSS0 = AVSS1 = VREFL0 = VSS_USB = 0 V,
V_{BATT} = 2.0 to 3.6 V, $T_a = T_{opr}$,
High-drive output is selected by the driving ability control register

After correction

Table 61.21 CLKOUT Pin Output Timing

Conditions: VCC = AVCC0 = AVCC1 = VCC_USB = V_{BATT} = 2.7 to 3.6 V, 2.7 V ≤ VREFH0 ≤ AVCC0,
VSS = AVSS0 = AVSS1 = VREFL0 = VSS_USB = 0 V,
$T_a = T_{opr}$,
High-drive output is selected by the drive capacity control register

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The V_{BATT} voltage in Conditions of Table 61.22, CLKOUT25M Pin Output Timing is changed as follows.

Before correction

Table 61.22 CLKOUT25M Pin Output Timing

Conditions: VCC = AVCC0 = AVCC1 = VCC_USB = 2.7 to 3.6 V, 2.7 V ≤ VREFH0 ≤ AVCC0,
VSS = AVSS0 = AVSS1 = VREFL0 = VSS_USB = 0 V,
V_{BATT} = 2.0 to 3.6 V, $T_a = T_{opr}$,
High-speed interface high-drive is selected by the driving ability control register

After correction

Table 61.22 CLKOUT25M Pin Output Timing

Conditions: VCC = AVCC0 = AVCC1 = VCC_USB = V_{BATT} = 2.7 to 3.6 V, 2.7 V ≤ VREFH0 ≤ AVCC0,
VSS = AVSS0 = AVSS1 = VREFL0 = VSS_USB = 0 V,
$T_a = T_{opr}$,
High-speed interface high-drive output is selected by the drive capacity control register

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The V_{BATT} voltage in Conditions of Table 61.60, Battery Backup Function Characteristics is changed as follows.

Before correction

Table 61.60 Battery Backup Function Characteristics

Conditions: VCC = AVCC0 = AVCC1 = VCC_USB = 2.7 to 3.6 V, 2.7 V ≤ VREFH0 ≤ AVCC0,
VSS = AVSS0 = AVSS1 = VREFL0 = VSS_USB = 0 V,
V_{BATT} = 2.0 to 3.6 V, $T_a = T_{opr}$

After correction

Table 61.60 Battery Backup Function Characteristics

Conditions: VCC = AVCC0 = AVCC1 = VCC_USB = 2.7 to 3.6 V, 2.7 V ≤ VREFH0 ≤ AVCC0,
VSS = AVSS0 = AVSS1 = VREFL0 = VSS_USB = 0 V,
V_{BATT} = 1.62 to 3.6 V, $T_a = T_{opr}$

Reference Documents

Applicable Products	Manual Title (Document Number)
RX66N Group	RX66N Group User's Manual: Hardware Rev1.11 (R01UH0825EJ0111)
RX72M Group	RX72M Group User's Manual: Hardware Rev1.11 (R01UH0804EJ0111)
RX72N Group	RX72N Group User's Manual: Hardware Rev1.11 (R01UH0824EJ0111)

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